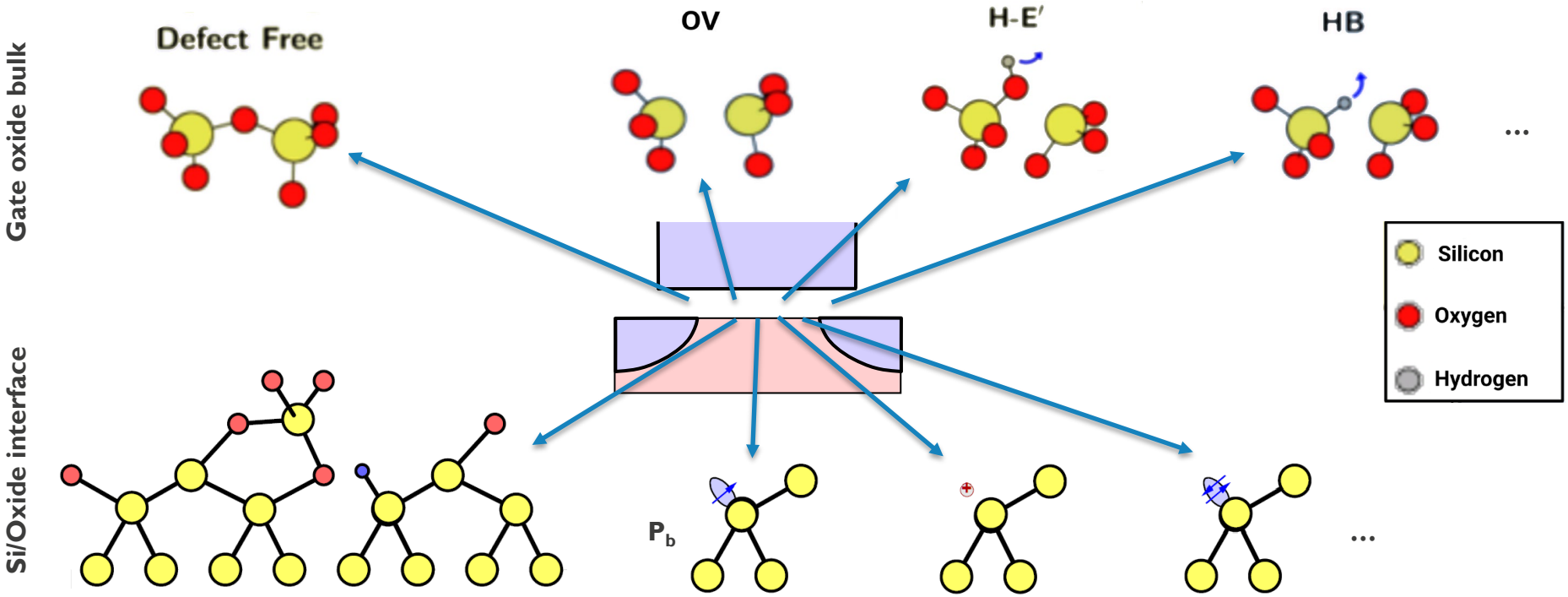
Toward reliability-aware physics-based FET compact models

B. Kaczer, Z. Wu, Y. Xiang, M. Vandemaele, S. Tyaginov, J. Franco, E. Bury, A. Grill, J. Diaz-Fortuny, A. Vaisman Chasin, Ph. J. Roussel, R. Degraeve, B. Parvais, S. Mishra, P. Weckx

VLSI technology is less than ideal

(Even though some would want you to believe otherwise)



- Defects trap charge and distort FET characteristics

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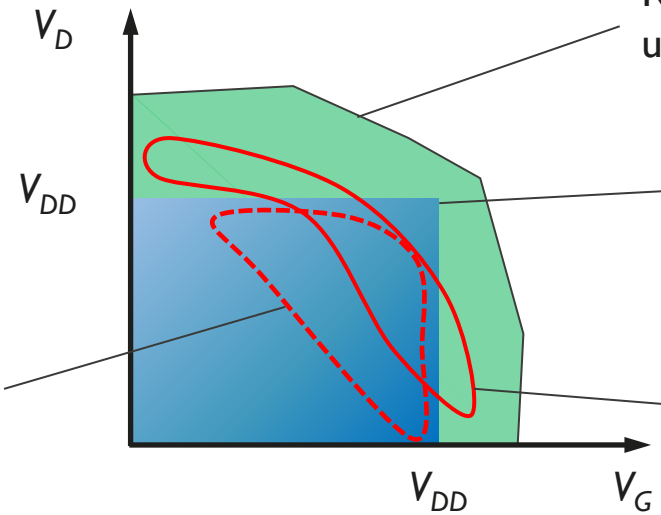
Our goal: unified physics-based reliability model for FETs

Covering entire (V_G,V_D) space

- Qualify and improve technology for reliability within V_{DD}
- Provide unified physics-based FEOL reliability model, based on deep understanding of underlying reliability phenomena



Real reliable conditions predicted by unified reliability model

Reliability guaranteed by fab

Product A:
Designed within V_{DD}

Product B:
Designed for real boundaries
→ Outperforms Product A

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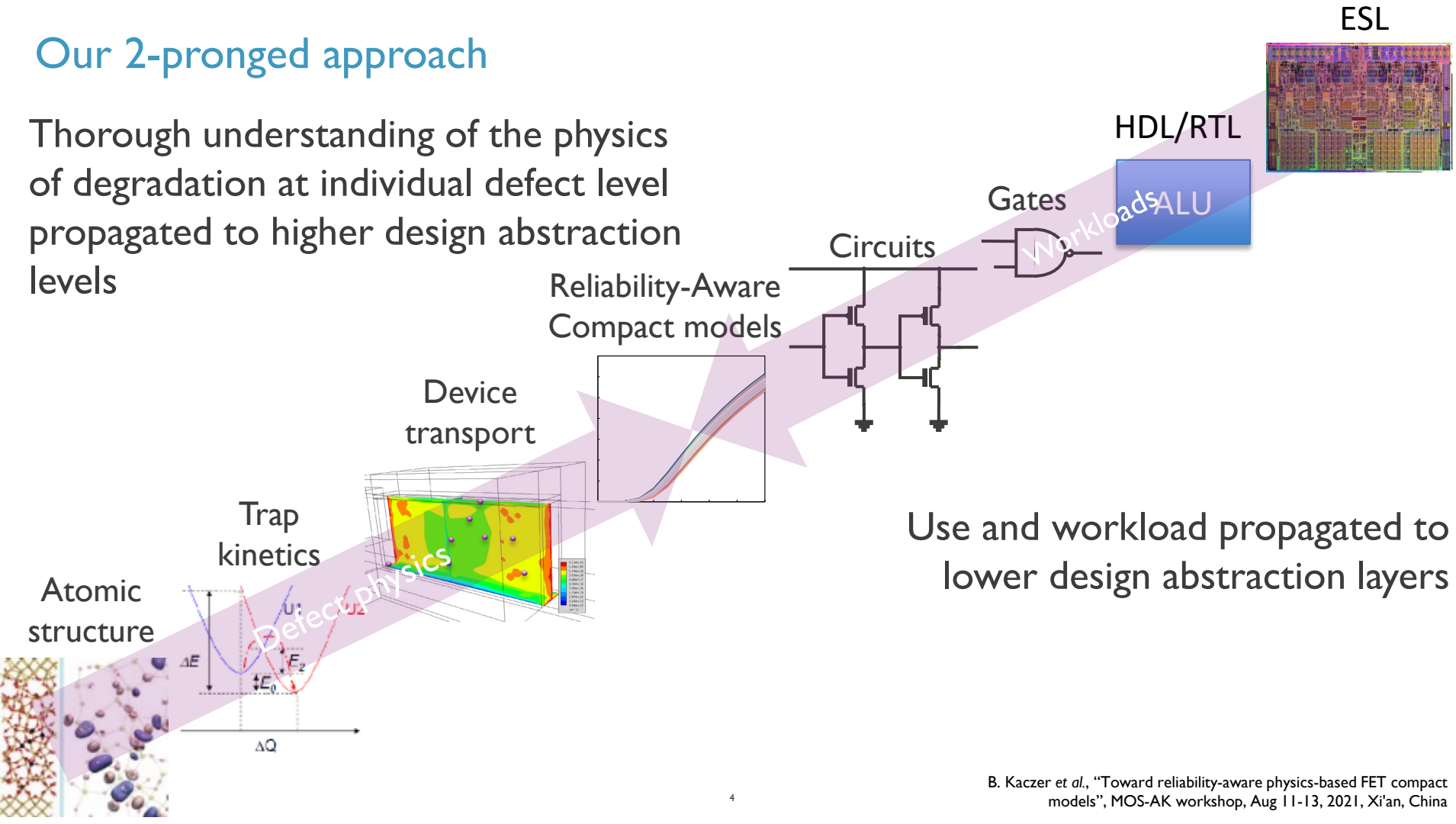
Our 2-pronged approach

Thorough understanding of the physics of degradation at individual defect level propagated to higher design abstraction levels



Use and workload propagated to lower design abstraction layers

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Purpose

- Construct a **Reliability-Aware** FET Compact Model

Encompasses our deep physical understanding of FET degradation mechanisms

Usable and appreciated by designers

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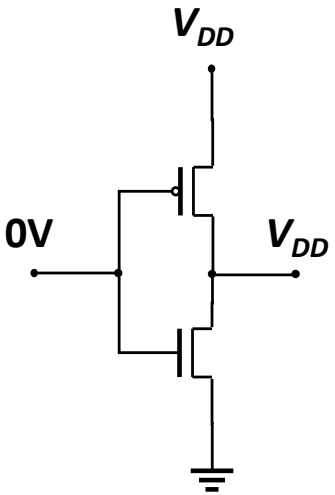
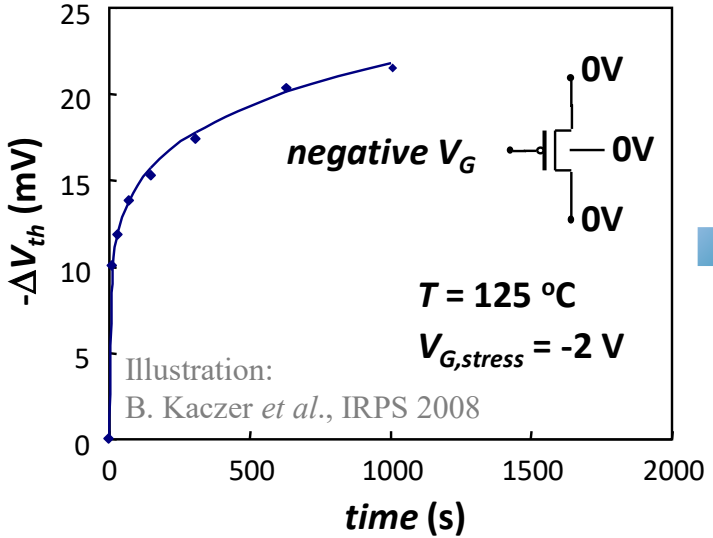
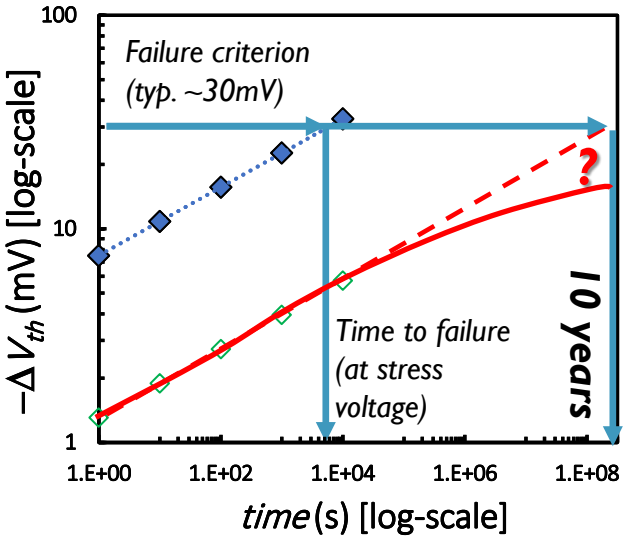
Drift of FET parameters during accelerated stress and operation

E.g.: pFET V_{th} at ***Negative*** gate ***Bias*** (and typically at elevated ***Temperature***) starts shifting (→shows ***Instability***)







- BTI affects FET threshold voltage, transconductance, subthreshold slope, ...
- Projections require understanding degradation physics

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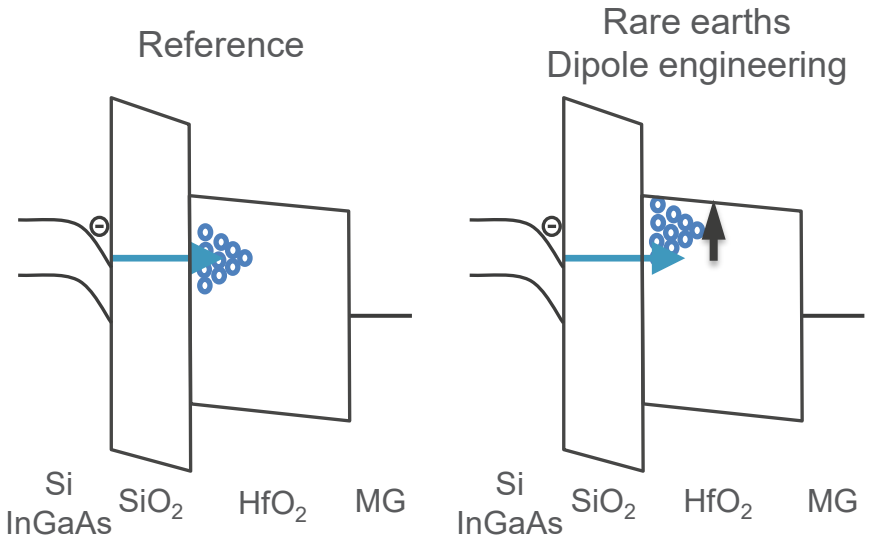
Our **trap** level "misalignment" model for BTI very successful

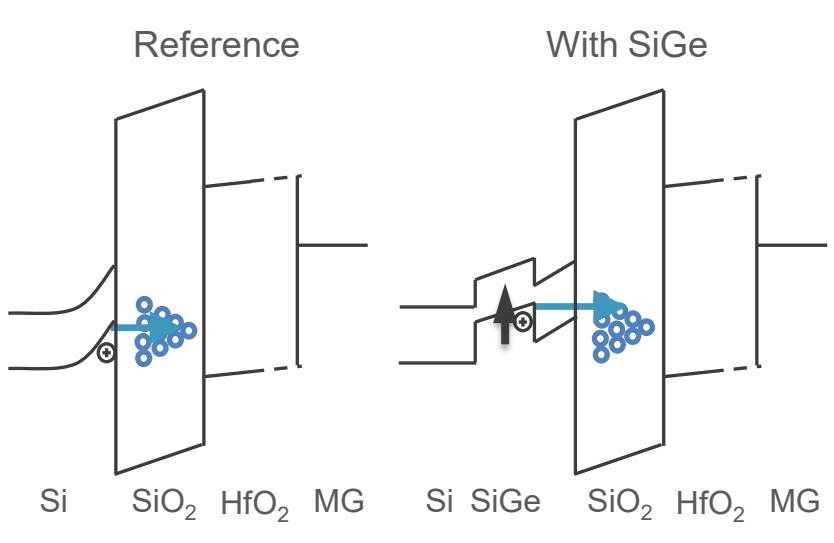
PBTI



e.g. Si: Kaczer *et al.*, Micr. Eng. (86) 2009

InGaAs: Franco *et al.*, VLSI 2016, etc...

NBTI



J. Franco *et al.*, IEEE TED 2013, Part II

Patent: US8062962, etc...

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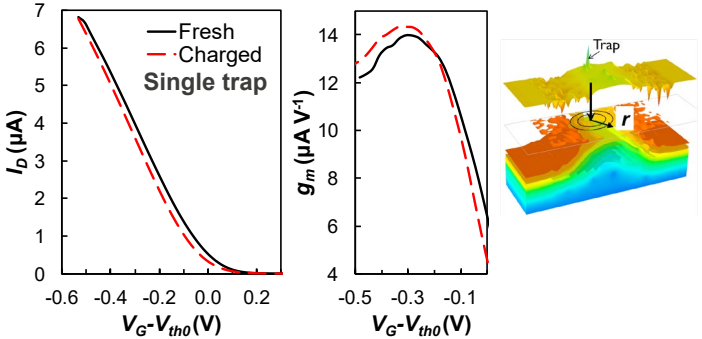
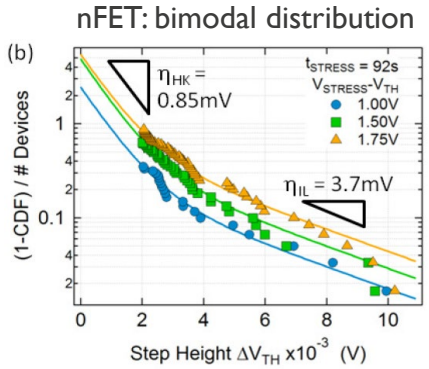
Measurements and deep understanding of single-defect properties

We can measure of capture & emission times, occupancy of **single traps** as a function of V, T, f, mechanical strain



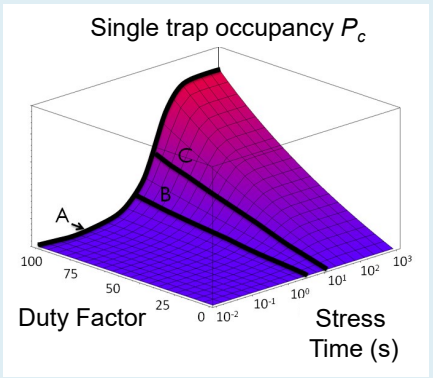
Franco *et al.*, "Impact of **Single** Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs", IRPS (2012)



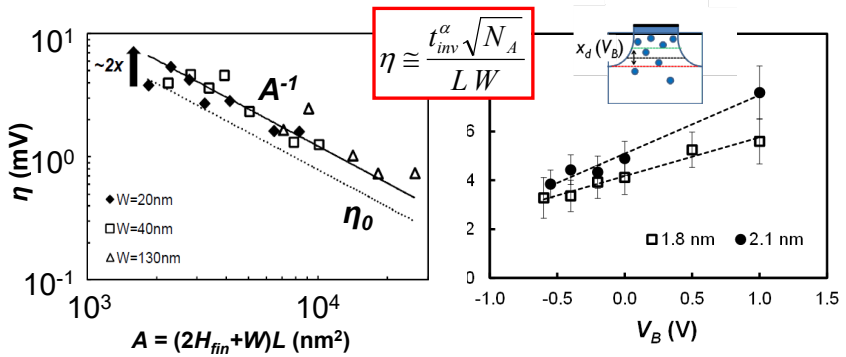
Toledano-Luque *et al.*, "From mean values to distributions of BTI lifetime of deeply scaled FETs through atomistic understanding of the degradation", VLSI (2011)

electrostatics

temporal

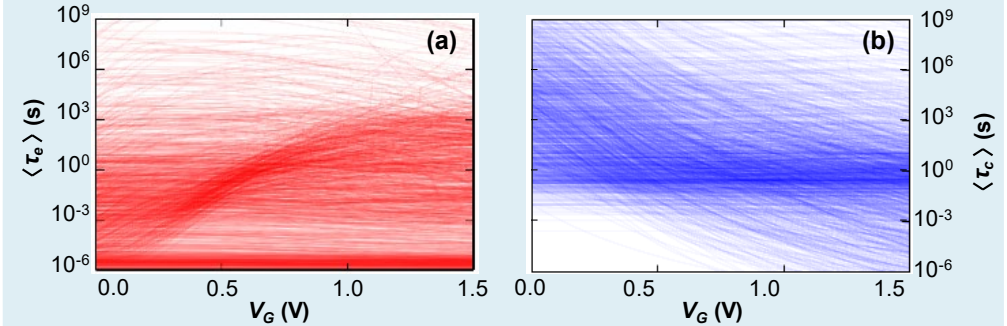


Toledano-Luque *et al.*, "Response of a single trap to **AC** Negative Bias Temperature Stress", IRPS (2011)



Franco *et al.*, "Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs", IRPS (2012)

Franco *et al.*, "Reduction of the BTI Time-Dependent Variability in Nanoscaled MOSFETs by Body Bias", Proc. Int. Reliab. Phys. Symp. (IRPS), pp. 2D.3.1—2D.3.6 (2013)



Kaczer *et al.*, "A brief overview of gate oxide defect properties and their relation to MOSFET instabilities and device and circuit time-dependent variability", Microelectronics Reliability 81 (2018) 186–194; "The defect-centric perspective of device and circuit reliability—From gate oxide defects to circuits", Solid-State Electronics 125 (2016) 52–62

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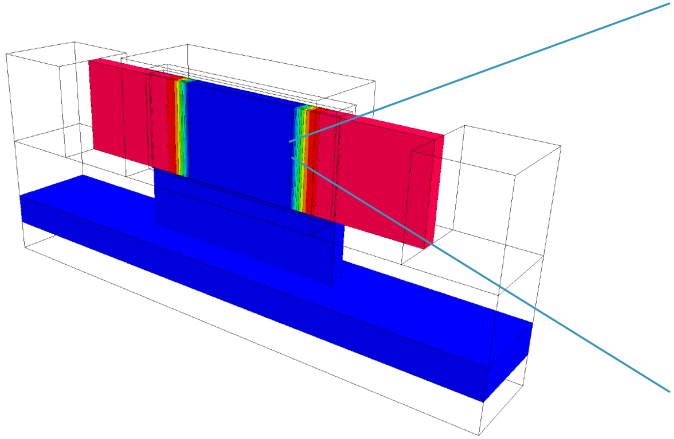
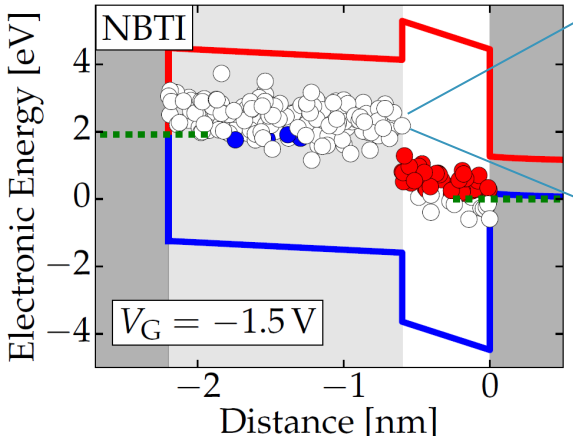
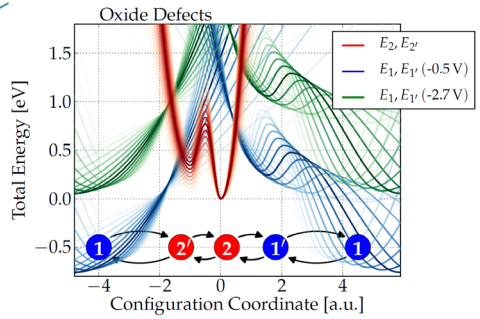
Full TCAD with 4-state NMP traps: Accurate but complex





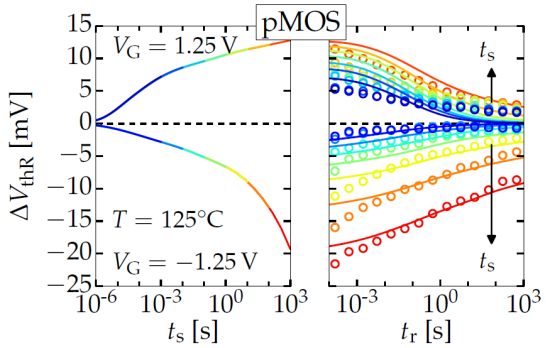


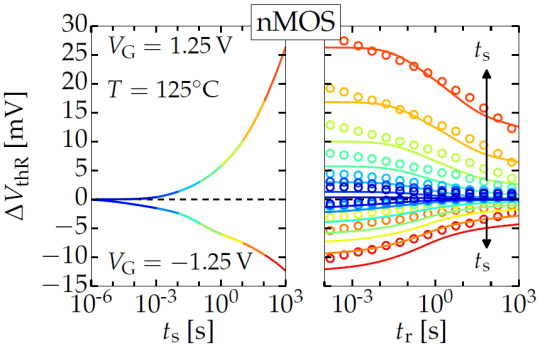
Each four-state NMP trap:

x_t, E_1, E_{1p}, E_{2p}, Eps_{11p}, Eps_{22p}
R_{12p}, S_{12p}, R_{21p}, S_{21p}

+ Fully physical
– Very complex & CPU time consuming

More info about trap distributions: PBTI / PFET and NBTI / NFET (Rzepa et al., VLSI 2016)





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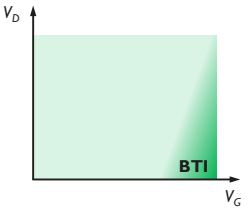
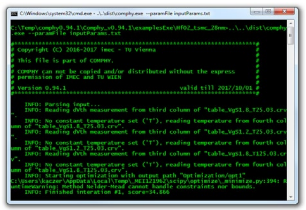
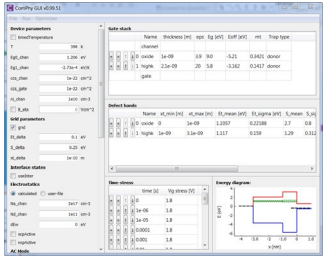
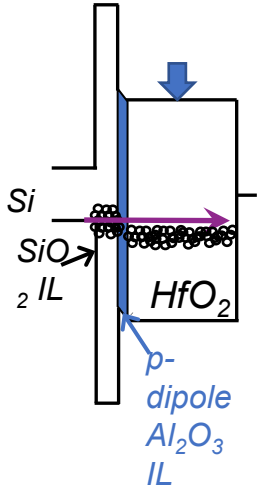
COMPHY: Compact physical BTI model

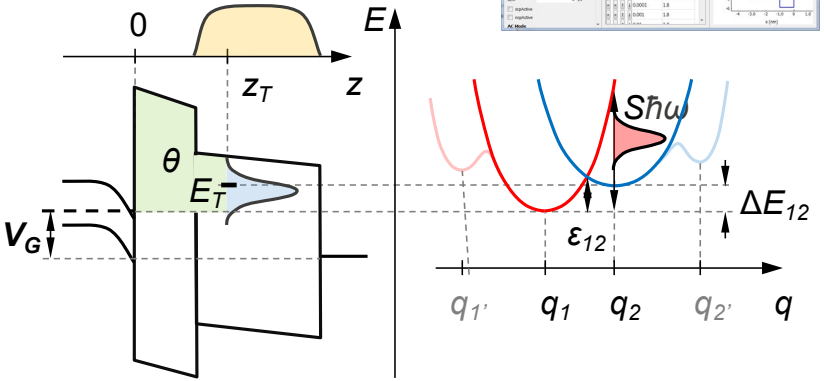


processing & pathfinding

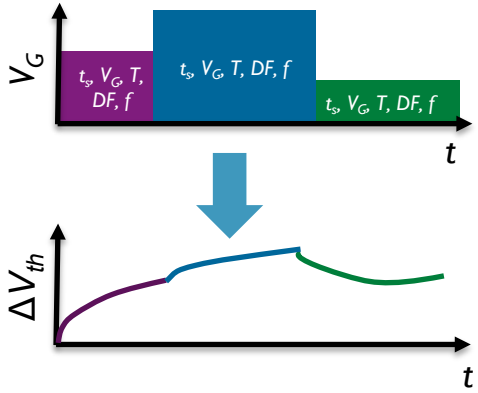








reliability/variability aware design



- Fully physical
- Defect levels
- Distributed parameters

+ voltage/temperature dependence (incl. outside operating conditions)
+ arbitrary ("stress & relax") workload reproduced
  → projections, modeling, simulations
+ extensible to variability/RTN etc.
– advanced effects (anomalous RTN, *f* dependence, etc.) not covered

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Rzepa *et al.*, MR 2018; http://comphy.eu/

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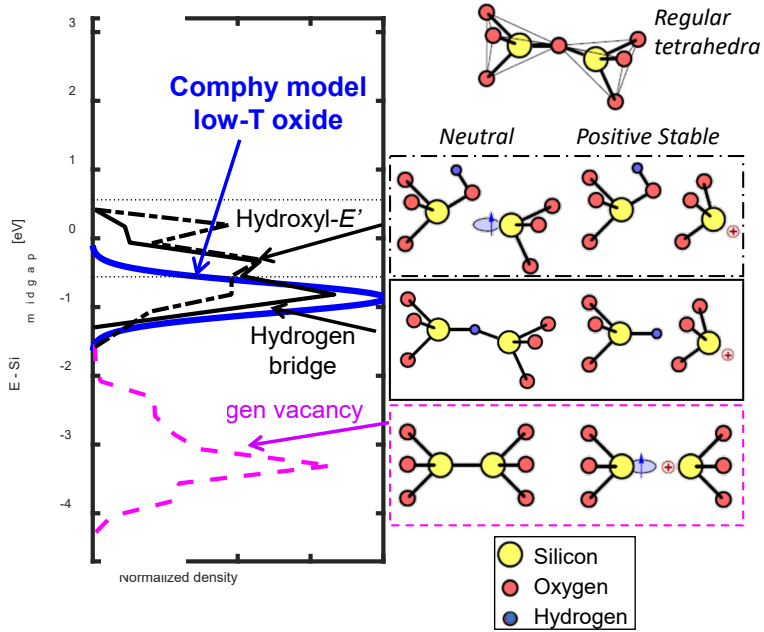
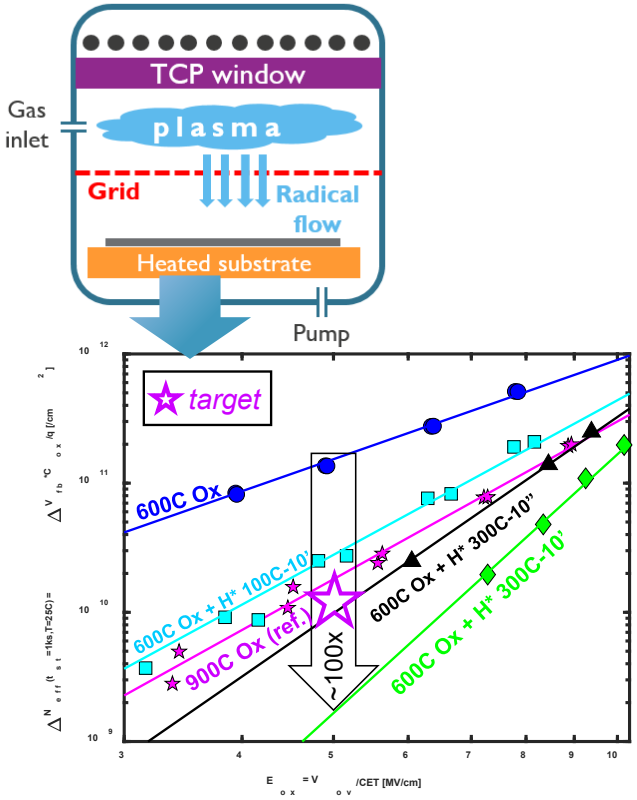
Reliability improvements at technology levels still possible: Outstanding Low-T Gate Stack Reliability achieved by identifying and targeting defects





H-related defects identified as reliability bottleneck for Seq3D low-T oxide
→ suppressed by targeted **atomic hydrogen exposure**

J. Franco *et al.*, IEDM 2020, VLSI 2021

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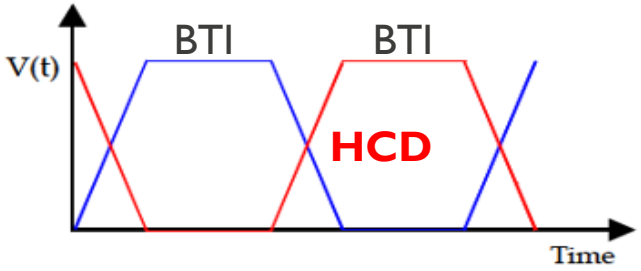
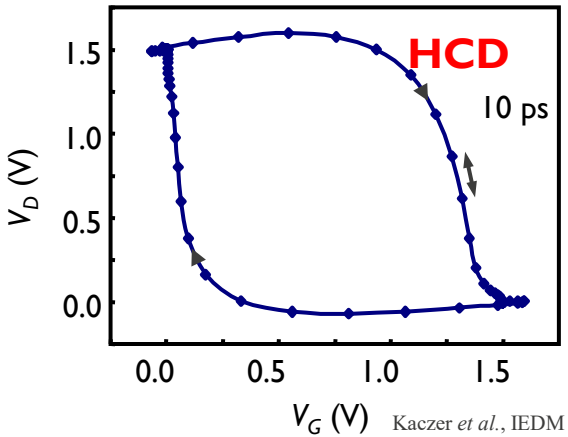
HCD degradation typically strongly non-uniform

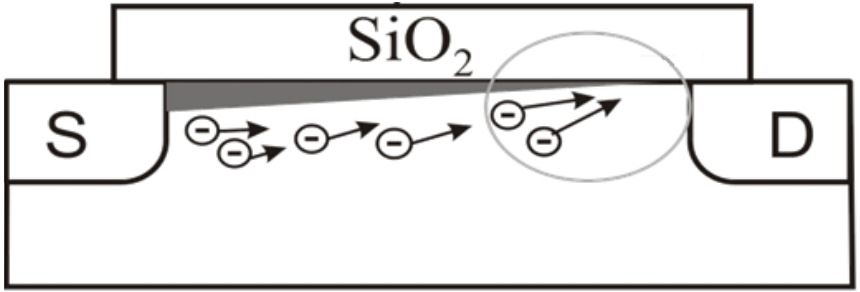
(One of the benchmarks of our models)





Kaczer *et al.*, IEDM 2002

- In digital applications HCD occurs during switching
- Highest carrier energy at the drain → (typically) **largest degradation at the drain**



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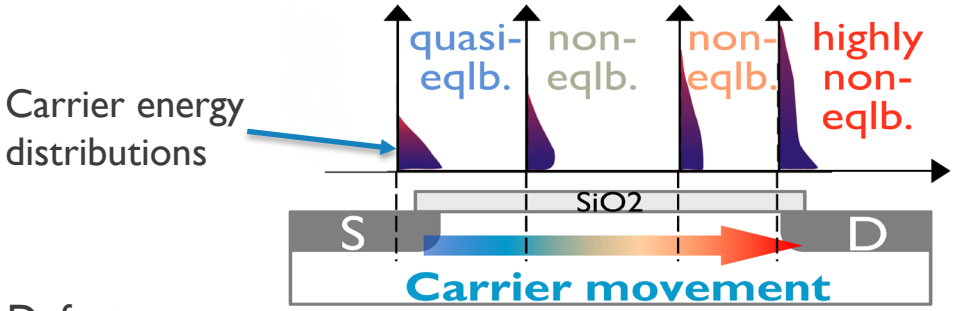
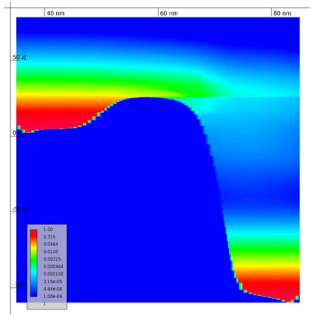
Hot Carrier Degradation (HCD): Carrier energy distributions and defects

Main concepts

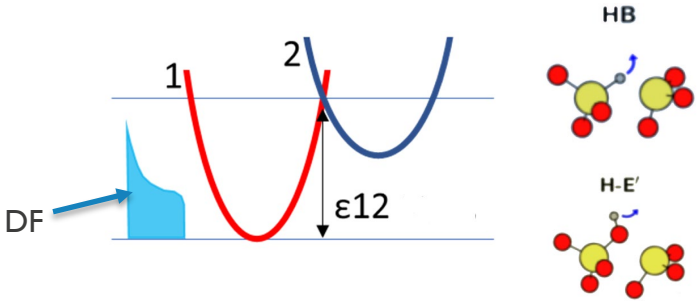
- Carrier energy distribution functions (DFs)



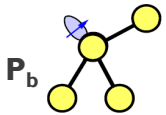
Example of DF vs x:

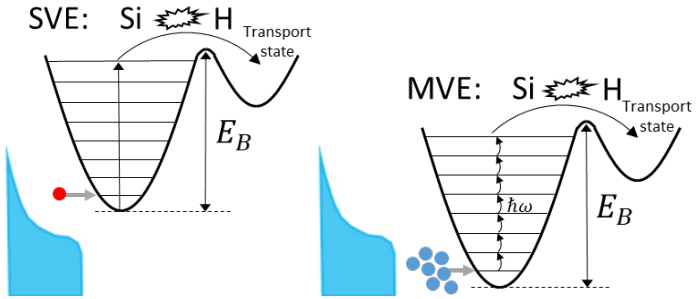


- Defects
  - **Thermalized ("BTI") and non-equilibrium ("hot") carrier trapping in bulk defects**



  - **<u>Generation of interface states</u>** (typical for HCD)





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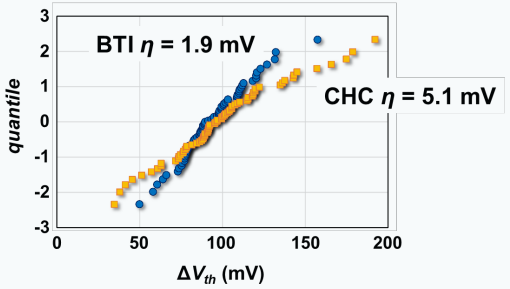
Example: TCAD Modeling of HCD variability

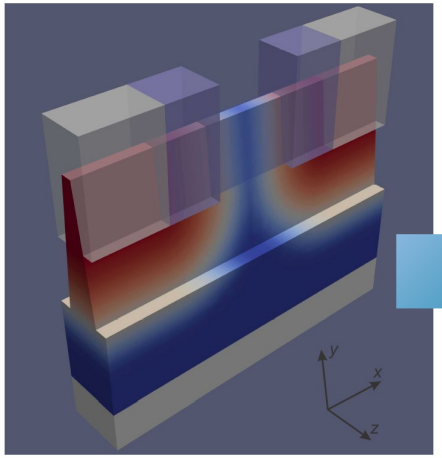
Kaczer *et al.*, IRPS 2015

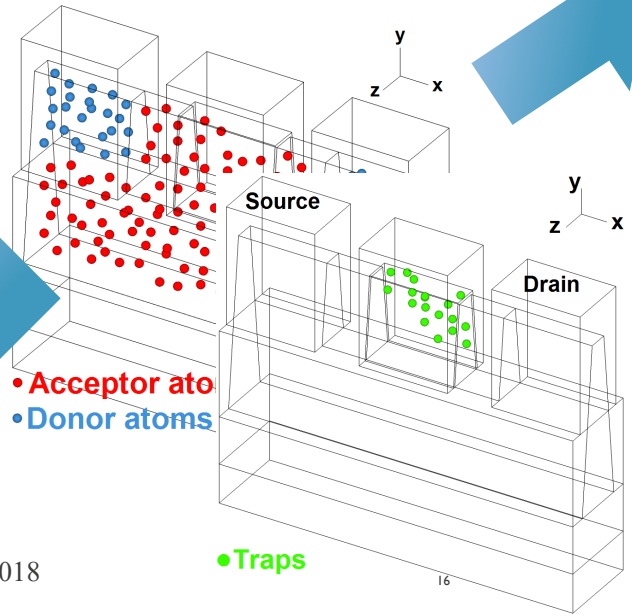


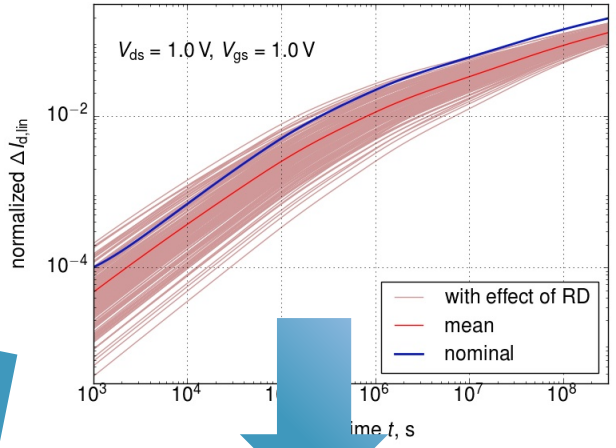
Calibrated model

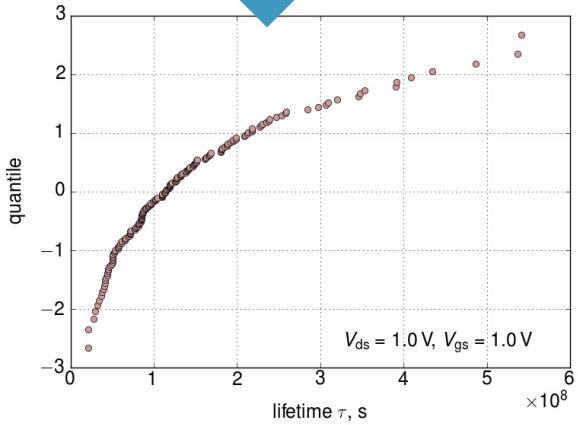
+ 200 FinFETs with individual random dopant configurations

x 100 different random traps configurations









(effect of RT var not shown for simplicity)

Tyaginov *et al.*, IEDM 2018

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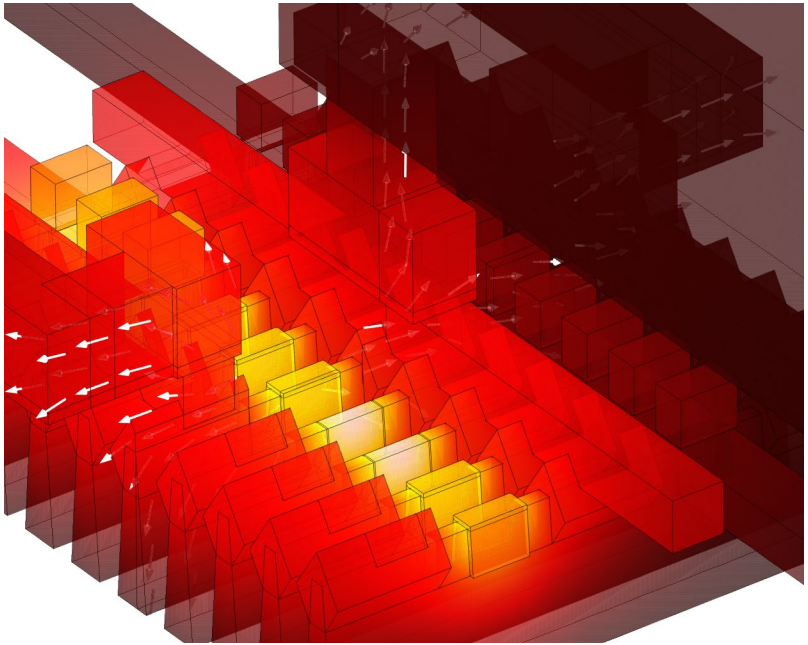
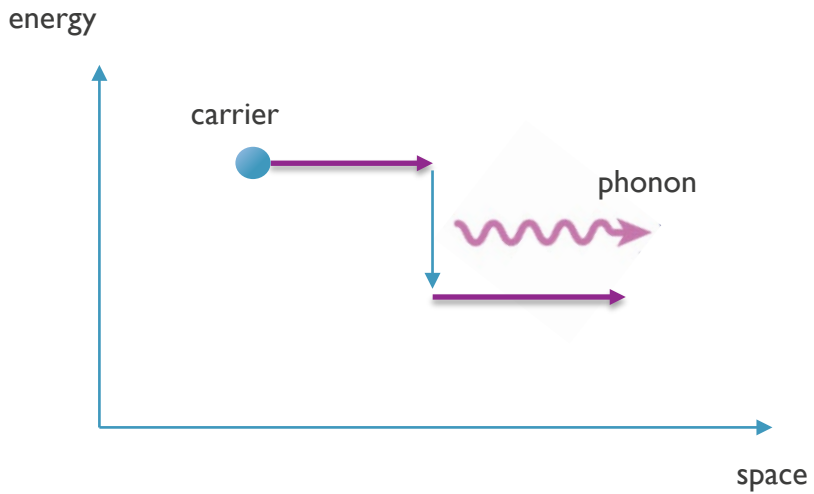
FET Self-Heating: increases temperature and typically accelerates degradation

"Macroscopic" (Fourier) picture



Bury et al., IRPS2014

Microscopic picture



- Carrier can also absorb phonon

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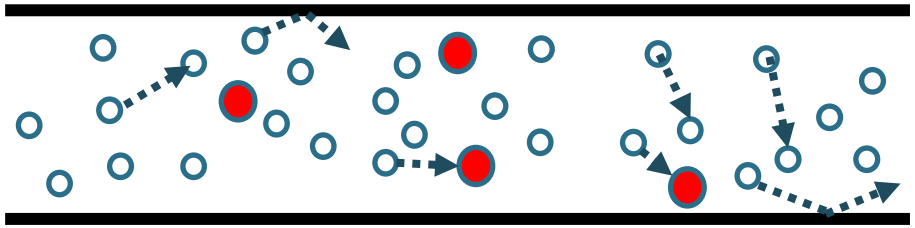
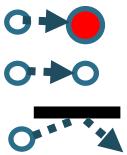
Origin of Fourier "breakdown": microscopic heat dynamics



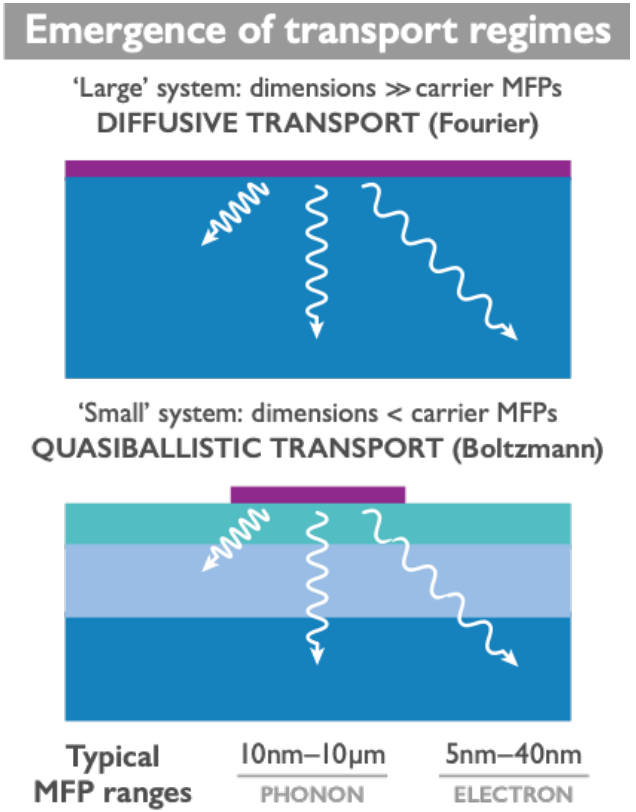


Phonon-impurity scattering

Phonon-phonon scattering

Phonon-boundary scattering

- Phonon-boundary scattering at narrow dimensions reduces mean free path
  → lower thermal conductivity for thin films
- Impurities or mass disorder enhance scattering
  → lower thermal conductivity for alloys
- Phonon-phonon scattering component
  → lower conductivity at elevated temperatures



imec

Graphics courtesy of E. Bury & B. Vermeersch

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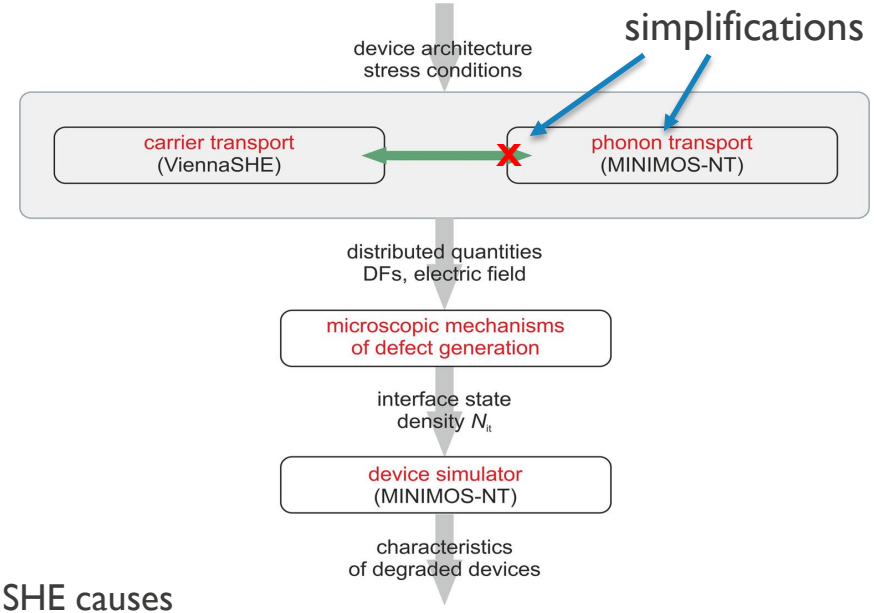
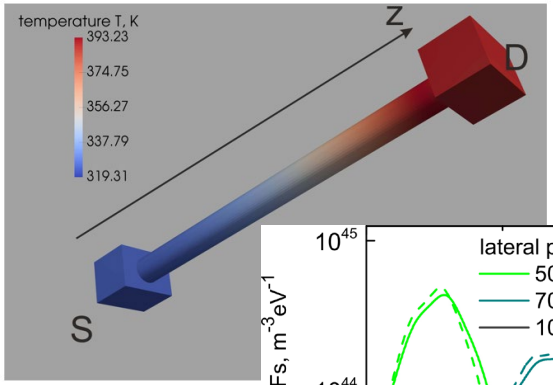
Example: Self-Heating + HCD TCAD

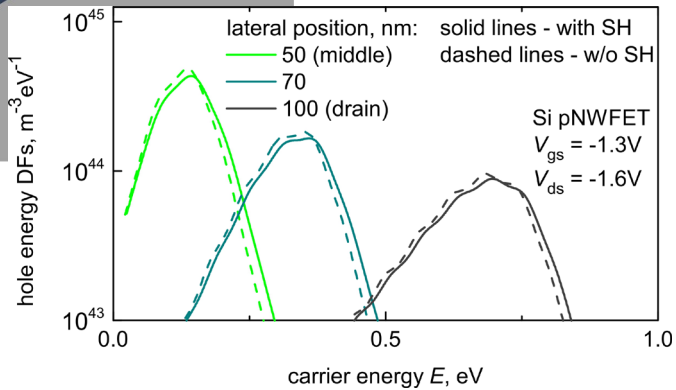


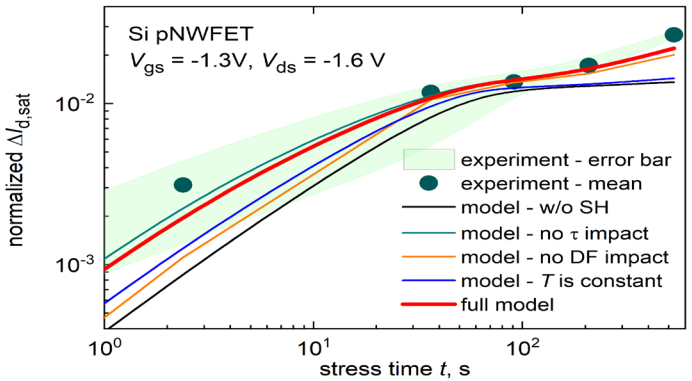
SHE causes

- perturbation of carrier transport
- acceleration of the thermal rate of bond-breakage
- shortening vibrational lifetime of the bond at higher T
  → reducing the MC-process rate

→ **Changes predictions at lower voltages**







Tyaginov *et al.*, IPFA 2020, MR 2021

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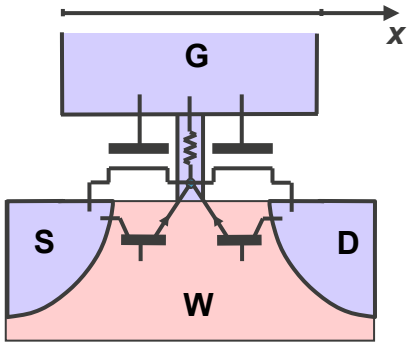
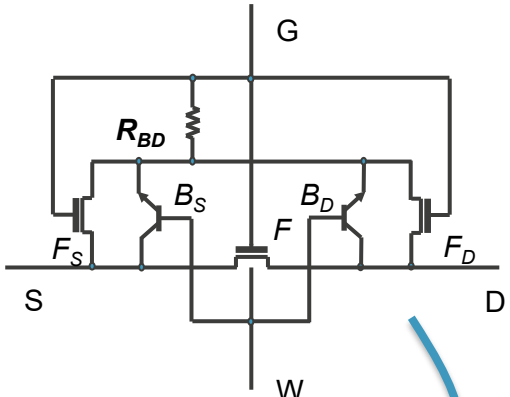
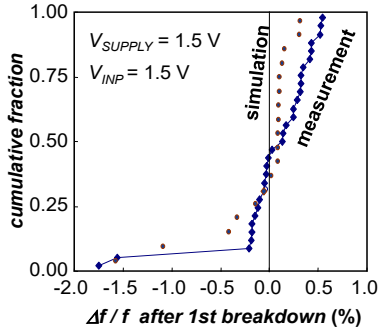
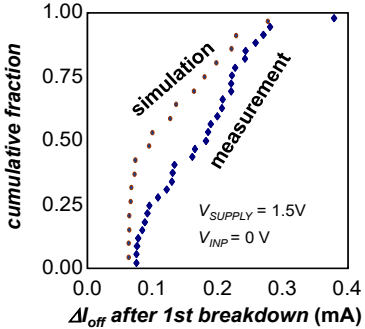
Time-Dependent Dielectric Breakdown (TDDB)

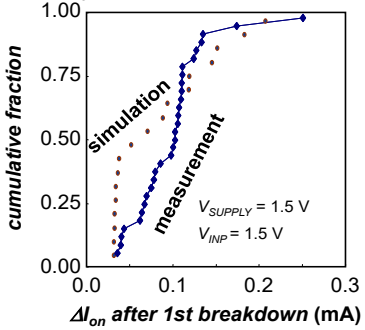
Example: equivalent lumped-element model for FET after BD





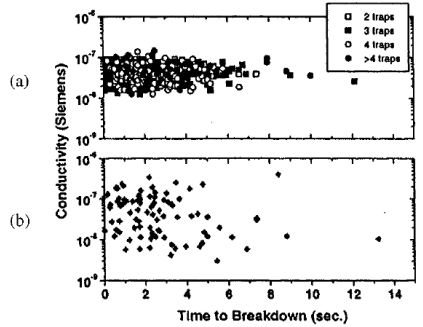




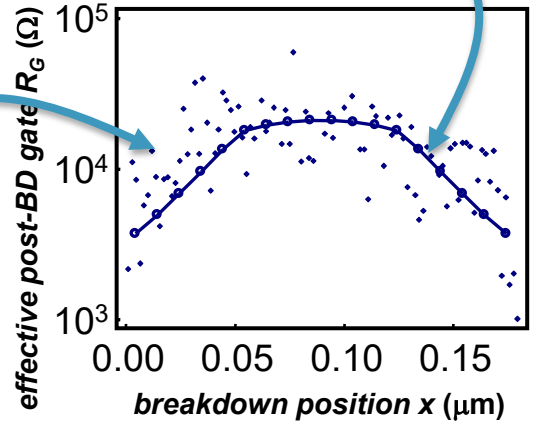


Ring Oscillator before and after breakdown

- Distribution BD magnitudes



Alam *et al.*, TED 2002



Kaczer *et al.*, TED 2001

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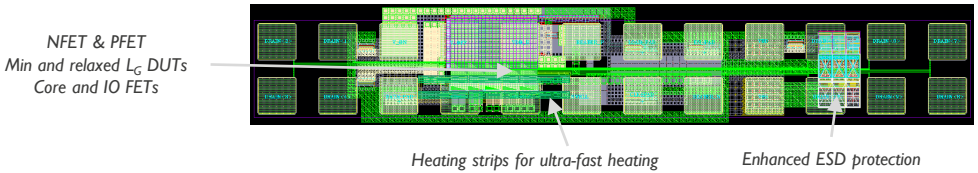
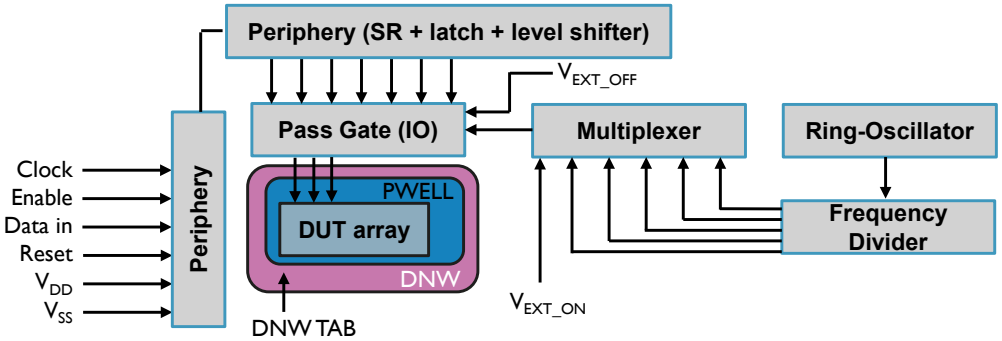
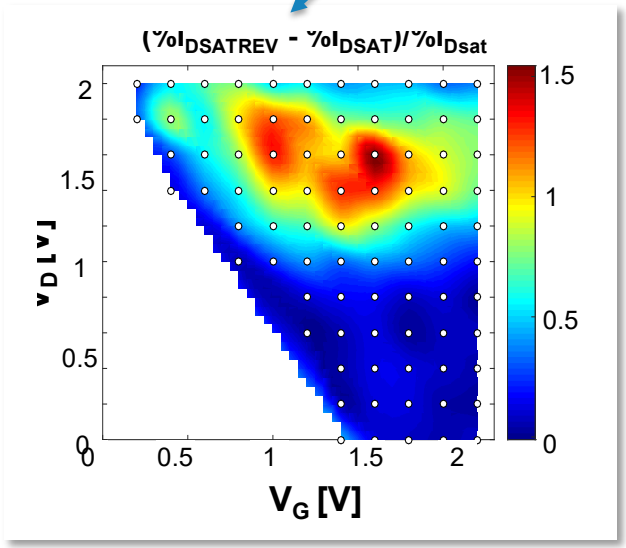
Technology degradation mapping with Smart Arrays



Courtesy: J. Diaz-Fortuny



Measure of degradation non-uniformity

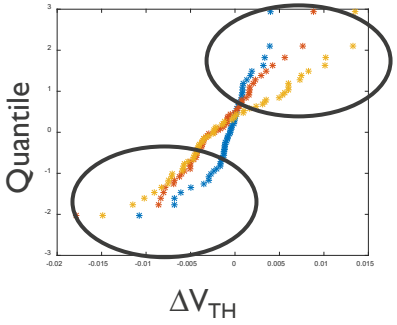


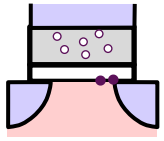
- FET degradation map provides information in ***all*** FET operating corners
- Based on large statistical dataset (median value depicted here)
- Application of degradation maps:
  - Fundamental understanding of underlying degradation mechanisms
  - Applied cases to maximize circuit performance and assess lifetime

E. Bury *et al.*: IRPS 2017

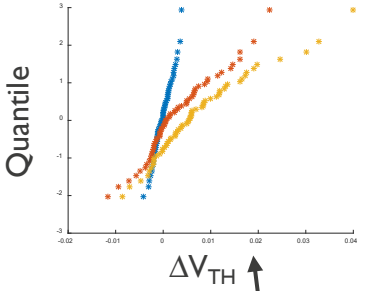
B. Kaczer *et al.*, "Toward reliability-aware physics-based FET compact models", MOS-AK workshop, Aug 11-13, 2021, Xi'an, China

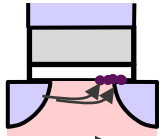
Measuring distributions allows deconvoluting degradation mechanisms





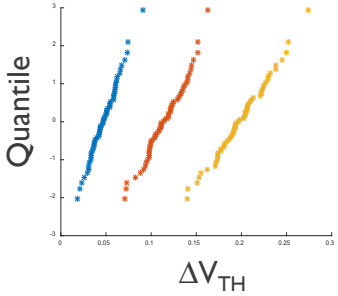
OSS

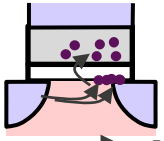




Hot carrier (SVE)

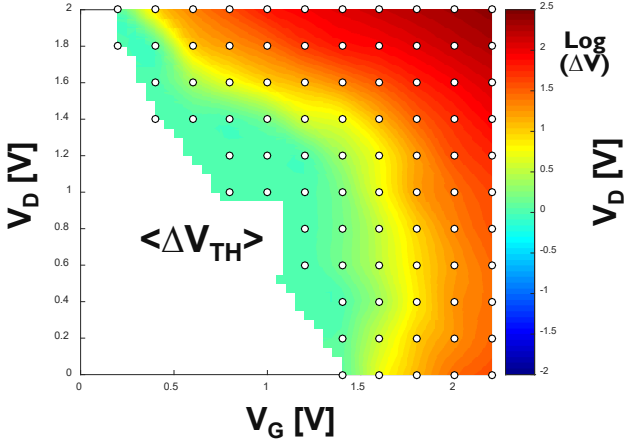
V_D

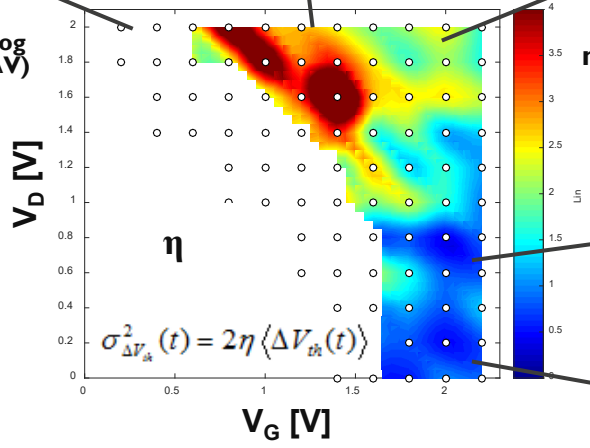


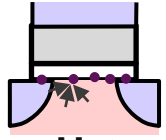


$N_{IT} + N_{OT}$ V_D

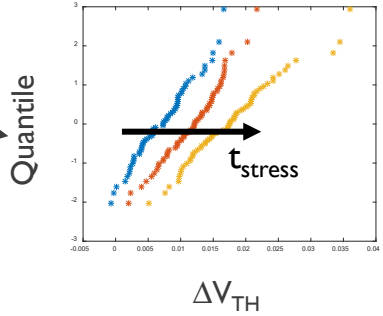
Mixed mode HCD

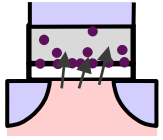






Hot carrier(MVE)





PBTI

- η related physical depth of the trapped charges related to deg
- I_{SAT} asymmetry related to lateral distribution of charge along channel

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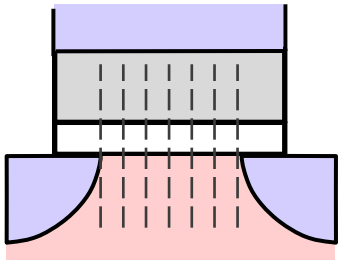
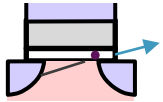
Determining horizontal and vertical location of traps

Horizontal trap localization

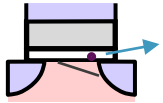
➔ $I_{d,sat}$ *compared to* $I_{d,sat_reverse}$





$I_{D,SAT}$: sensitive near **source**

charge at drain has **no impact**

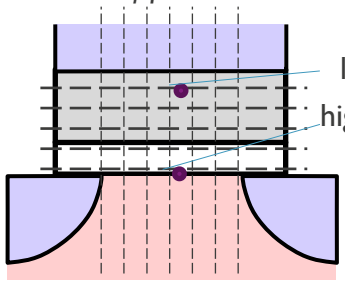


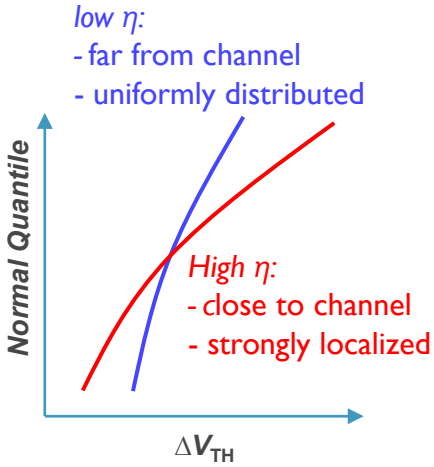
I_{D,SAT_REV}: sensitive near **drain**

charge at drain has **impact**

Vertical trap localization

➔ η *parameter*





- Horizontal trap localization by comparing forward and reverse saturation degradation:

$$\frac{\langle \%I_{D,SAT} \rangle - \langle \%I_{D,SAT_REV} \rangle}{\langle \%I_{D,SAT} \rangle}$$

- Vertical trap localization (+ horizontal) by studying variability: $\eta = \frac{\sigma^2_{\Delta V_{th}}}{2\langle \Delta V_{th} \rangle}$

E. Bury *et al.*: IRPS 2019

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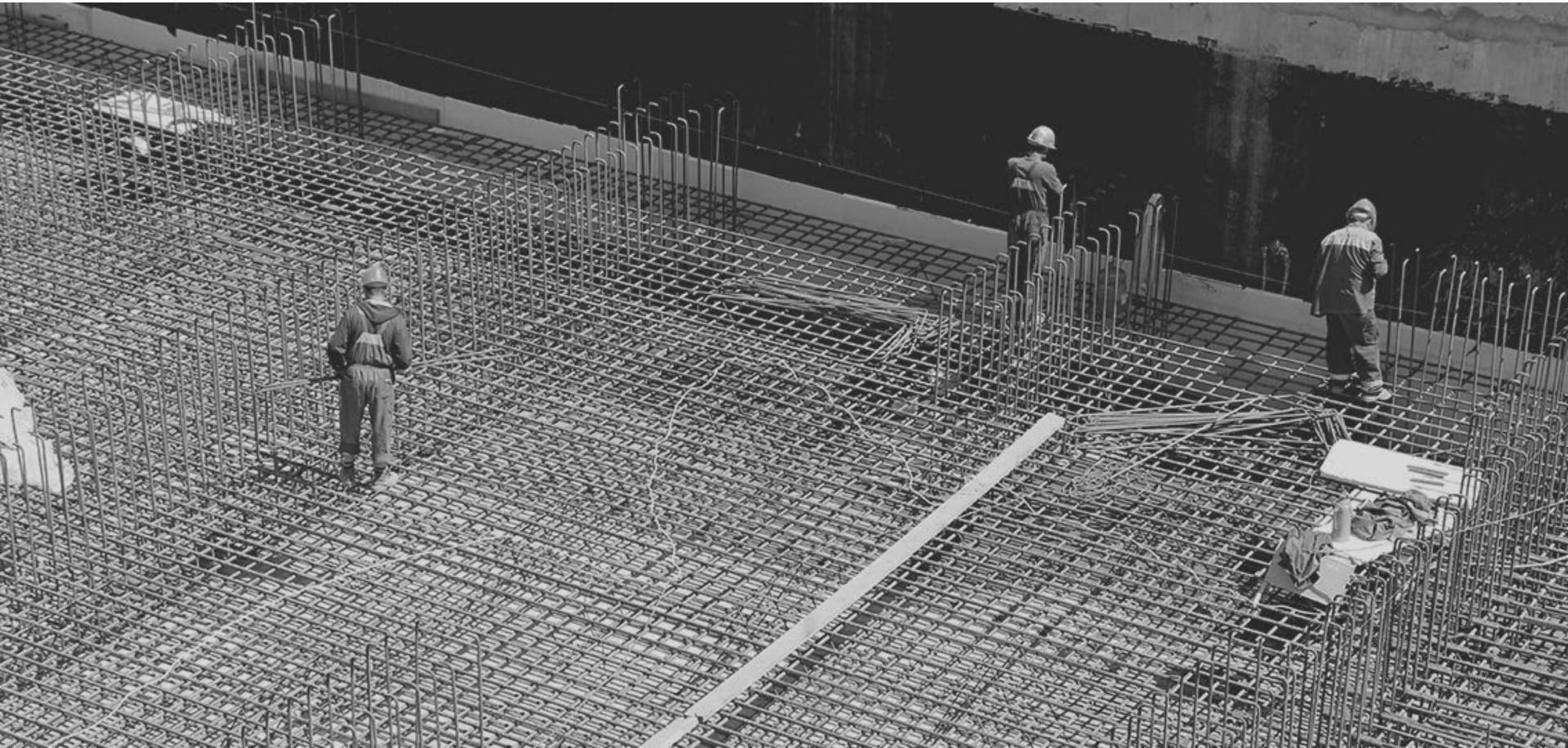
Toward Rel-Aware CM: Building on solid foundations



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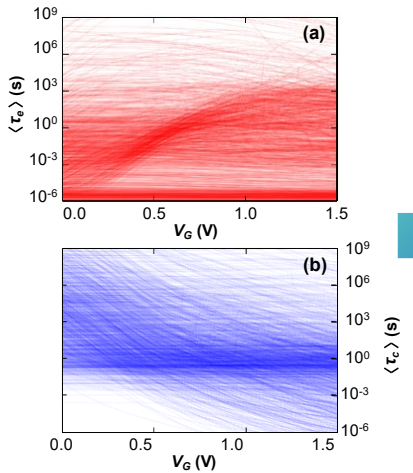
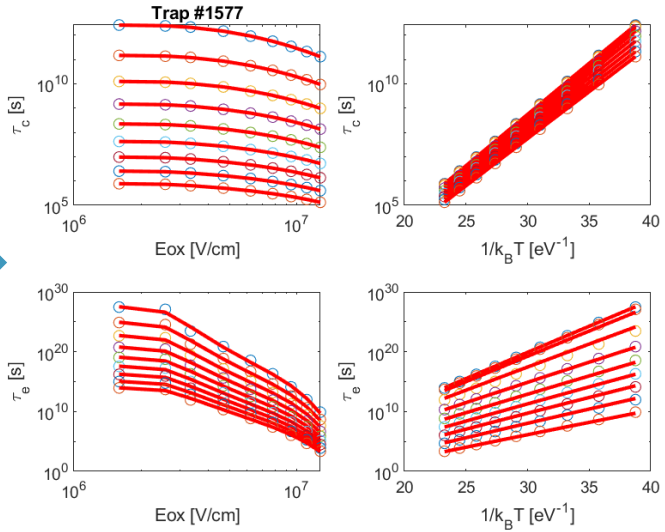
Exporting Comphy traps to circuit simulations



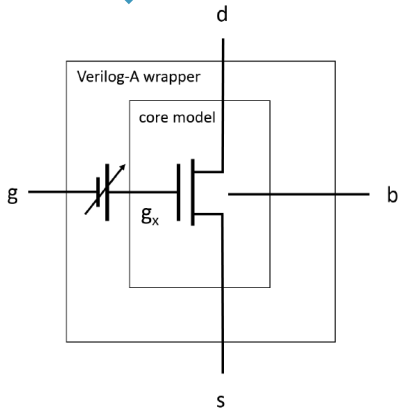


$$F(X,Y) = P_1 X^N Y^M + P_2 X^{N-1} Y^M + \cdots + P_{N+1} Y^M + P_{N+2} X^N Y^{M-1} + P_{N+3} X^{N-1} Y^{M-1} + \cdots + P_{2(N+1)} Y^{M-1} + \cdots + P_{M(N+1)+1} X^N + P_{M(N+1)+2} X^{N-1} + \cdots + P_{(N+1)(M+1)}$$

$$X = \log_{10}(E_{ox})$$

$$Y = {}^{1}/_{k_B T}$$

$N=4$ and $M=2$



- Comphy extracts from measurements time constants for large number of traps (10k) at different bias conditions and temperatures
- Polynomial functions are fitted to describe the trap behavior
- Polynome constants ported to Verilog-A wrapper, calculates trap occupancy and contribution to V_{th} shift

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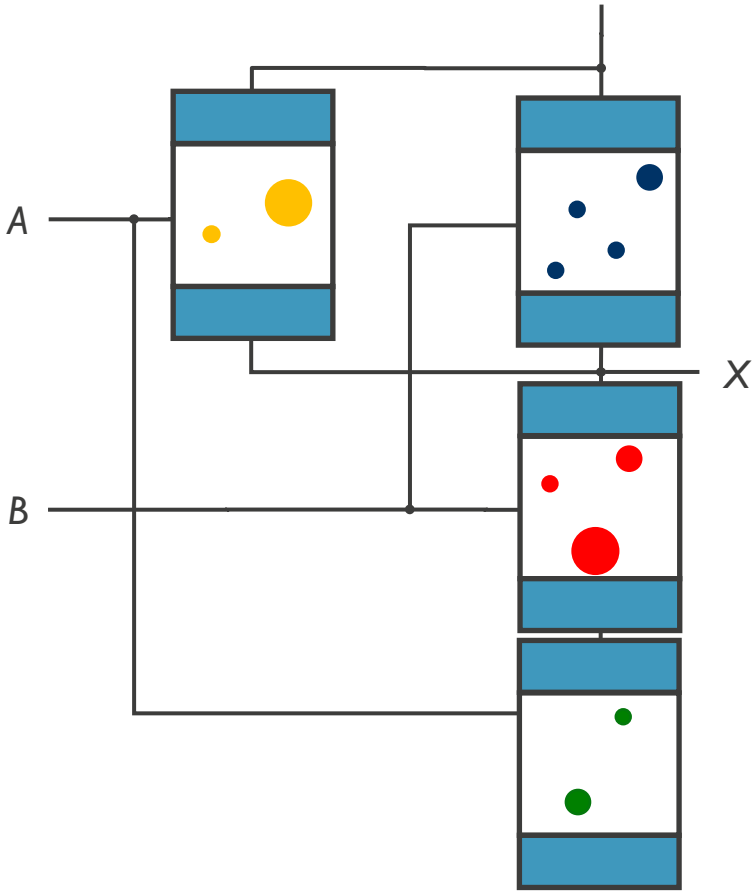
FETs in circuit netlist instantiated with individual traps



Kaczer *et al.*, IRPS 2011

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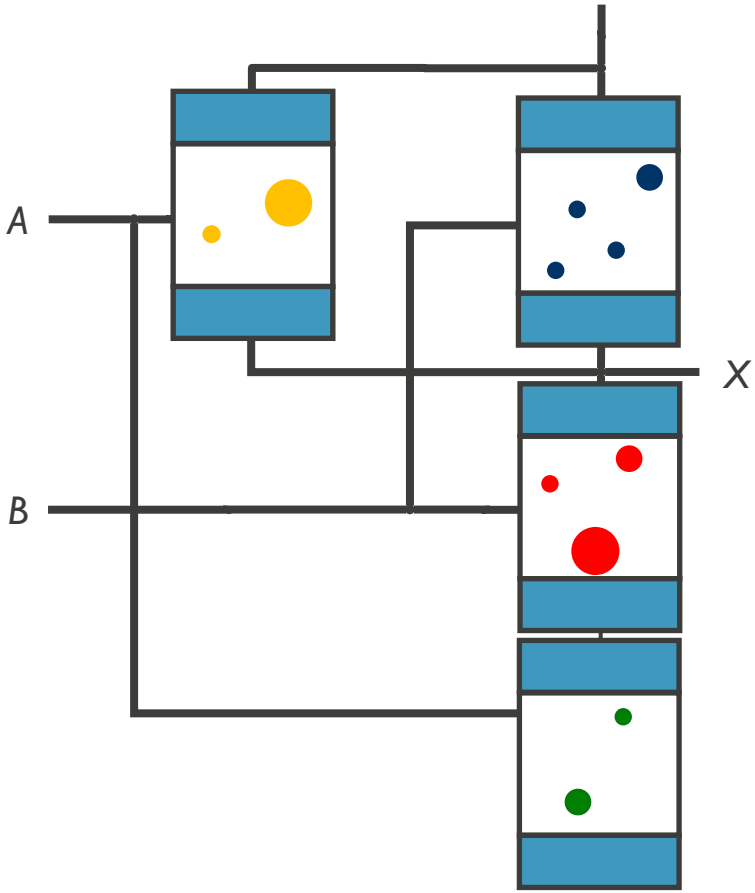
The circuit is solved with individual defect properties



Kaczer *et al.,* IRPS 2011

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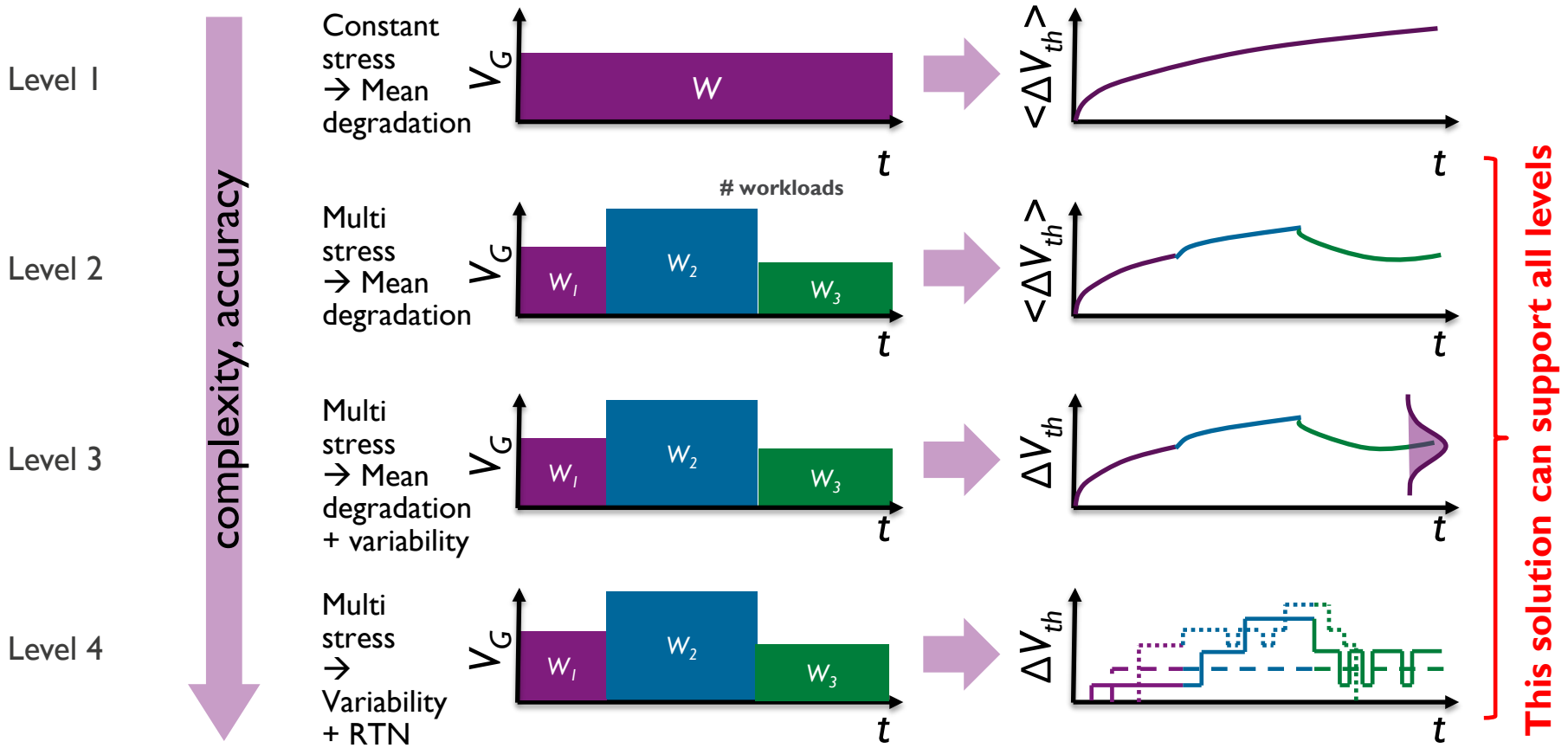
Different ways to introduce BTI degradation into Compact models



B. Kaczer *et al.*, SSE 2016

B. Kaczer *et al.*, "Toward reliability-aware physics-based FET compact models", MOS-AK workshop, Aug 11-13, 2021, Xi'an, China

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Cornerstone 1: Analytical description of charrier energy distribution functions (DF)

$$f(\varepsilon) = A\exp\left[-\left(\frac{\varepsilon}{E_{\mathrm{ref}}}\right)^{\mathrm{b}}\right] + C\exp\left[-\frac{\varepsilon}{k_{\mathrm{B}}T_{\mathrm{L}}}\right]$$

hot carriers — thermalized carriers

With the weight factors *A*, *C* and the reference energy E_{ref} from:

$\int_0^\infty f(\varepsilon)g(\varepsilon)\mathrm{d}\varepsilon = n$ (carrier concentration)

$\int_0^\infty \varepsilon f(\varepsilon)g(\varepsilon)\mathrm{d}\varepsilon = \frac{3}{2}nk_{\mathrm{B}}T_{\mathrm{n}}$ (local carrier tempearture)

$\frac{3}{5}\frac{\langle\varepsilon^2\rangle}{\langle\varepsilon\rangle^2} = \frac{3}{5}\frac{n\int_0^\infty \varepsilon^2 f(\varepsilon)g(\varepsilon)\mathrm{d}\varepsilon}{\left(\int_0^\infty \varepsilon f(\varepsilon)g(\varepsilon)\mathrm{d}\varepsilon\right)^2} = \beta_{\mathrm{k}}$ (kurtosis)

$g(\varepsilon) = g_0\sqrt{\varepsilon}(1 + \eta\varepsilon)$ (density-of-states) η = 1.404eV^{-1} – nonparabolicity factor

T. Grasser *et al.*, JAP, 91, p. 3869, 2002

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Cornerstone 1 (continued)

Carrier temperature T_n

$$T_n = T_L + \frac{2}{3}\frac{q}{k_B}\tau\mu F^2$$

T_L – lattice temperature, τ – relaxation time, μ – mobility, F – electric field

Kurtosis β_k in source/channel by empirical formula

based on a full BTE solution

$$\beta_k(T_n) = \frac{T_L^2}{T_n^2} + \left[x_0 + x_1\left(1 - \exp\left[-x_2\frac{T_L}{T_n}\right]\right)\right]\left(1 - \frac{T_L}{T_n}\right)$$

$x_0 = 0.69$, $x_1 = 1.34$, $x_2 = 1.89$ – fitting parameters

Kurtosis in the drain: $\beta_k = 2$

Simulations of pristine devices are needed for carrier transport

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Cornerstone 2: Simplified electrostatics treatment in the lateral direction

- Device laterally divided into (small # of) slices

For each slice with index *i*

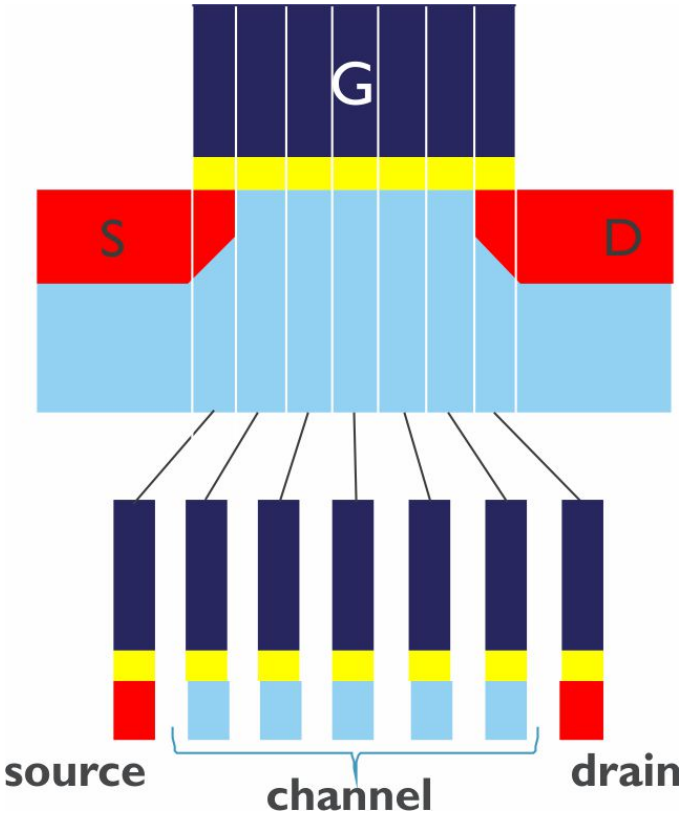
doping concentration $N_{D,i} \rightarrow$ resistivity ρ_i

potential drop: $V_{ds,i} = V_{ds} \cdot \rho_i / \sum \rho_i$

obtain local electric field F_i

make corrections to the local gate voltage:

$V_{gs,i} \rightarrow V_{gs,i} - V_{ds,i}$



S. Tyaginov *et al.*, IRPS 2020

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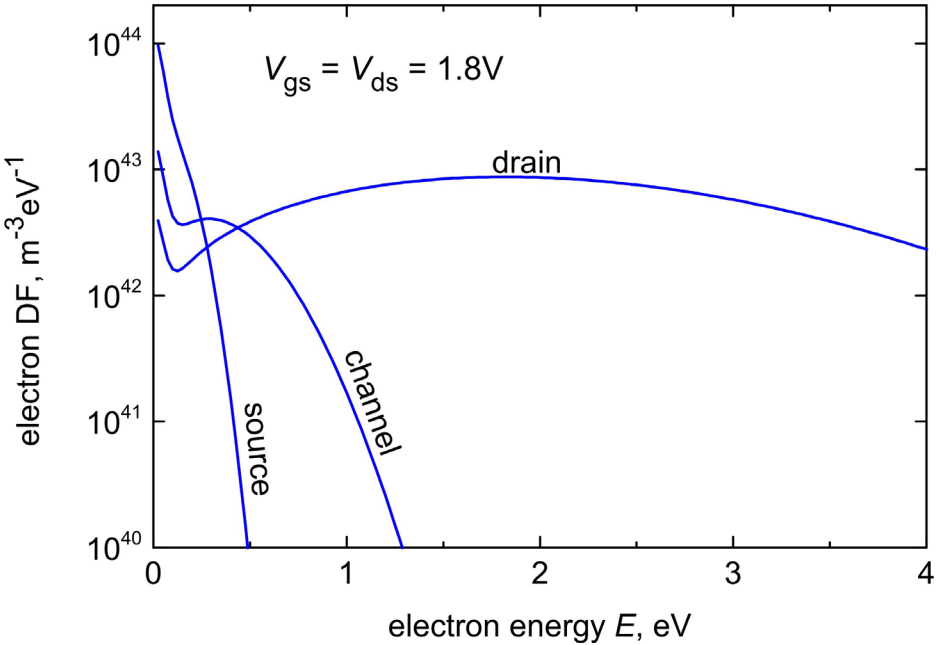
Analytical carrier DF's in all channel slices obtained



- Source: DFs are Maxwellian
- Channel/drain: DFs are non-equilibrium

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Cornerstone 3: Analytical description of (D_{it}) defect generation

- Single- and multiple-carrier mechanisms of Si-H dissociation

Rates of SC- and MC-mechanisms:

$$I_{\mathrm{SC/MC}} = \int_0^{\infty} f(E)\, g(E) v(E) \sigma_0 (E - E_{th})^p \mathrm{d}E$$

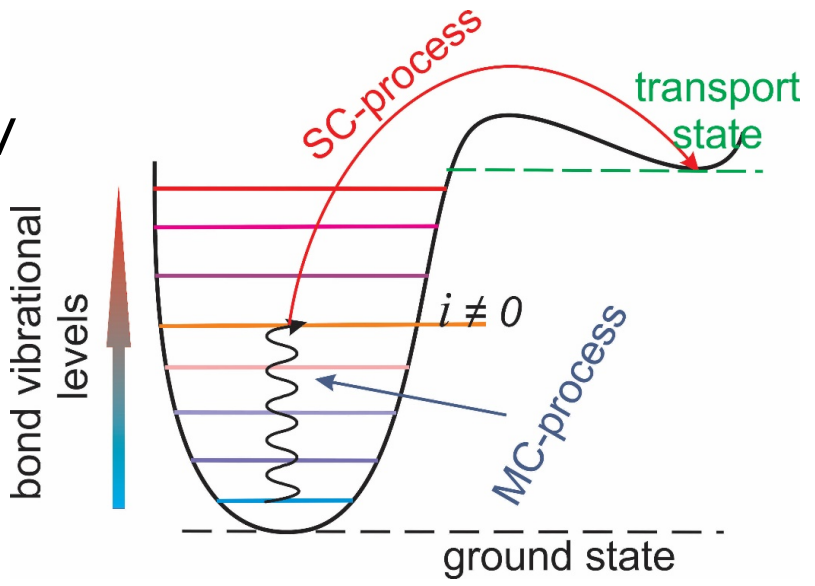
SC-mechanism: $p_{\mathrm{SC}} = 11, E_{\mathrm{th}} = E_{\mathrm{a}} = 2.56\mathrm{eV}$

MC-mechanism: $p_{\mathrm{MC}} = 1, E_{\mathrm{th}} = \hbar\omega = 0.25\mathrm{eV}$

Rates $I_{\mathrm{SC/MC}}$ can be expressed by

combination of Γ-functions

= analytical expression



S. Tyaginov *et al.*, SISPAD 2014, p. 89 S. Tyaginov *et al.*, IEEE EDL, v. 37, p. 84, 2016

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Cornerstone 3 (continued)

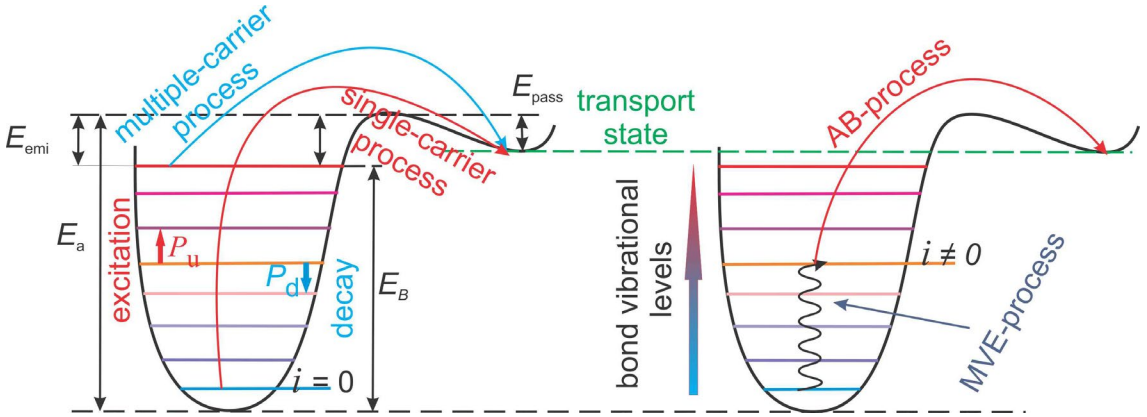
- Interface state density N_{it}

  Described by analytical expressions

$$N_{\mathrm{it}} = \frac{1}{2\tau \boldsymbol{P}} \frac{1 - f(t)}{1 + f(t)} - \frac{\boldsymbol{R}}{\boldsymbol{P}}$$

$$f(t) = \frac{1 - \tau \boldsymbol{R}}{1 + \tau \boldsymbol{R}} \exp\left(-\frac{t}{\tau}\right)$$

$$\frac{1}{\tau} = 2\sqrt{\boldsymbol{R}^2/4 + N_0 \boldsymbol{R} \boldsymbol{P}}$$



Cumulative rate from all levels: $\boldsymbol{R} = \frac{1}{k} \sum R_{\mathrm{a},i} \left(\frac{P_{\mathrm{u}}}{P_{\mathrm{d}}}\right)^i$

$R_{\mathrm{SC},i} = w_{\mathrm{th}} \exp\left[-\frac{E_a - E_i}{k_{\mathrm{B}} T}\right] + I_{\mathrm{SC},i}$ (Arrhenius and hot-carrier terms)

S. Tyaginov *et al.*, SISPAD 2014, p. 89 S. Tyaginov *et al.*, IEEE EDL, v. 37, p. 84, 2016

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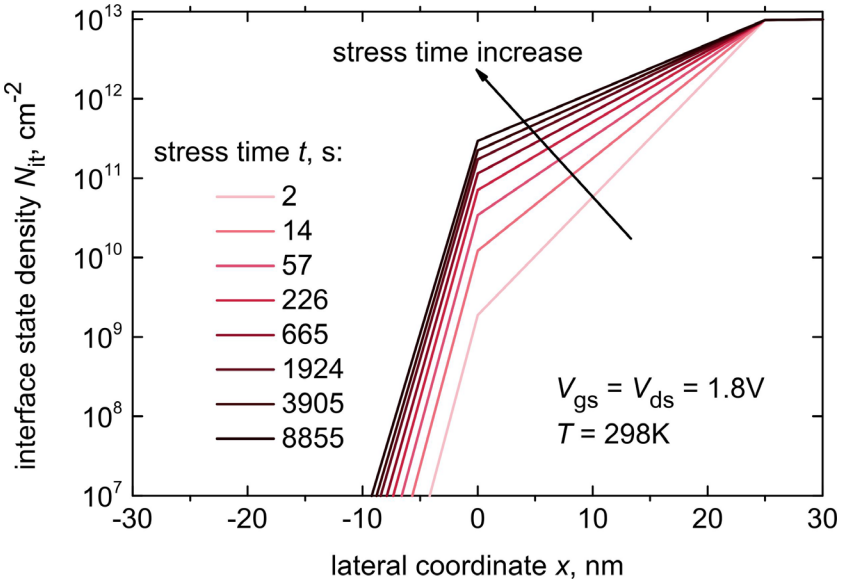
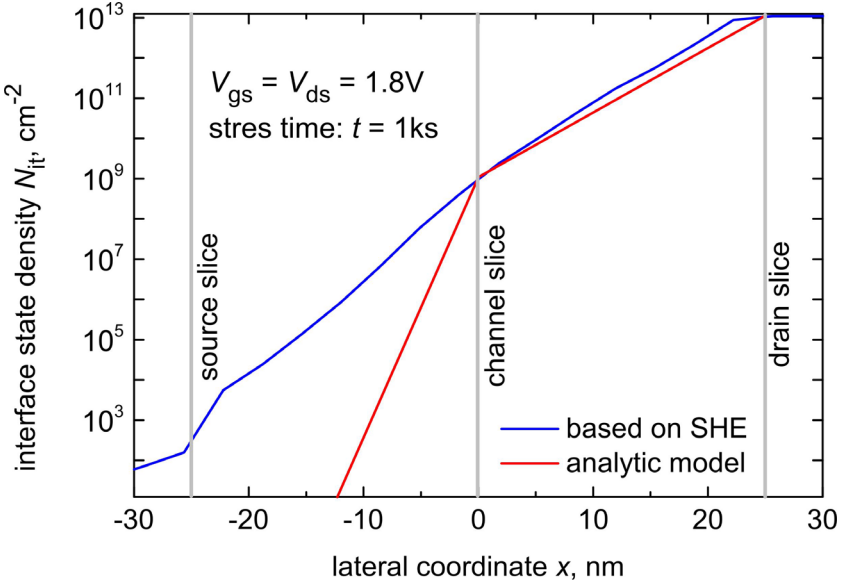
Defect generation along the channel

- Interface state density N_{it}
  - Example: 3 slices (source, channel, drain)
  - Good agreement with full TCAD model



S. Tyaginov *et al.*, IRPS 2020



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Cornerstone 4: Impact of traps on FET characteristics

- Impacts on electrostatics and mobility

$I_{\mathrm{d}} = \sigma V_{ds}$ σ – conductivity

$\Delta I_{\mathrm{d}} = \Delta(\sigma) V_{\mathrm{ds}}$

$$\sigma = \left[\sum_i \frac{1}{\sigma_i}\right]^{-1} = \left[\sum_i \frac{1}{q n_i \mu_i}\right]^{-1}$$

n_i and μ_i are carrier concentration and mobility in slice *i*

$$\Delta I_{\mathrm{d}} = \Delta\left(\left[\sum_i \frac{1}{q n_i \mu_i}\right]^{-1}\right) V_{\mathrm{ds}}$$

perturbation in n_i calculated with Pregaldiny model, $\delta V_{gs,i} = N_{it,i}/C_{ox}$

- Mobility degradation model

$$\mu_{\mathrm{degr}} = \frac{\mu_{\mathrm{fresh}}}{(1 + \alpha N_{\mathrm{it}})}$$

μ_{degr} – mobility of degraded device

μ_{fresh} – mobility of pristine device

$\alpha = 10^{-13}\mathrm{cm}^2$ is fitting parameter

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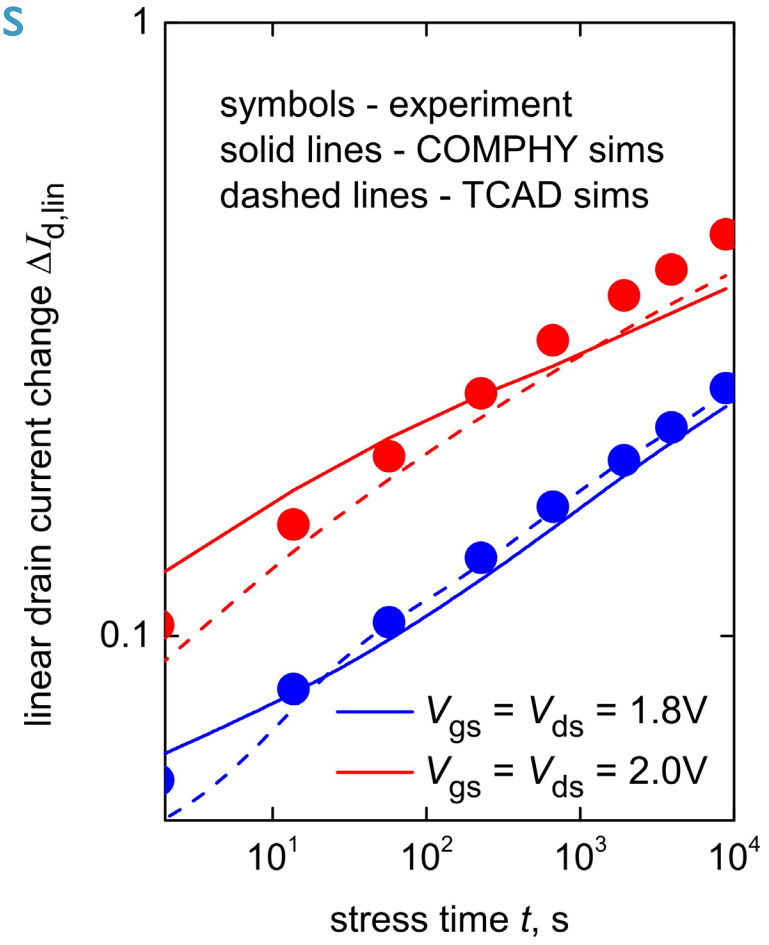
End result: Modeling of degraded devices

- $\Delta I_{d,lin}(t)$ degradation traces
  - good agreement
    - with experimental data
    - with the "full" TCAD model
  - Increased number of slices needed
    - improve model accuracy
    - obtain better time dependence



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Outline

- Introduction
- Degradation mechanisms basics
  - Bias Temperature Instability (BTI) and Compact Physical (Comphy) model for trapping
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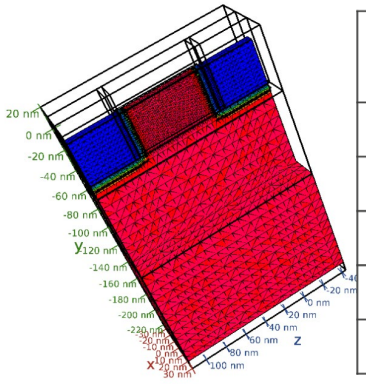
Simplified-EKV + analytical solution for lateral carrier density

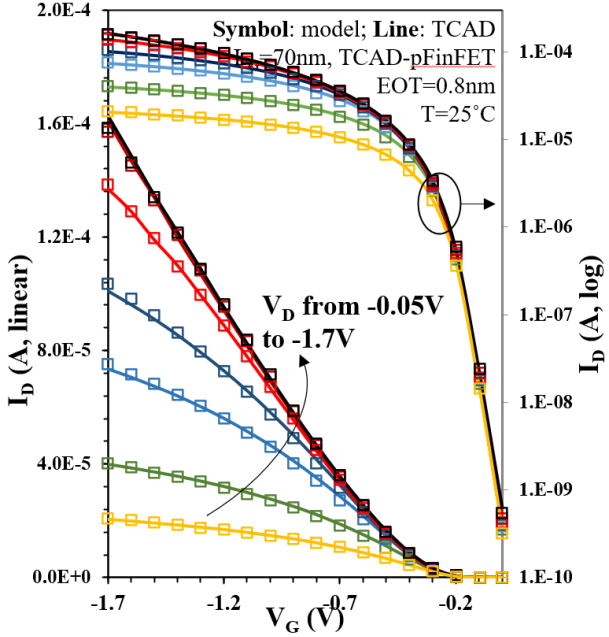
$$\xi = x/L$$

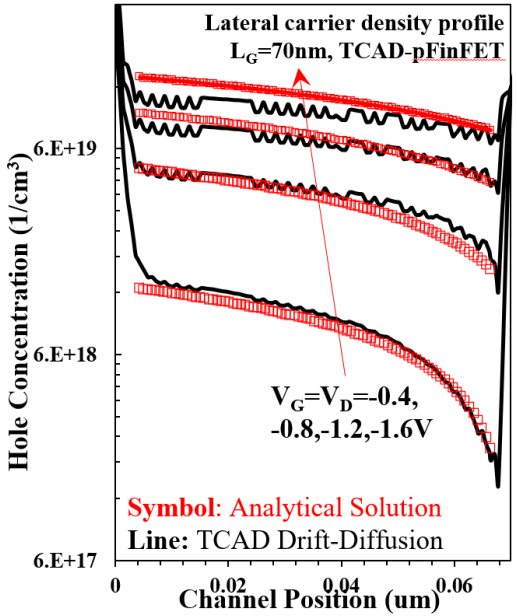
$$Q_i(\xi) = 2 \cdot NIDE \cdot \phi_t \cdot C_{ox} \cdot \sqrt{q_s^2 - IC \cdot \xi}$$

TCAD FET for benchmarking



Hydro-dynamic or Drift-Diffusion	
$L_{G,phy}$	70nm
Fin-Width	7nm
Fin-Height	36nm
EOT	0.9nm
$R_{S/D}$	700Ω





- Carrier density + Poisson Equation → lateral potential profile

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Channel slicing from Lin to Sat regimes: A DD FET from a series of ballistic FETs

Physics-Based Compact Model of Nanoscale MOSFETs—Part I: Transition From Drift-Diffusion to Ballistic Transport

Giorgio Mugnaini and Giuseppe Iannaccone, *Member, IEEE*

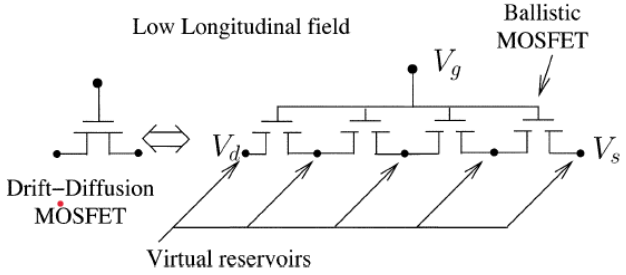

Fig. 2. Long chain of B MOSFETs. The contacts act as thermalizing reservoir. We also show the symbol we use for a B MOSFET in the following figures.

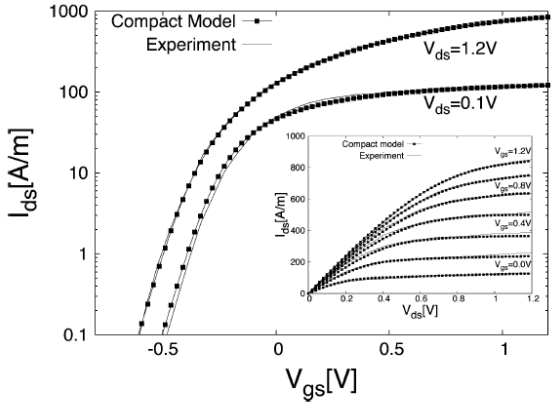

Fig. 9. Comparison between the transfer characteristics obtained from experiments on a FinFET with $L = 80$ nm reported in [33] and from a compact model fitted to the data. The comparison of output characteristics is illustrated in the inset.

Lambert-W function

$$I_{ds} = \frac{\lambda}{2\phi_t} v_{th} Q_n \mathcal{W}\left(e^{\frac{V_g - V_{Fn} - V_T}{\phi_t}}\right) \frac{dV_{Fn}}{dx}$$

$$Q_m = Q_n \mathcal{W}\left[e^{\frac{V_g - V_{Fn} - V_T}{\phi_t}}\right]$$

Potential slope (single value)

$$I_{ds} L = \mu_{no} \int_0^L Q_m \frac{dV_{Fn}}{dx} dx = \mu_n \int_{V_s}^{V_d} Q_m dV_{Fn}.$$

$$\int \mathcal{W}(e^x) dx = \frac{\mathcal{W}^2(e^x)}{2} + \mathcal{W}(e^x)$$

$$I_{ds} = \frac{\mu_{no} Q_n \phi_t}{L} \left[\frac{Q_{ms}^2 - Q_{md}^2}{2Q_n^2} + \frac{Q_{ms} - Q_{md}}{Q_n}\right]$$

- The main requirement is the "local" potential continuity at each "virtual reservoir"

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Impact of D_{it} and N_{ot} on individual slice

Mobility degradation

$$\mu_c = \frac{\mu_{ph,sr}}{1 + \frac{\mu_{ph,sr}}{\mu_{coulo,deg}}} \Rightarrow \mu_{coulo,deg} = \frac{\mu_{coulo,0}}{1 + \alpha D_{it}}$$

$$v_d = \frac{\mu_c F}{[1 + (\frac{\mu_c F}{v_{sat}})^{\gamma}]^{1/\gamma}}$$

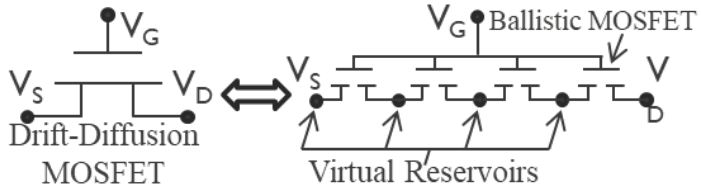
Carrier loss

$$V_{th,deg} = V_{th,0} + dV_{th,N_{ot}} + dV_{th,D_{it}}$$

$$n_{idea,deg} = n_{ide,0} + n_{Dit}$$

$$q_s = \frac{1}{2} lambertw\left(2\, exp\left(\frac{V'_{gs} - V_{th,deg}}{n_{idea,deg} \cdot ut}\right)\right)$$

- Carrier density/velocity, lateral/oxide field are considered constant within each slice:
  - For long channel device, large slicing number can be mitigated by non-uniform slicing and weighting
  - The full I-V (from linear to saturation) is captured by modelling the mobility degradation and carrier loss only
- The degraded individual slice is concatenated with Perturbation based "current sensitivity model"



Current Sensitivity Model

$$I = \frac{W_G}{\frac{1}{a_1 n_{inv,1} v_1} + \frac{1}{a_2 n_{inv,2} v_2} + \cdots + \frac{1}{a_N n_{inv,N} v_N}}$$

$$a_N = \frac{1}{N_{slice}} \; for\ uniform\ slicing$$

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Lin and Sat degraded IV's excellently reproduced

- Reminder:

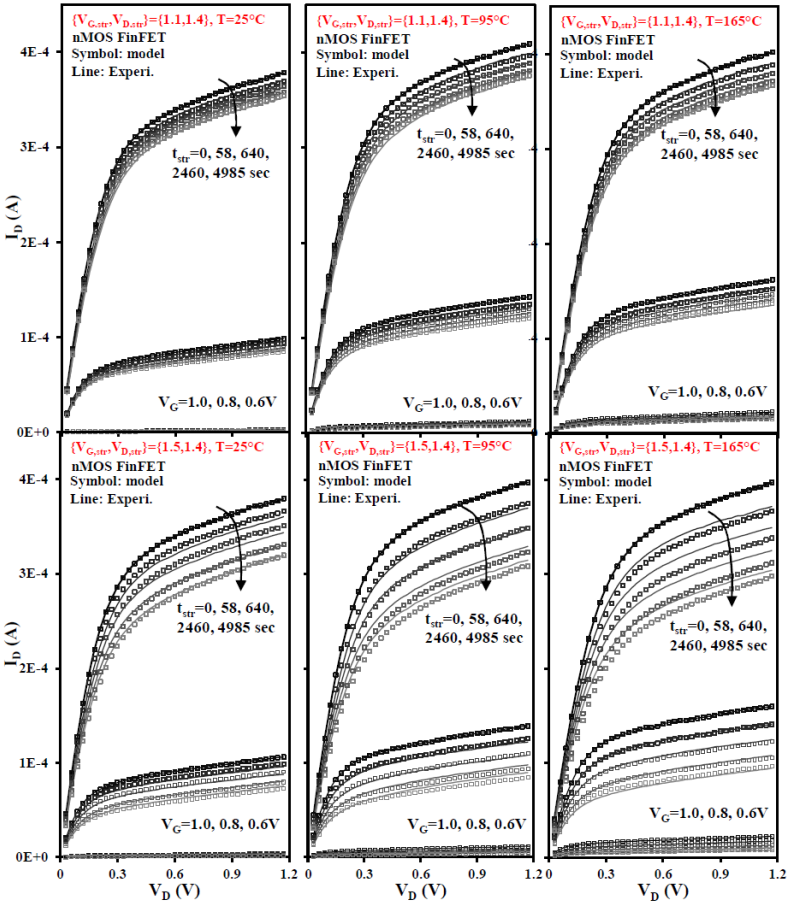
1. *Device description*: I-V compact model and analytical lateral profiling

2. *Distribution function*: lateral field extraction and analytical form of EDF

3. *Local degradation*: 2-state NMP, SVE and MVE models

4. *Degraded device characteristics*: current sensitivity model for concatenating slices

5. *Results interpretation*: I-V modelling results and degradation components separation



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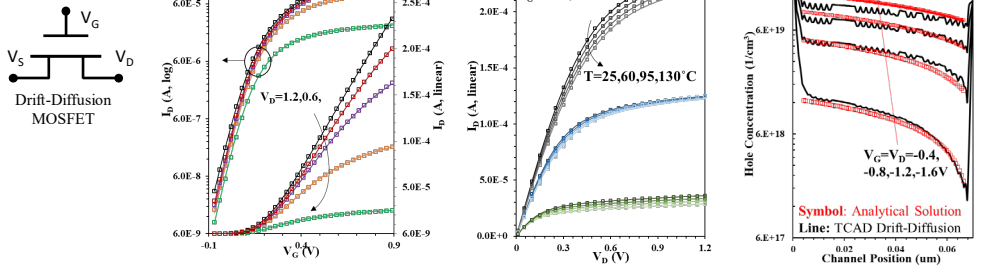
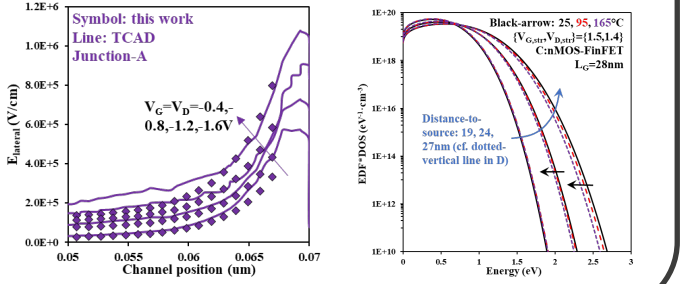
Summary: Enhanced aging modeling framework for reliability analysis

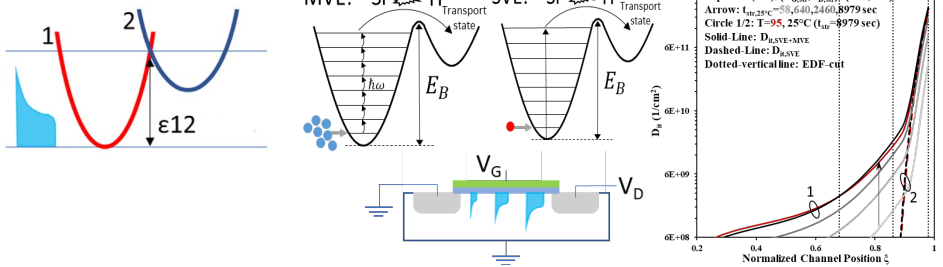
1. Time-0 I-V Compact Model and analytical carrier lateral profile



2. Lateral Poisson eq. and analytical EDF



3. Physical modeling of charge trapping, SVE, MVE per slice



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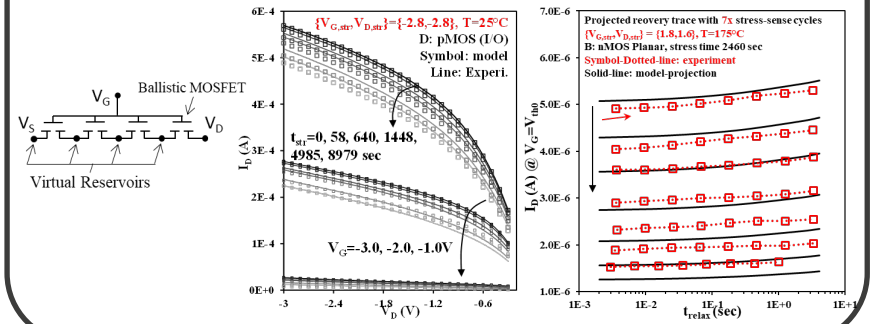
4. Current sensitivity model for concatenated slices



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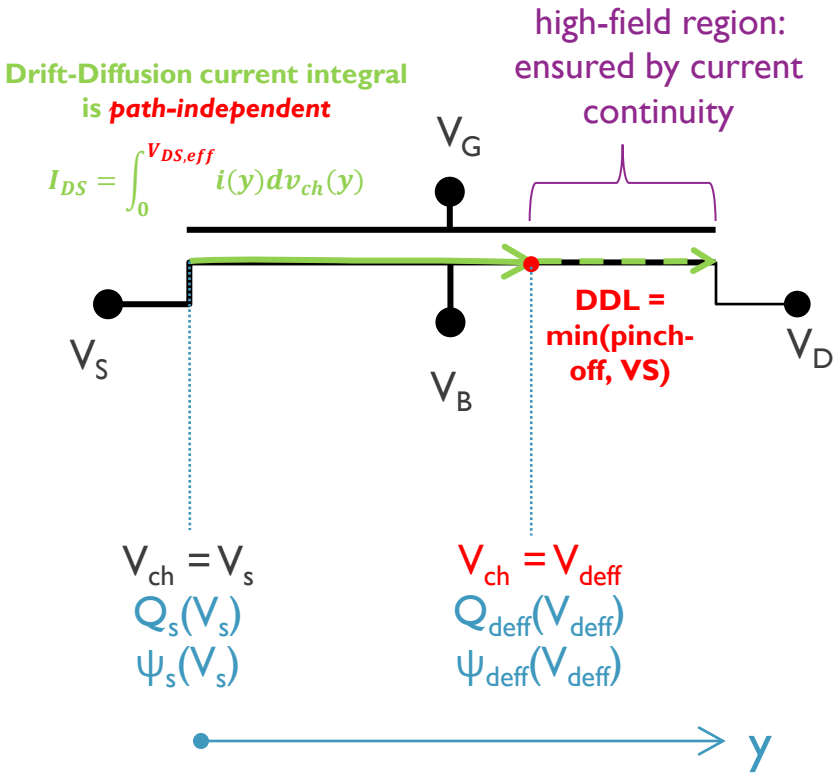
BSIM assumptions and available parts in core equations



What are available in BSIM?

- **Core electrostatics** = *one-dimensional* electrostatics: V_{ch} → $\psi(V_{ch})$, $Q(V_{ch})$, where $V_{ch} \in [V_S, V_D]$
- **Core transport**: from source to drift-diffusion current integral limit ("DDL"), clipped at velocity saturation / pinch-off
- **DDL y-coordinate** is NOT available: current integral is "path-independent", spatial coordinates not needed

→ $n_{car}(y)$ available from $Q(V_{ch})$, but y not !

→ $E_y(y)$ unavailable

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[1] BSIM-BULK106.2.0 Technical Manual
[2] BSIM-CMG 110.0.0 Technical Manual

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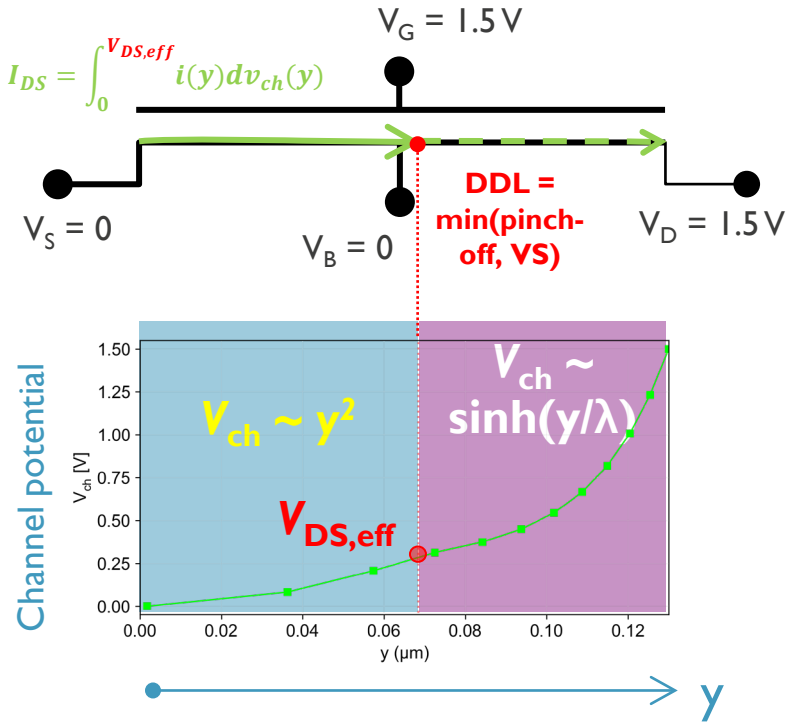
Lateral field reconstruction from available parts

"Patch" for *y* and E_y inspired by substrate-current-induced body effect



[1] BSIM-BULK106.2.0 Technical Manual

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- Bias-dependent $V_{DS,eff}$ generated by **core *I-V*** :

$$V_{DS,eff} = \min(V_{DS,sat}, V_{DS,velsat})$$

- $V_{ch}(y)$ for y > DDL from **SCBE**

$$V_{ch}(y) = V_{DS,eff} + 2\delta \sinh\left(\frac{y - DDL}{\lambda}\right)$$

- Assume parabolic potential for y < DDL

$$V_{ch}(y) = \frac{\alpha}{2} y^2$$

➔ (α, δ, DDL) solved by V_{ch} continuity and derivative continuity @ $V_{ch} = V_{DS,eff}$

➔ **Lateral field**:

$$E_y(y) = \begin{cases} \alpha y & if\ y < DDL \\ \frac{2}{\lambda}\delta \cosh\left(\frac{y - DDL}{\lambda}\right) & if\ y \geq DDL \end{cases}$$

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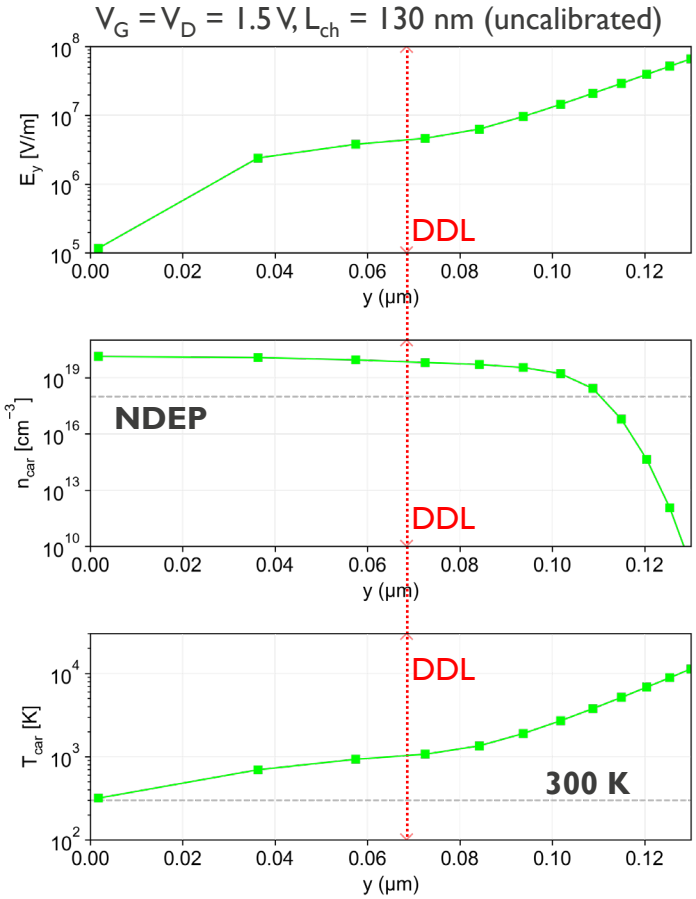
Guesstimated longitudinal solutions: $E_y(y)$, $n_{car}(y)$ and $T_{car}(y)$



- **Lateral field** ~10^7 V/m beyond DDL point, typical range obtained in TCAD [1]
- **Volume carrier concentration** using Q_{inv} based on 1D MOS equation

$$n_{car}(y) \approx \frac{Q_{inv}^2(V_{ch}(y))}{2k_B T \epsilon_{Si}}$$

  - n_{car} >> NDEP @ y = DDL, not depleted ➔ DDL here is velocity saturation
- **Carrier temperature** [2]

$$T_{car} = T_{lattice} + \frac{2}{3}\frac{q}{k_B}\tau_E v_{sat} E_{lat}$$

  - τ_E: energy relaxation time, ~ 0.3 ps
  - v_{SAT}: saturation velocity
  - Carrier temperature <10^3 K for y < DDL, but ~10^4 K at drain y >> DDL

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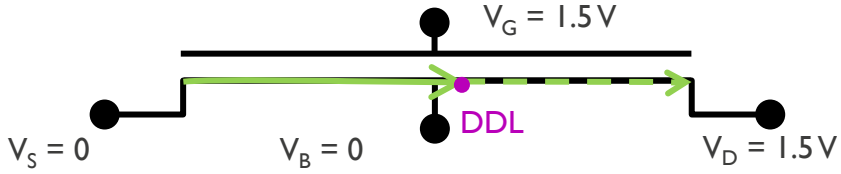
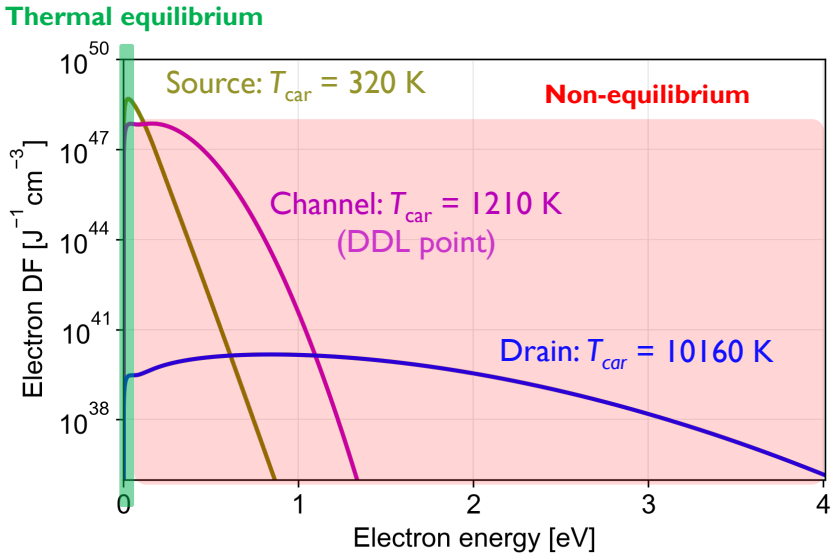
Verilog-A solved carrier DF for different positions

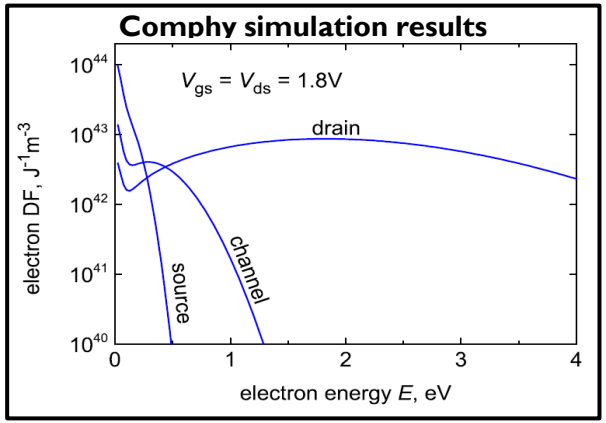
LCH = 130 NM, EOT = 1.9 NM (*UNCALIBRATED*)

$$f(\epsilon) = A\,exp\left(-\left(\frac{\epsilon}{\epsilon_{ref}}\right)^2\right) + C\,exp\left(-\frac{\epsilon}{k_B T_L}\right)$$





- Captures increasing non-equilibrium carrier distribution towards drain
- Qualitatively similar trend to Comphy simulation



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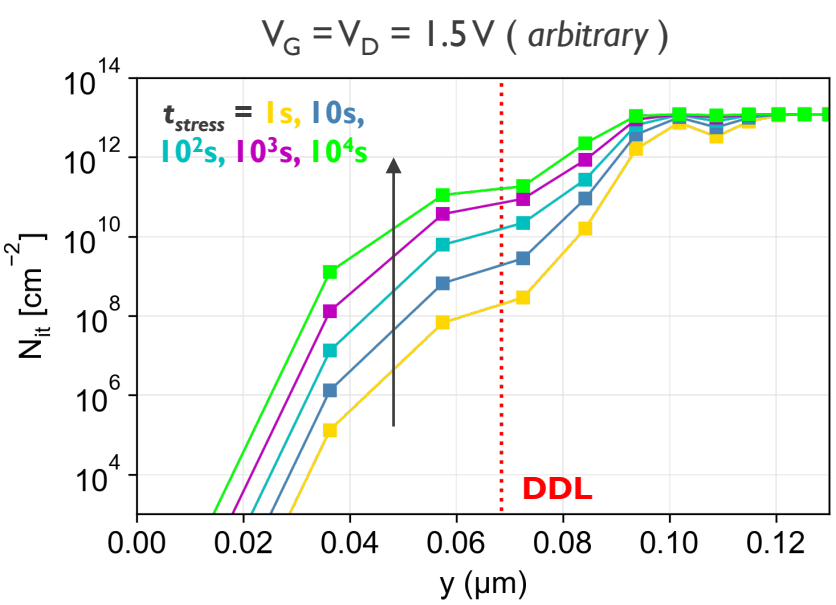
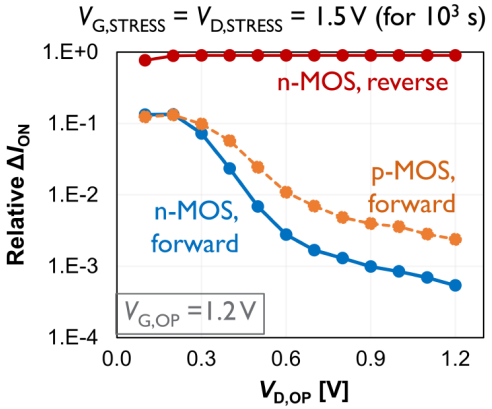
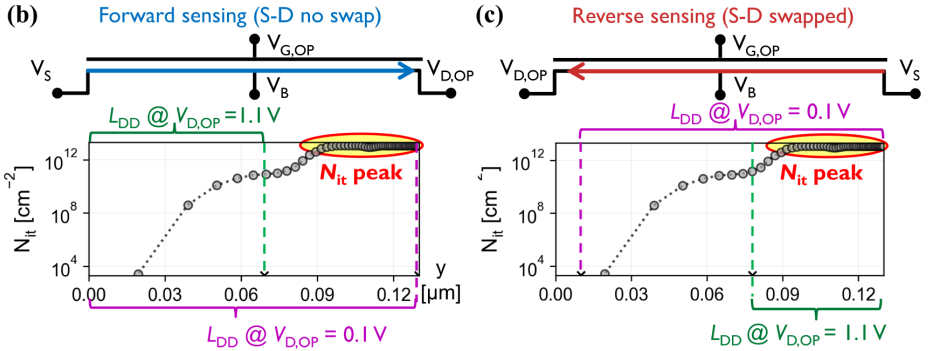
Verilog-A solved N_{it} profile along the channel using carrier DF $f(\varepsilon)$

LCH = 130 NM, EOT = 1.9 NM *(UNCALIBRATED)*



Captures asymmetry of degradation





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Summary: HCD embedded in (open-source) BSIM

BSIM probing

E_y (y)
n_{car} (y)
T_{car} (y)

EDF calculation $f(\varepsilon)$ (energy distribution function)

$f(\varepsilon)|_y$

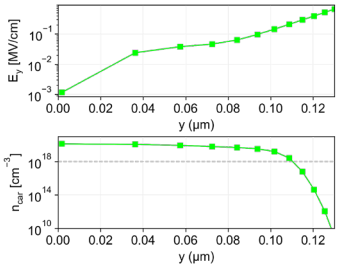
Total bond dissociation rate R_a

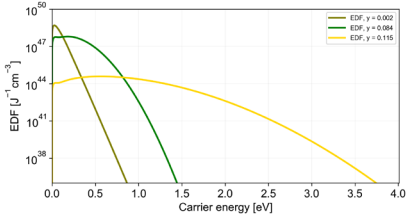
R_a(y)

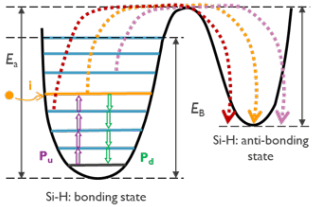
Degradation profile

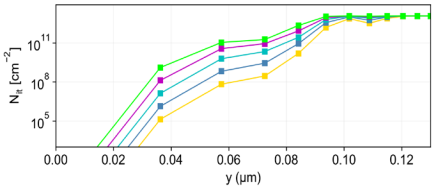
N_{it}(y)

Impact on device calculated



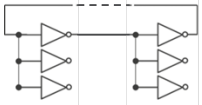


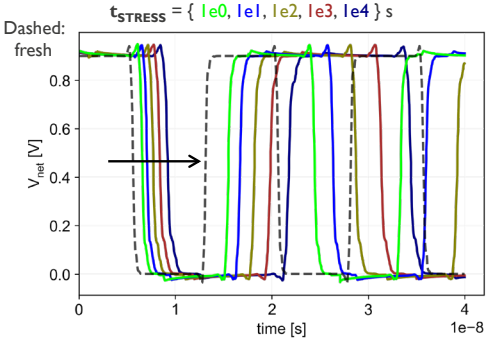


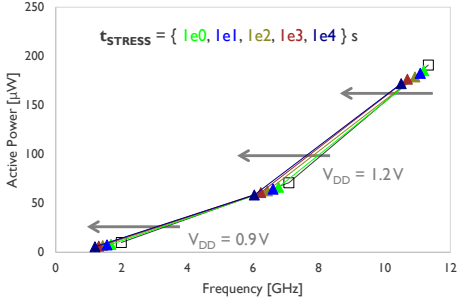


Example: SPICE simulation and frequency-power plot after HCD stress

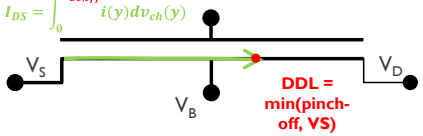
FO3, unloaded, 15 stages







$I_{DS} = \int_0^{V_{DS,eff}} i(y)dv_{ch}(y)$



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Outline

- Introduction
- Degradation mechanisms basics
  - Bias Temperature Instability (BTI) and Compact Physical (Comphy) model for trapping
  - Hot Carrier Degradation (HCD)
  - Self-Heating (SH)
  - Time-Dependent Dielectrics Breakdown (TDDB)
- Measuring degradation using on-chip circuits
- Approaches to reliability compact modeling
  - Comphy → CM
  - Comphy + HCD
  - sEKV-based CM
  - BSIM-based CM
  - TCAD → CM
- Conclusions

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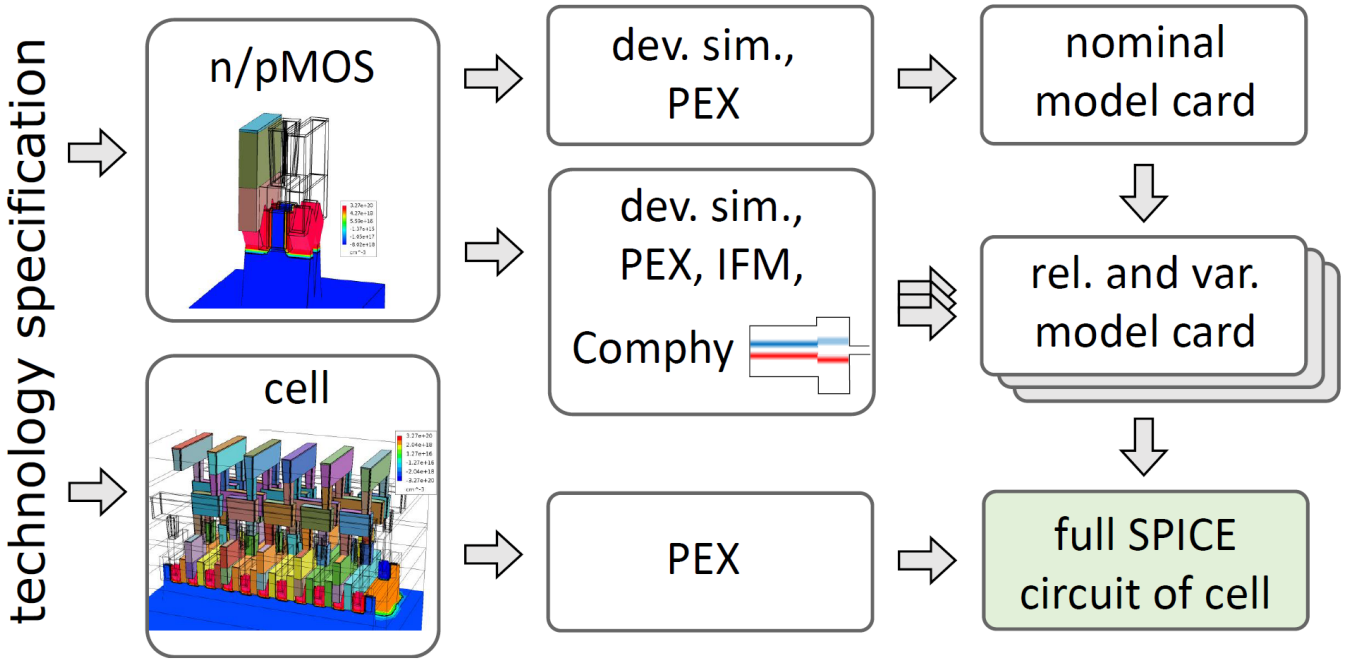
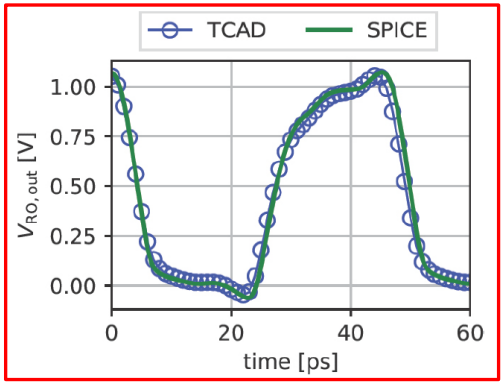
From TCAD to SPICE

"Reliability and Variability-Aware DTCO Flow"



- Device or simple cell simulated in TCAD
- SPICE circuit simulation via automated CM extraction



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Global TCAD Solutions

Also Prof. Asenov's group (Glasgow U.) → Synopsys

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Conclusions

- We know a lot about the physics of FET reliability
  - Degradation mechanisms, e.g. (non-uniform) trapping and defect generation
  - Properties of individual traps and degradation variability and statistics
- We have constructed multiple Reliability-Aware FET Compact Models
- We still need to understand better which properties are important to propagate to higher abstraction levels

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