



What's in the Standard?

Establishing the CMC Policy for Verilog-A Models

Geoffrey Coram, Analog Devices
CMC Technical Advisor for Verilog-A

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Outline



- History and Motivation
- Items for Consideration
- Current Status



History and Motivation



- Verilog-A has been accepted as the de facto standard language for compact modeling
- CMC requires new model candidates in VA
 - All recent models have been in VA:
MVSG, ASM-HEMT, LUTSOI
- Significant improvement over C (or Fortran!)



History and Motivation



- But how much of the Verilog-A code is considered “standard” ?
 - Everything (module name, parameters, operating-point values, noise names, warning messages, ...)
 - Only electrical quantities (currents & charges)
 - Something in between



History and Motivation



- Specific issue:
 - One simulator changed the sign of V_{TH} as defined in the Verilog-A code for PMOS devices
 - Does this violate the standard?



Items for Consideration



1. Module name
2. File name
3. Terminal names
4. Parameters
5. Operating-point values
6. Noise source names
7. Reference temperature
8. Temperature offset
9. Gmin
10. Scaling
11. Warning and error messages

1. Module name

- Hicum has module `hic2_full`
- Mextram has module `bjt504tva`,
`bjt504va`, `bjtd504tva`, `bjtd504va`
- PSP has module `PSP103VA`, `PSP103TVA`,
`PSPNQS103VA`
- HiSIM-HV has module `hisimhv_va`,
`hisimhv_n4_va`, `hisimhv_n5_va`
- BSIM-CMG has module `bsimcmg`
- BSIM-IMG has module `bsimimg`



1. Module name



- We want to have a standard convention for names
- Some simulators may not allow replacement of internal devices
- For debugging, useful to be able to instantiate VA and built-in in the same netlist
- **Requirement: module name should be lower-case, and append `_va` to the official name of the model**



4. Parameters



- Should parameters be declared UPPERCASE or lowercase?
- UPPER: PSP, MOSVAR, BSIM6, BSIMCMG, BSIMIMG, BSIMSOI, HiSIM, HiSIM-HV, HiSIM-SOI, HiSIM-SOTB, Mextram, Diode_CMC
- lower: HiCUM, R2_cmc, R3_cmc



4. Parameters



- UPPERCASE makes it easy to read the code and know which quantities are parameters
- lowercase is consistent with implementation in (case-sensitive) simulators
- Verilog-AMS uses lowercase in Annex E (Spice compatibility)
- Hard to switch between VA and built-in if case is not consistent

4. Parameters

- Requirement: parameters should be written in lower-case

- Model developers may want to use macro to visually mark parameters:

```
`define PAR(x) x
```

```
Weff = `PAR(w) + `PAR(dw) ;
```



5. Operating-point values



- Simulations may use op-pt values for SOA checks
- CMC's Open Model Interface (OMI) uses op-pt values for computations (e.g., aging)
- Values must be consistent across simulators
- **Requirement: Operating-point values are part of the standard**



Current Status



- CMC ballot on these 11 items
 - All passed per CMC voting policy
 - However, significant disagreement on Scaling (to be discussed at CMC Q4 meeting)
- Official policy document will be posted soon
- Suggestions for additional items are welcome



Implementation Timeline



- All new candidates for standard models are expected to follow the policy
- Existing CMC standards are not required to change
- Expectation that existing standards will be updated on the next version change (e.g., version 103.3 to 104.0)