

Si2 Compact Model Coalition: 2019 Update

Peter M. Lee, Si2 CMC Chairman

December 11, 2019

Contents

- General Information
- New Standards
 - Two new model standards are about to be released
 - HICUM/L0: Bipolar model for fast simulations approved in November for release
 - L-UTSOI: Ultra-thin-body SOI model (now in ballot, approval possible by Dec. 13)
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Present CMC Membership

- Total of 30 members for 2019

ams	Intel	Qualcomm	SK Hynix
Analog Devices	Keysight	Raytheon	Sony
AWR	Mentor Graphics	Renesas Electronics	ST Microelectronics
Broadcom	Micron	Samsung	Synopsys, Inc.
Cadence Design Systems	United Semiconductor Japan Co., Ltd.	Sandia Labs	Texas Instruments
GLOBALFOUNDRIES	NXP	Silvaco	Toshiba Memory
IBM	Empyrean Software	TowerJazz / Panasonic	TSMC
Infineon Technologies			ProPlus

Model Developers

- **University of California at Berkeley:** BSIM-Bulk, BSIM-SOI, BSIM-CMG, BSIM-IMG
- **Hiroshima University:** HiSIM2, HiSIM-HV, HiSIM-SOI, HiSIM-SOTB
- **India Institute of Technology, Kanpur:** BSIM-Bulk, BSIM-SOI, BSIM-CMG, BSIM-IMG, ASM-HEMT
- **CEA-LETI:** PSP, L-UTSOI
- **ADM Enterprises:** HICUM/L2, HICUM/L0
- **Auburn University:** Mextram
- **University of South Florida:** ASM-HEMT
- **University of Waterloo:** MVSG_CMC GaN HEMT
- **MIT:** MVSG_CMC GaN HEMT

Active Work Groups in the CMC

Work Group Names (CMOS Devices)	Chair
BSIM-Bulk	Kaiman Chan (Texas Instruments)
BSIM-CMG, Advanced Multigate Model	Richard Williams (IBM)
BSIM-SOI	Anupam Dutta (GLOBALFOUNDRIES)
BSIM-IMG	Tanvir Morshed (GLOBALFOUNDRIES)
HiSIM2, HiSIM_HV	Takeshi Naito (KIOXIA)
HiSIM_SOI, HiSIM_SOTB	Marek Mierzwinski (Keysight)
PSP	Andries Scholten (NXP)
L-UTSOI	Harrison Lee (Samsung)

Active Work Groups in the CMC (continued)

Work Group Name (Bipolar Devices)	Chair
HICUM/L0	Didier Celi (ST Micro)
HICUM/L2	Colin Shaw (Silvaco)
Mextram	Wei Chen (Texas Instruments)

Work Group Name (Other Devices)	Chair
ASM-HEMT, MVSG_CMC	Colin Shaw (Silvaco)
MOSVAR, Resistor Models	Geoffrey Coram (Analog Devices)
ESD Compact Models	You Li (GLOBALFOUNDRIES)

Active Work Groups in the CMC (continued)

Work Group Name (Other Standards)	Chair
Model QA and Release	Shahriar Moinian (Broadcom)
OMI API	Colin Shaw (Silvaco)
Reliability Model Standardization (not yet a standard)	Klaus-Willi Pieper (Infineon)
Verilog-A Recommended Practices	Geoffrey Coram (Analog Devices)
Operating Point Variable Names and Definitions	Samuel Mertens (Cadence)
Random Telegraph Noise (not yet a standard)	Min-Chie Jeng (TSMC)
GMIN	Ahmed Ramadan (Mentor Graphics)

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New Standards (1): HICUM/L0

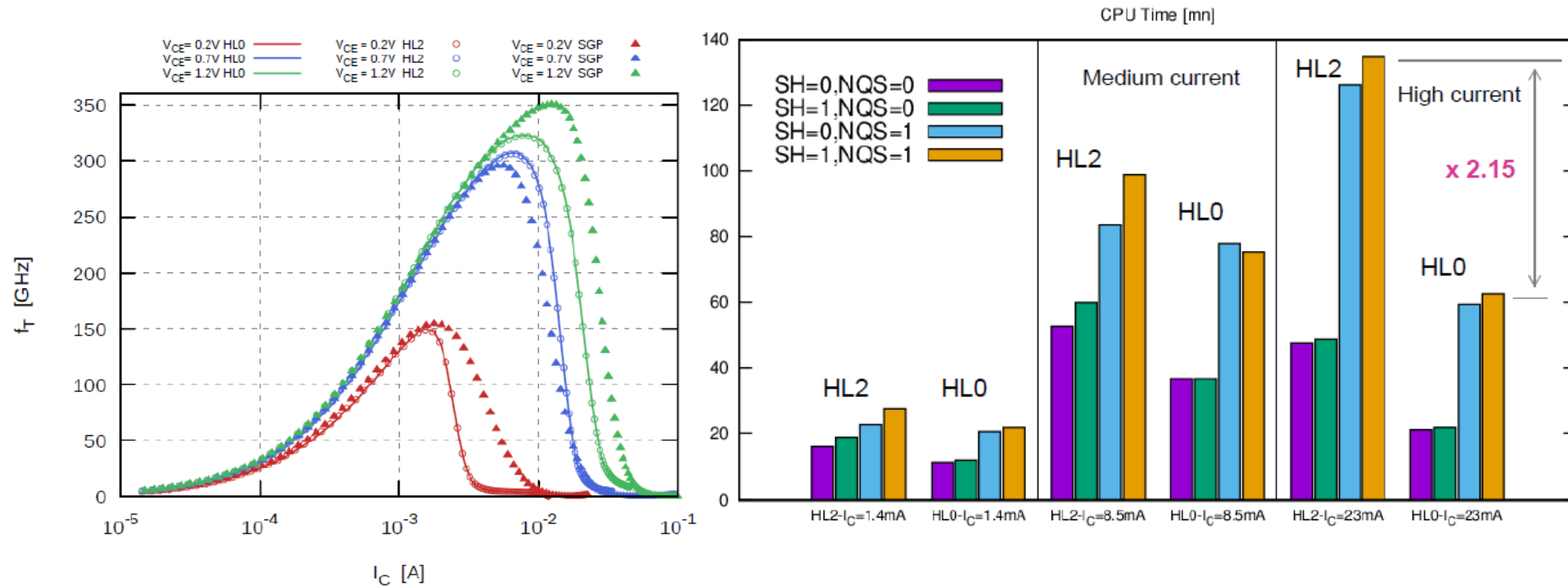
- **Fast bipolar model: HICUM/L0**
 - HICUM/L0 has been developed for addressing the need of **reducing simulation time** while maintaining sufficient accuracy for the bias, frequency, and temperature range relevant for HF design
 - Meets the need of designers wanting a faster model but with less features but sufficiently accurate for flagging major design errors
 - Easily interchangeable with the HICUM/L2 CMC-standardized model
- **Model Developer**
 - Michael Schroter (ADM Enterprises)

Features of HICUM/L0

Physical effects	HICUM/L 2	HICUM/L 0	SGP
BC capacitance partitioning	X	X	X
NQS effects	X	X	X
Bias dependence of the forward and reverse Early voltages	X	X	
BC and CS punch-through	X	X	
Parasitic BE and BC oxide capacitances	X	X	
Parasitic substrate PNP	X	X	
Conductivity modulation and current crowding of the base resistance	X	X	
Impact ionization	X	X	
Physics based transit time model	X	X	
Bias and bandgap dependent reverse Early voltage (HBTs)	X	X	
Self-heating	X	X	
Split of the base resistance with BE and BC capacitances	X		
BE capacitance partitioning	X		
Substrate network	X		
I_C and I_B noise correlation	X		
BC barrier effect at high currents	X		
Tunneling current in the EB junction (reverse mode only)	X		
Lateral scaling and lateral NQS effects	X		

HICUM/L0 Performance

- HICUM/L0 addresses the requests from designers to have a simple model (equivalent circuit) like the SGP model, but more accurate than SGP and faster than HICUM/L2



New Standards (2): L-UTSOI

- Ultra-thin body SOI new model: L-UTSOI
 - L-UTSOI comes from Leti-UTSOI, a highly mature model first developed in 2007 and used in industrial environment for about 8 years, thus spanning several industrial technology generations. The model is based on more than 25 years of CEA-Leti expertise on fully-depleted SOI technology.
 - Since 2013, this model is able to physically describe the fully-depleted SOI transistor behavior whatever the bias configuration, including the case of strong forward back bias, in which two channels exist at the front and back interfaces of the thin silicon body. This relies on a unique solution for surface potential analytical calculations, as well as on innovative solutions to describe the current and charge models.
- Model Developer
 - CEA-Leti

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New Model Releases (2018-2019)

- **BSIM-CMG 111.0.0**
 - Developer: University of California, Berkeley
 - Released: September 12, 2019
 - Features: 25 new enhancements and 13 bug fixes improving accuracy, convergence, and performance ([Si2 press release](#))
- **BSIM-IMG 102.9.2**
 - Developer: University of California, Berkeley
 - Released: December 20, 2018
 - Features: 2 new enhancements and 6 bug fixes. Enhancements include binning equation for quantum mechanical effects and drain-induced V_{th} shift.

New Model Releases (continued)

- **HiSIM2 3.1.0**
 - Hiroshima University
 - Released: November 11, 2018
 - Features: Six new enhancements and one bug fix
 - Additional bug fix version released as HiSIM2 3.1.1 on April 4, 2019 (junction diode related)
- **HiSIM_HV 2.5.0**
 - Developer: Hiroshima University
 - Released: May 21, 2019
 - Features: Five new enhancements and two bug fixes
- **PSP 103.7.0**
 - Developer: CEA-LETI
 - Released: May, 2019
 - Features: Six enhancements and a bug fix

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Look-ahead Projects

- **ESD**
 - Goal: Standardize on an ESD model based on a diode
 - Status: Studying models proposed by two university model developers
- **Reliability Model**
 - Goal: Standardize a device-level degradation model
 - Status: Currently studying a model from one university. Another university is also proposing to participate
- **Random Telegraph Noise (RTN)**
 - Goal: Standardize an RTN model
 - Status: Starting initial background studies. Planning to start searching for existing models developed by universities or research institutions as candidates for consideration

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New CMC Policies

- 18-month exclusivity of newly released CMC standards
 - From 2018, Si2 has instituted a policy to restrict model code and documentation of new releases to CMC members for 18 months before they become available to the general public
 - These newest releases are available for download from the Si2 website for CMC members.
 - This does not restrict the general public from using the models themselves. New standard models will be available for use in EDA vendor tools as soon as they are released from the vendors
 - Model documentation and Verilog-A code will be made available to the general public 18 months after release

More information is available at the Si2 websites as follows:

Si2: <http://www.si2.org/>

CMC: <http://www.si2.org/cmc/>

Standard models: <http://www.si2.org/standard-models/>

