MOS-AK FOSS Compact Modeling Perspective

Technology - Devices - IC Design

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www.mos-ak.org

FOSS TCAD/EDA tools for semiconductor device modeling

Technology - Devices - IC Design

Outline

- Moore's Law
- Numerical TCAD Device Simulations
- Schematic Entry and Circuit Simulation
  - Qucs
  - ngspice
  - Xyce
  - GnuCap
- Device Level Parameter Extraction
- Standardized Data Exchange Format For Device Modeling
- 2019 MOS-AK Compact/SPICE Modeling Events

Moore’s Law

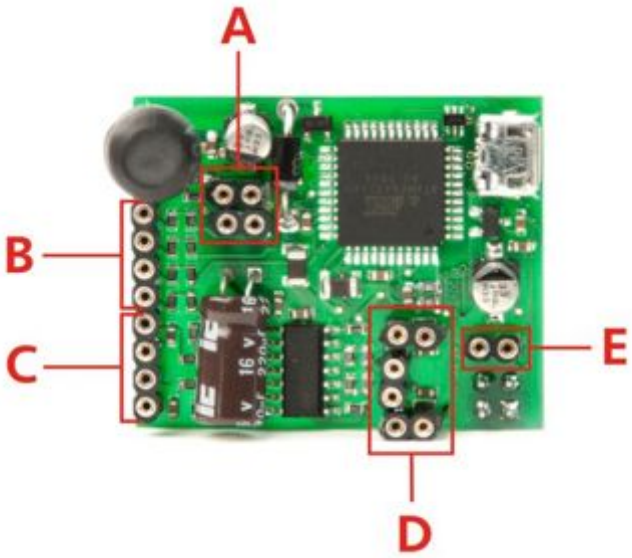
The first working monolithic devices (IC) presented by Fairchild Semiconductor on May 26, 1960

The Raspberry Pi Zero is half the size of a ModelA+, with twice the utility. A tiny Raspberry Pi that’s affordable enough for any project!
($5 or event free as early 2016)
<www.raspberrypi.org/products/pi-zero>

Five Powerful Lab Instruments

Open Hardware Board

On-board is a complete arsenal of electronic engineering instruments: **only $29**

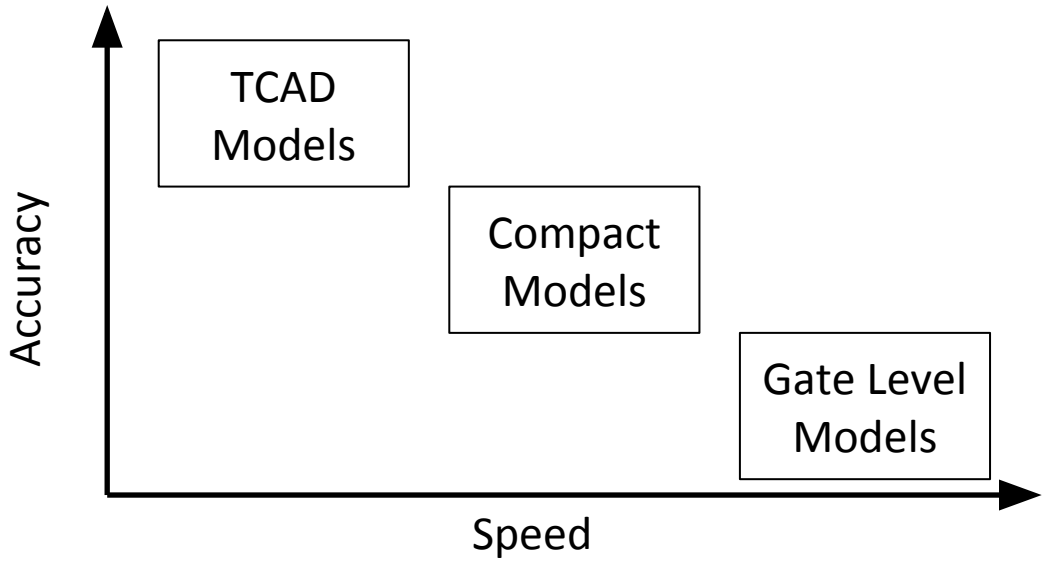


A. Power Supply (4.5 to 15V, 1.5W max)
B. Digital Output
C. Function Generator (2 channel, 1MSPS)
D. Oscilloscope/Multimeter (2 channel, 750kSPS)
E. Logic Analyzer (2 channel, 3MSPS)

https://espotek.com/labrador/product/espotek-labrador-board/

Compact/SPICE Modeling

- A model of semiconductor device charges, currents and voltages
- Built from physically-motivated equations
- Intended for use in an analog circuit simulator



REF: G.J. Coram, "How to (and How NOT to) Write a Compact Model in Verilog-A", BMAS2004 Tutorial

FOSS Modeling/Simulation Flow

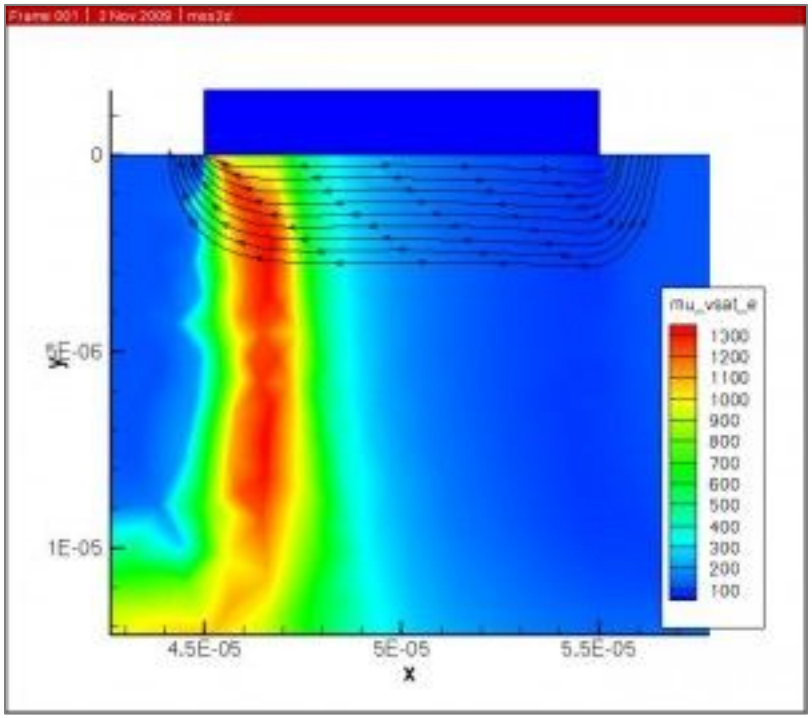
- Cogenda TCAD
- DevSim TCAD
- *Other*
  EM Simulators

- Spice/Verilog-A Simulators
- Paragon
- Tiburon RTE
- ADMS
- i-MOS
- MAPP
- *parameterization*
- *other*

- Ngspice
- Qucs
- Xyce
- GnuCap
- *other*

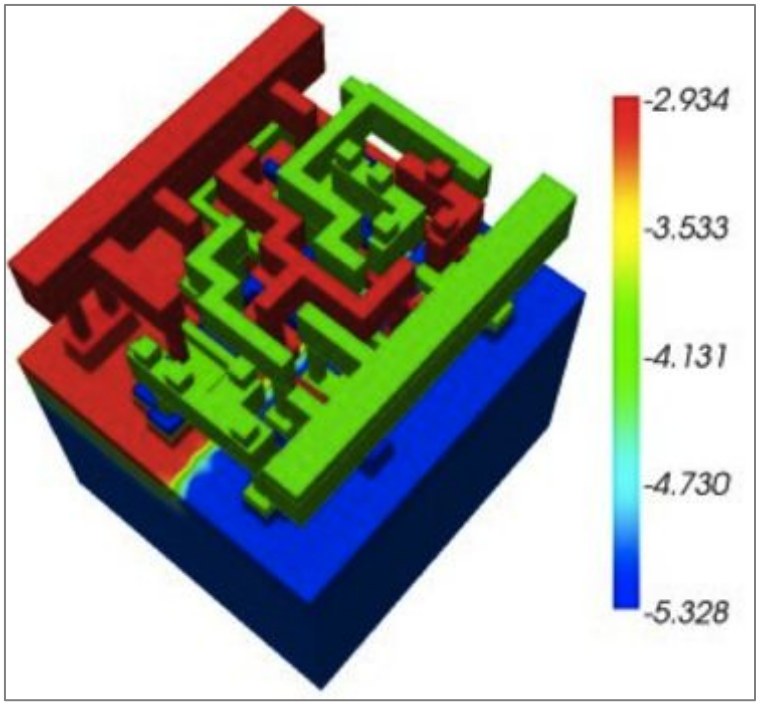
Process TCAD Simulation

- DevSim TCAD



2D MOSFET simulation

- Cogenda TCAD



3D SRAM Cell

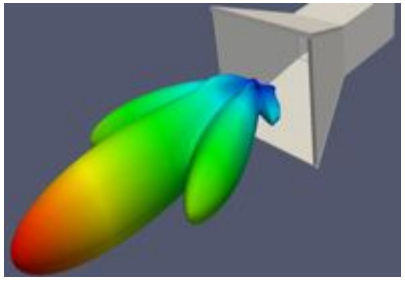
Free Computational Electromagnetic (EM) Modeling Tools

The software in this list is either free or available at a nominal charge and can be downloaded over the internet. Some of the codes require the user to register with the distributor's web site. If you are familiar with other free EM modeling software that that should be added to this list, please send the name of the software, a hypertext link, and a brief description to CVEL-L@clemson.edu.

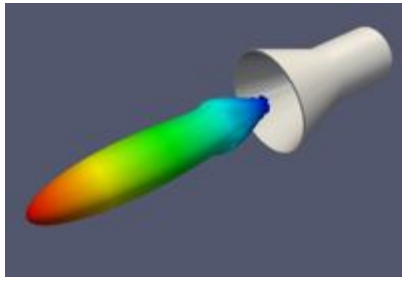
ASAP - Antenna Scatterers Analysis Program
AtaiTec Free 2D Field Solver
ATLC - Arbitrary Transmission Line Calculator
ATLC2 - Arbitrary Transmission Line Calculator 2
emAnalyze
EMAP
EMCoS Antenna VLab SV
EM Explorer
emGine Environment
ERMES
FastCap and FastHenry
FEKO LITE
FEMM - Finite Element Method Magnetics
gprMax
MagNet (Infolytica)
MMANA-GAL (basic version)
MEEP
MMTL
Multiple Multipole (MMP) Algorithms
NEC2
newFasant (student version)
openEMS
pdnMesh
Puma-EM
Qsci
Radia
SATE Static Field Analysis Toolkit (Educational)
Students' QuickField
Sonnet Lite
Trace Analyzer

openEMS: FOSS Electromagnetic Field Solver

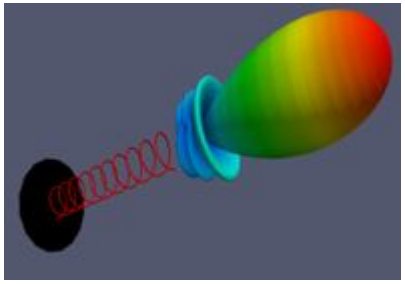
http://openems.de



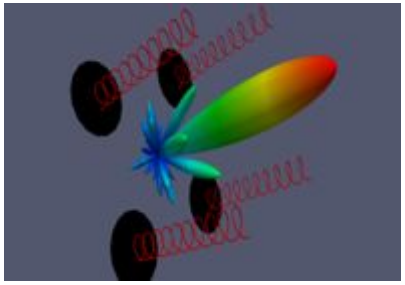
Horn antenna



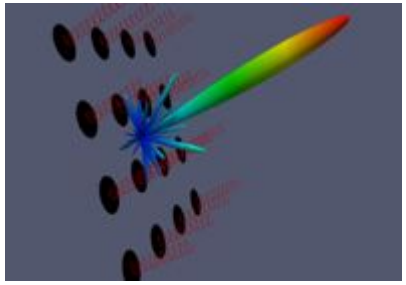
Conical horn antenna



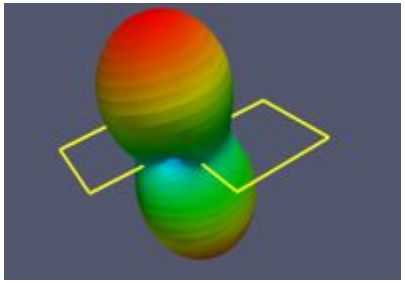
Helix antenna



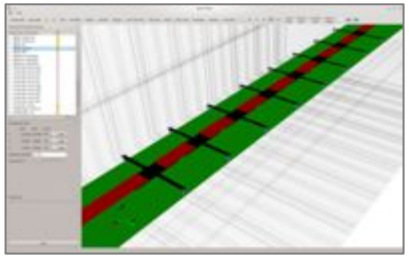
Helix antenna array



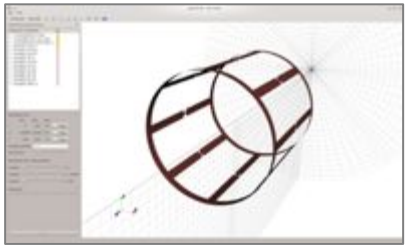
Large helix antenna array



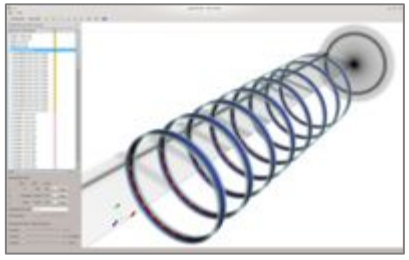
Biquad antenna



CRLH antenna

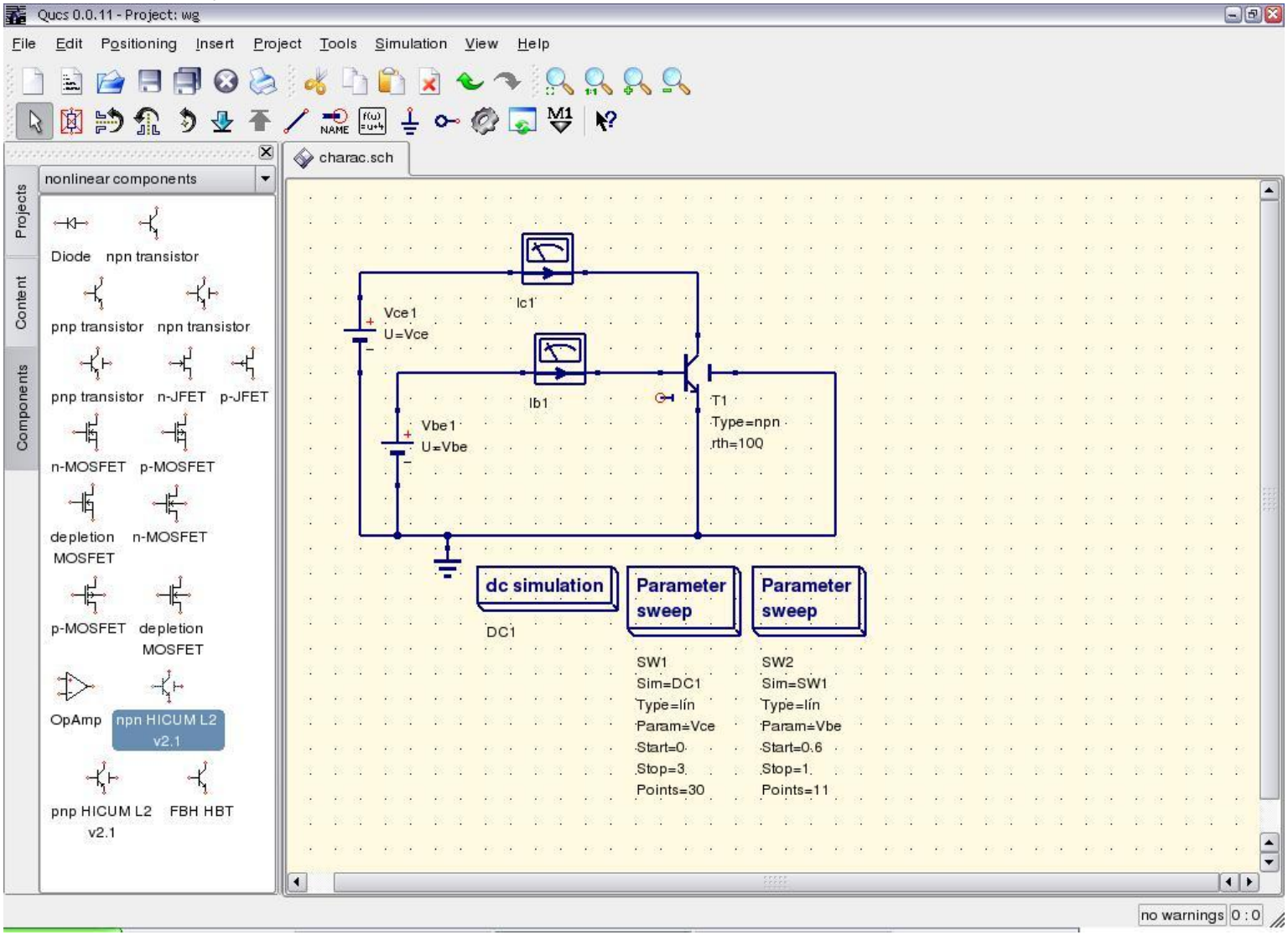


MRI birdcage model



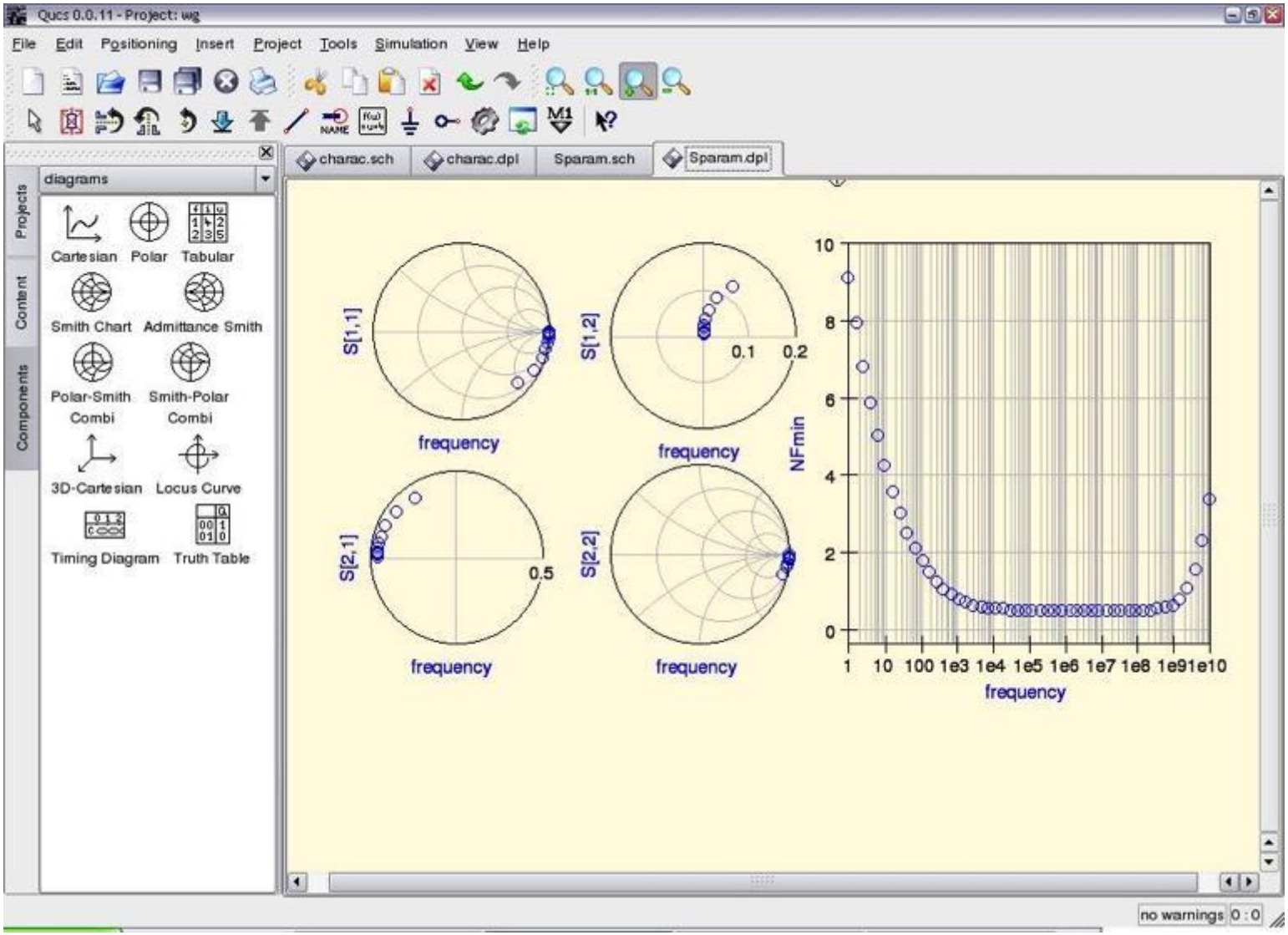
MRI ring antennas

QUCS: HiCUM Schematic



Quite Universal Circuit Simulator: qucs.sourceforge.net

QUCS: HiCUM S-Parameters



Quite Universal Circuit Simulator: qucs.sourceforge.net

NGSpice & ADMS

Ngspice uses ADMS for Verilog-A modeling:

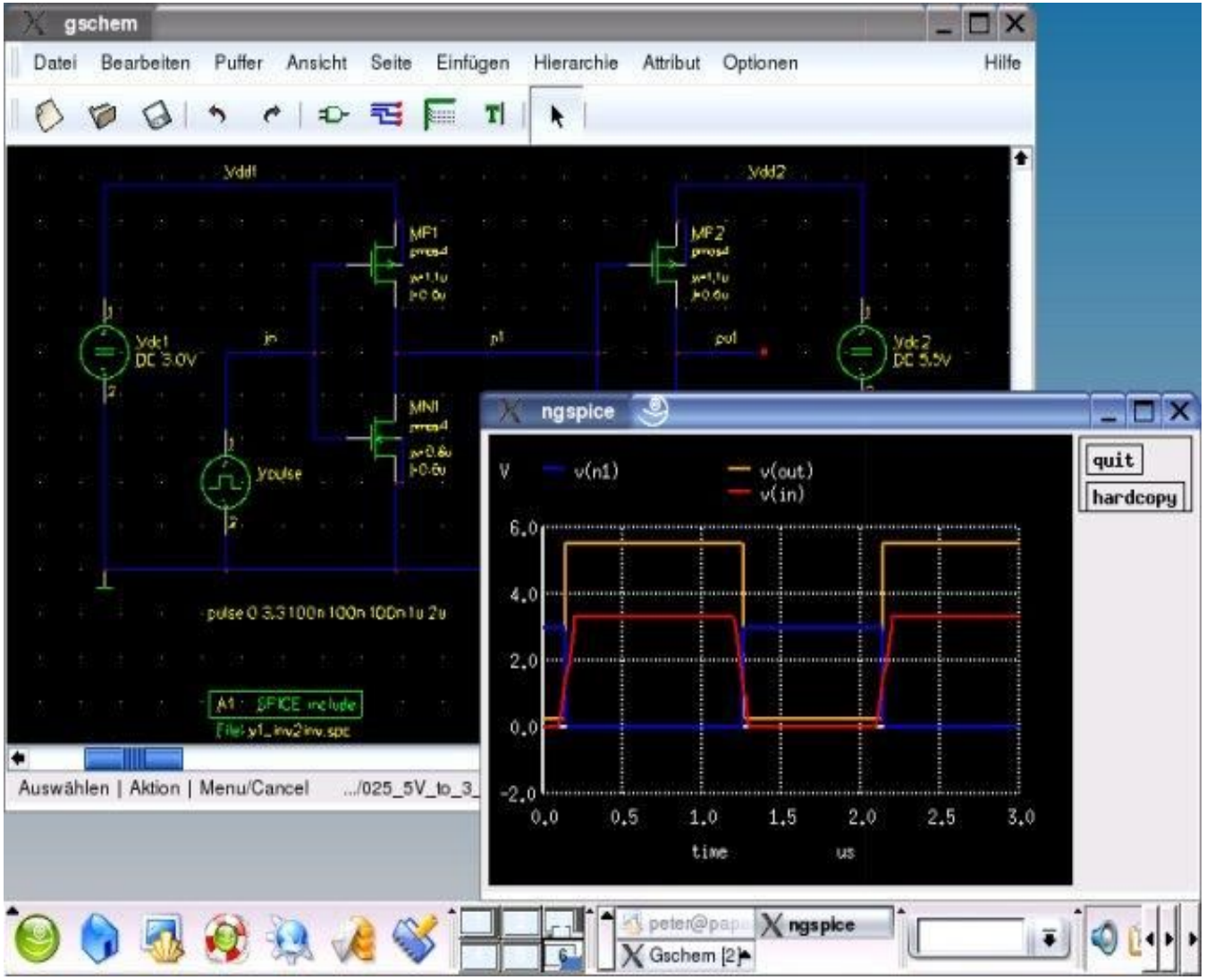
ADMS is a code generator that converts electrical models written in Verilog-A into C code conforming to the API of spice simulators. The generated code will then be compiled into the simulator executable and the new device is ready for simulation.

ADMS is not (yet) included into NGSpice and must be downloaded separately.

- ADMS templates are used to translate Verilog-A code and fill with the appropriate code NGSpice model structure.
- There exist a template file for each file to be created.
- Spice noise analysis is not (yet) supported.
- There exist a “special” template file needed to generate the Makefile.am needed by NGSpice to build C code from XML and this file is processed first

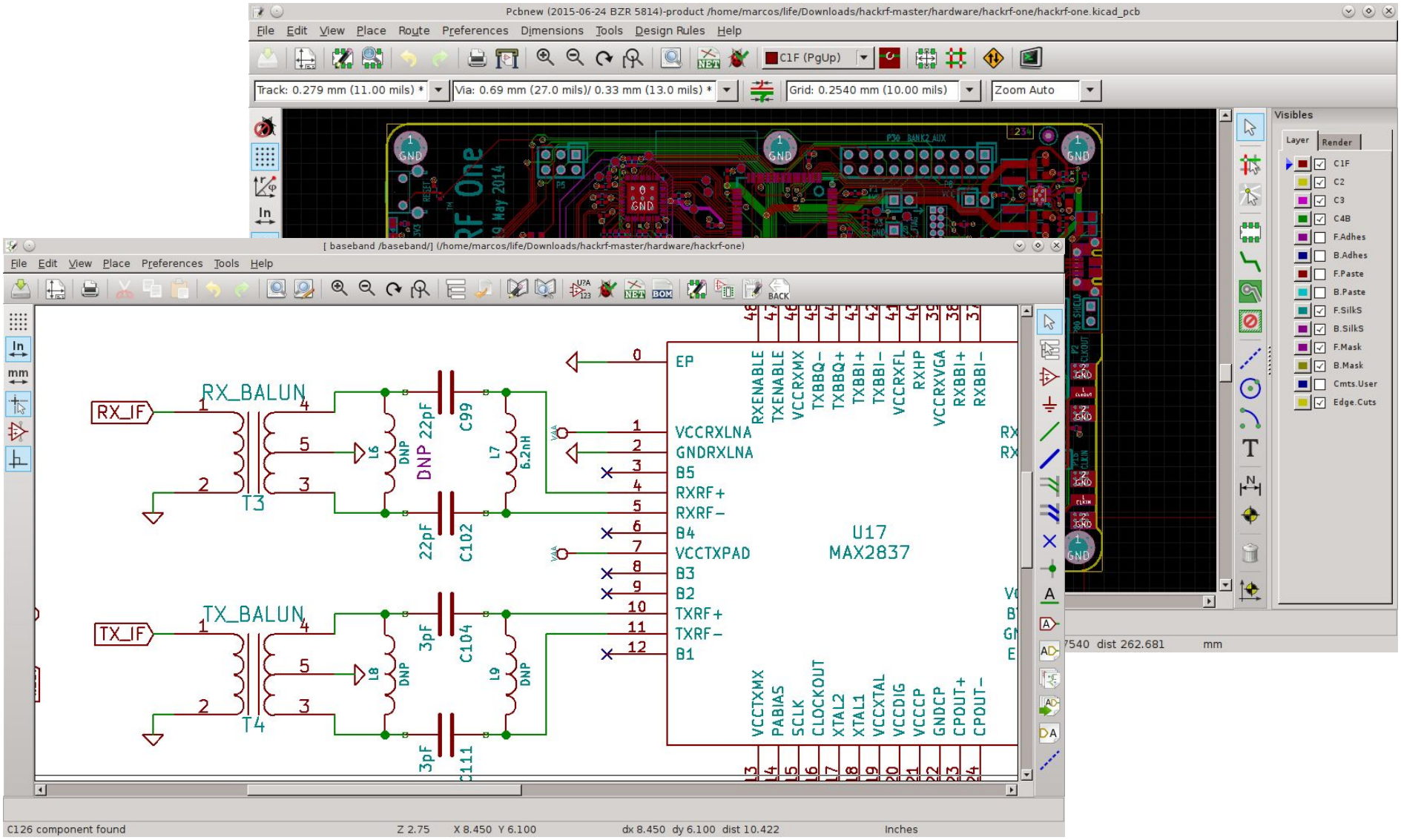
- http://ngspice.sourceforge.net/admshowto.html
- http://ngspice.sourceforge.net/adms2/adms-svn-ngspice-src.zip

NGSpice & ADMS



http://ngspice.sourceforge.net/

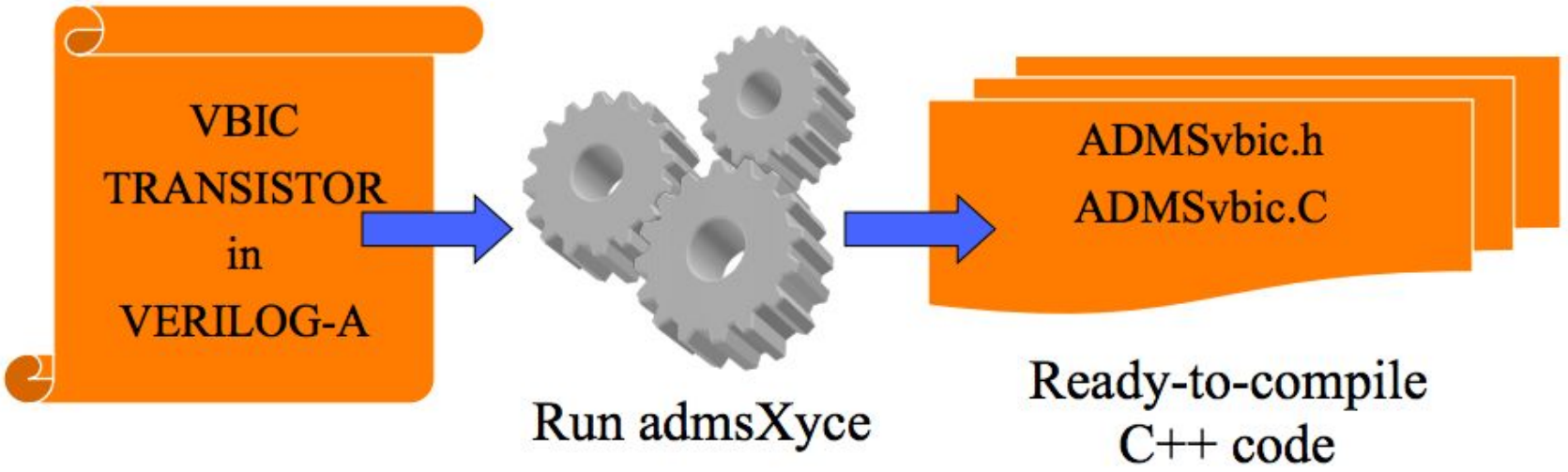
ngspice and KiCAD



http://kicad-pcb.org

Xyce & ADMS

- Verilog-A interface, via ADMS model compiler
  - VBIC, Mextram, EKV, HiCUM, etc.
- Verilog-A: industry standard format for new models
- ADMS translates Verilog-A to compilable C/C++ code;
- API automatically handles data structures, matrices, tedious details.



https://xyce.sandia.gov/

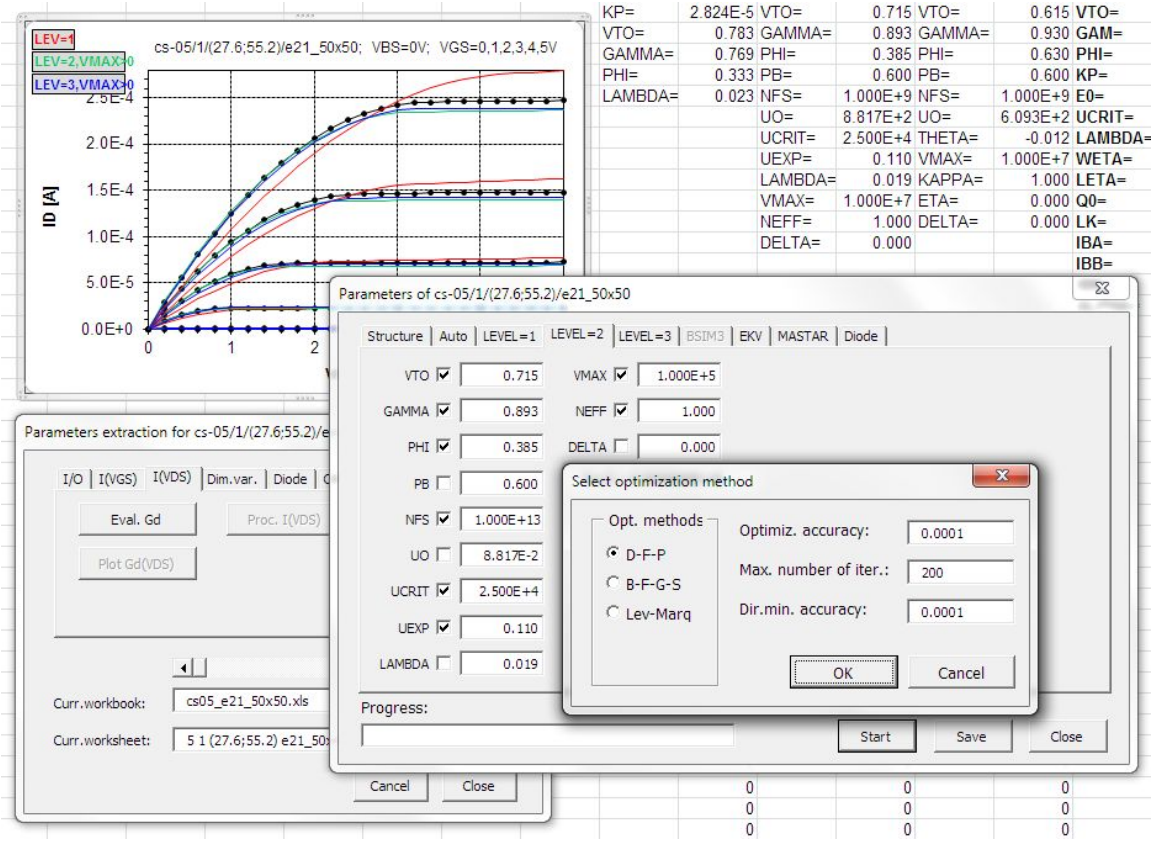
Gnucap: GNU Circuit Analysis Package

- Gnucap is a modern post-spice circuit simulator with several advantages over Spice derivatives.
- Additional Gnucap GIT repositories:
  - ADMS model compiler
  - Device models
  - Gnucap-modelgen Verilog model compiler

www.gnucap.org

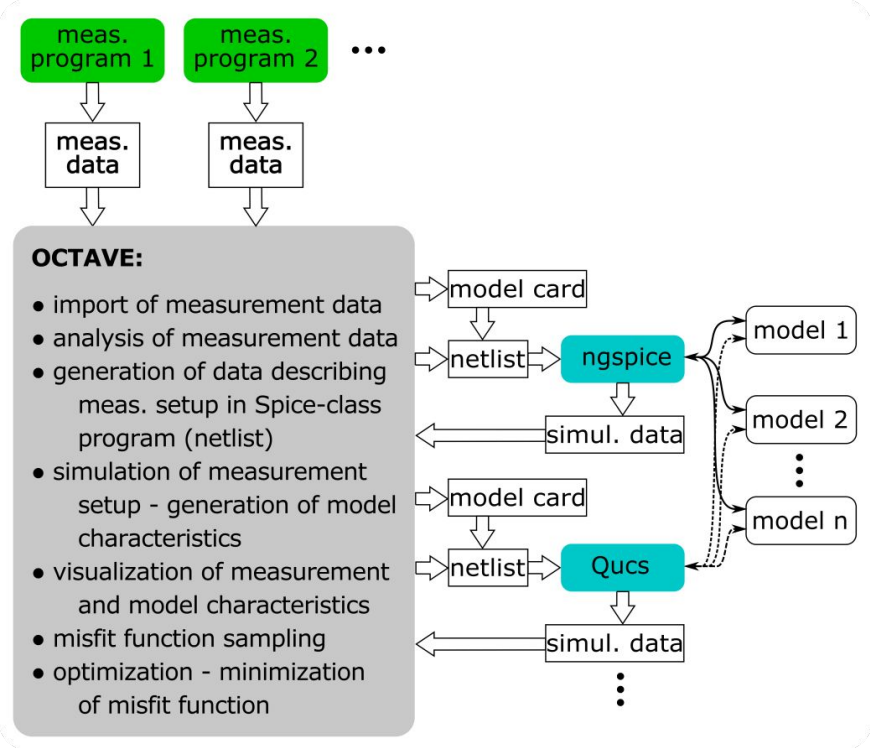
MS Excel VBA Parameter Extraction

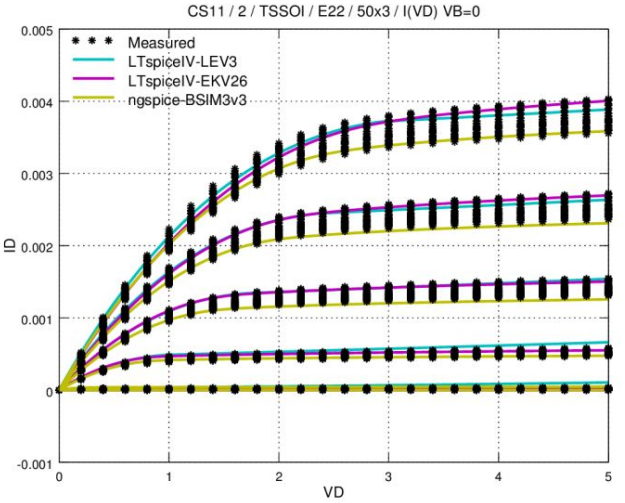
- Local parameter extraction using MS Excel VBA optimization

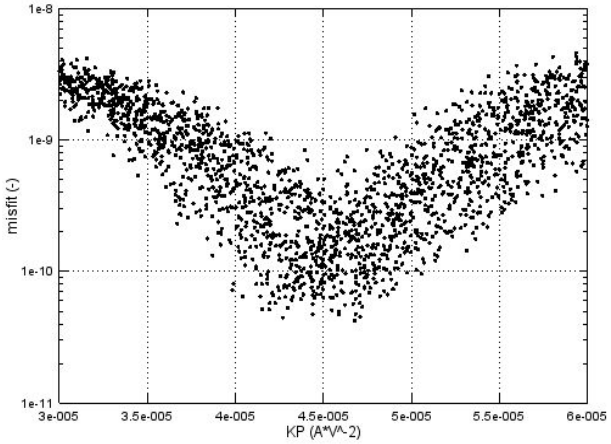


[Ref] D. Tomaszewski, A. Kociubiński, J. Marczewski, K. Kucharski, K. Domański, P. Grabiec, "A Versatile Tool for Extraction of MOSFETs Parameters", Proc. 6th Y&D Symposium, 2003, Warsaw

OCTAVE for Parameter Extraction







[Ref] D. Tomaszewski, G. Głuszko, M. Brinson, V. Kuznetsov, W. Grabinski, "FOSS as an Efficient Tool for Extraction of MOSFET Compact Model Parameters", MIXDES'2016

PROFILE: Inverse Modeling Tool

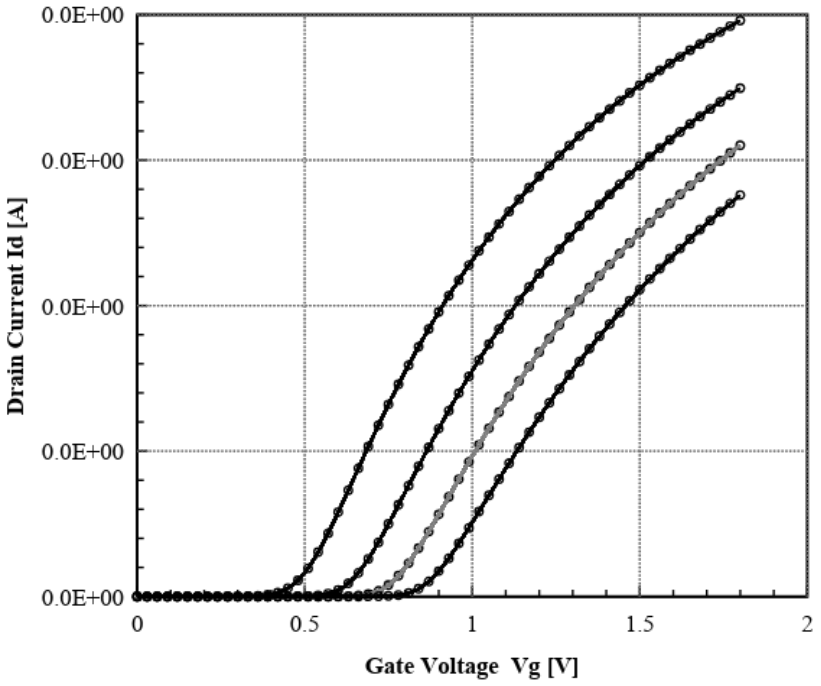
The **PROFILE** [1] is a tool for inverse modeling of the semiconductor devices using 2D data and advanced optimization driver. All the files and its documentation is available at the official homepage of PROFILE:

http://profile.ewi.tudelft.nl/
http://sourceforge.net/projects/profile2d

[REF] G.J.L. Ouwerling. Inverse modelling with the PROFILE optimization driver. NASECODE VI Software Forum, Dublin, July 1989.

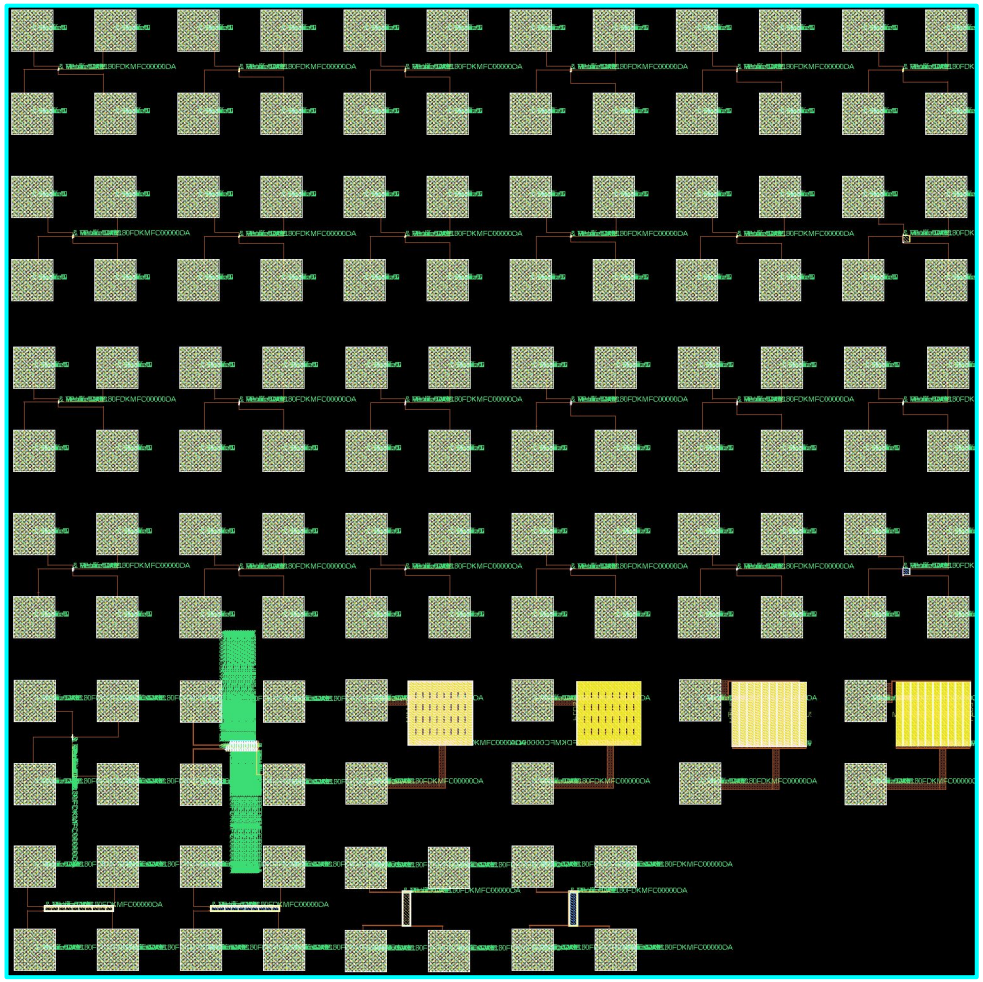
PROFILE: Inverse Modeling Tool

```
: main.pro : main optimization loop
type v_m i_m i_s $
var real VTO UO KP $
: read measured IV data
get IdVg.dat v_m i_m $
: set LEVEL3 parameters
VTO = 1.0
UO  = 425
KP  = 2E-4
: Constrain specifications
constrain VTO 0.1 2
constrain UO  100 500
constrain KP 0.1E-4 1E-3
setlm deltapr 0.01
: call external non-linear model
setext call ~/bin/profile ngspice.pro >
ngspice.log
setlm talk 2
setlm itermax 15
: levmar fits a non-linear model to
measurement data.
levmar pro i_m v_m i_s VTO KP | UO $
```

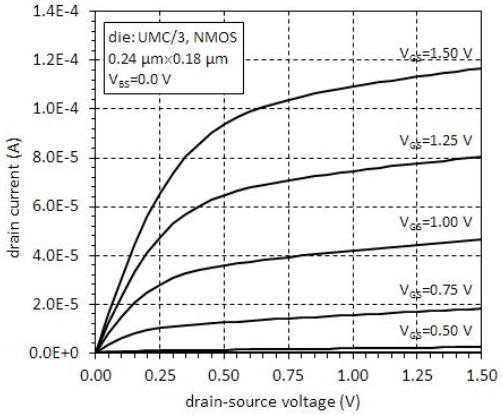


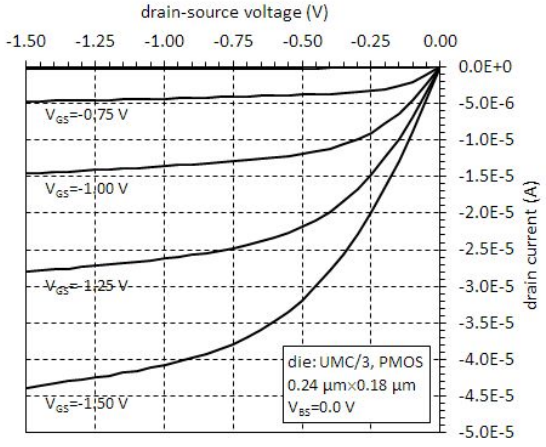
Transfer MOSFET IV characteristic after VTO, U0, KP extraction (**o** :measured, **-** :simulated)

FOSS EKV2.6 UMC 180nm Validation



Free Silicon EKV2.6 Test Chip
in UMC 180nm





Output characteristics
n- and p-mos 0.24x0.18um

FOSS Modeling/Simulation Flow

- Cogenda TCAD
- DevSim TCAD
- *Other*
  ***EM** Simulators*

- Spice/Verilog-A Modeling Platform
  - ADMS
  - MAPP
  - VALint
- *measurements*
- *parameterization*
- *other*

- Ngspice
- Qucs
- Xyce
- GnuCap
- *other*

FOSS TCAD/EDA tools for semiconductor device modeling

Technology - Devices - IC Design

SUMMARY (open topics)

- Process TCAD Simulation
  - Interoperability:
    Data Exchange Formats
- Compact/SPICE Modeling
  - **Verilog-A Standardization**
  - **Simulated/Measured Data Exchange**
- Analog/RF IC Design
  - Interoperability:
    Netlist/Schematic Exchange Formats

Arbeitskreis Modellierung von Systemen und Parameterextraktion
Modeling of Systems and Parameter Extraction Working Group

2019 MOS-AK Events

- FOSDEM CAD/EDA DevRoom
  with ngspice and GnuCap talks
  Feb.3, 2019, ULB Solbosch, Brussels (B)
- 1st **MOS-AK** at LAEDC
  Feb. 25-28 2019 Armenia (CO)
- 2nd **MOS-AK** India Conference
  Feb. 25-27, 2019, IIT Hyderabad (IN)
- 4rd Sino **MOS-AK** Workshop
  June 20-23, 2019, UECST Chengdu (CN)
- MIXDES Special CM Session
  June 27-29, 2019, Rzeszow (PL)
- 17th **MOS-AK** at ESSDERC/ESSCIRC
  Joint ESSDERC/ESSCIRC Tutorial
  ESSDERC TPC Track 4: Compact Modeling
  September 23-26, 2019, AHG Krakow (PL)