From Physics to Power, Performance, and Parasitics

The GTS-Team

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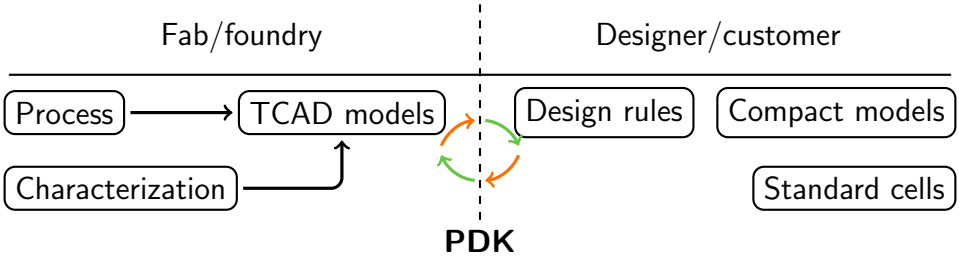
Scales, methods, hierarchies

Abstraction level	Transistors	Description	Quantity
System level	1.000.000.000	Behavioral	Message
Register transfer level (HDL)	1.000.000		
Gate level	1.000.000	Signal state	0/1
Transistor level (SPICE)	10.000	ODE	I
Classical TCAD	100	PDE (DD)	$\mathbf{J}(x, y, z)$
Nano TCAD	1	PIDE (SBTE)	$\mathbf{J}_n(x, y, z, E)$
Quantum transport	≤ 1	NEGF	
Atomistic	< 1	DFT	

Introducing TCAD in design



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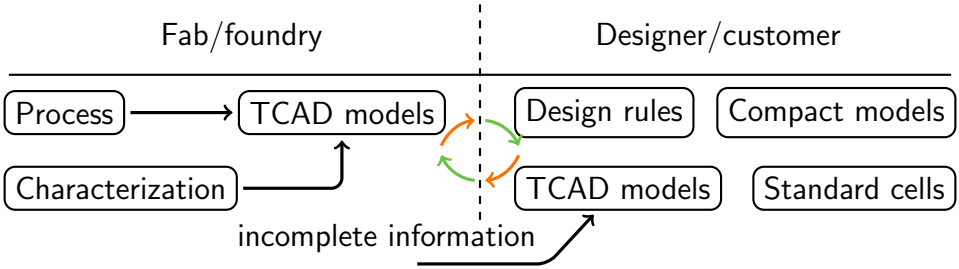


- Potential benefit: More spot-on designs; fewer, shorter iterations
- Problem for TCAD in design: Where to start from?
- No calibrated device models (mobility)
- No detailed process information

Our solutions

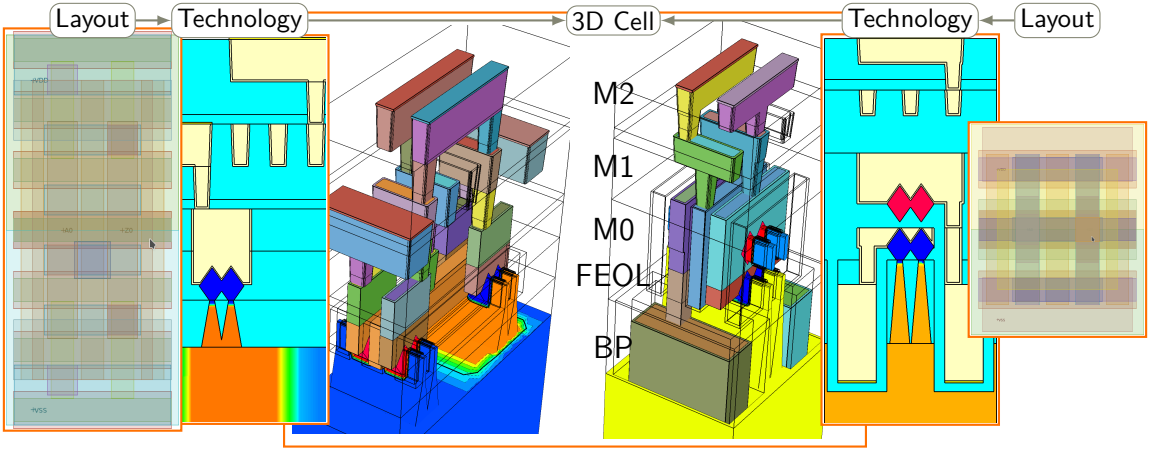
Nano-scale TCAD ⟵ Single-device TCAD ⟶ Large-scale TCAD

- Path finding
- Process to device to cell to circuit variability
- Design-technology co-optimization (DTCO)

Modules

- Layout-based structrue generation
  - Rapid prototyping
  - Process-flow awareness
- Device simulation
  - Steady-state, transient, AC
  - Reliability
  - What about calibration?
- Parasitics extraction
  - R/C-network topology extraction
- Self-heating
  - Quasi-transient simulation
  - Thermal network extraction

Layout-based structure generation



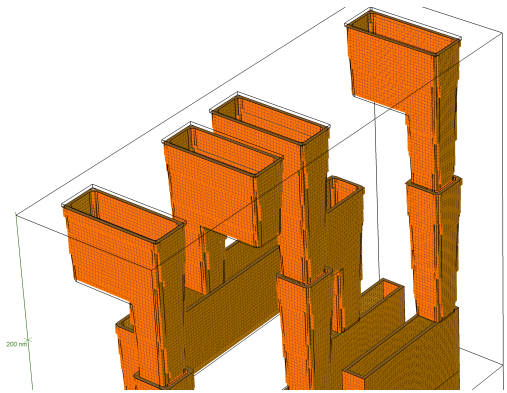
Process emulators

- Voxel-based topographical process emulators
  - Coventor SEMulator3D
  - Synopsys Process Explorer
- Valuable tools for process exploration and integration
- Lacking features of a full-fledged process simulator
- Require detailed knowledge about process

- Combination with device simulation poses difficulties
- Voxel-based topography contains step-like surfaces
- Layer thicknesses?
- Requires *repair* procedure
- May contain *artifacts*
- High number of surface points

$\rightsquigarrow$ Large mesh size, excessive device simulation times

Process emulators



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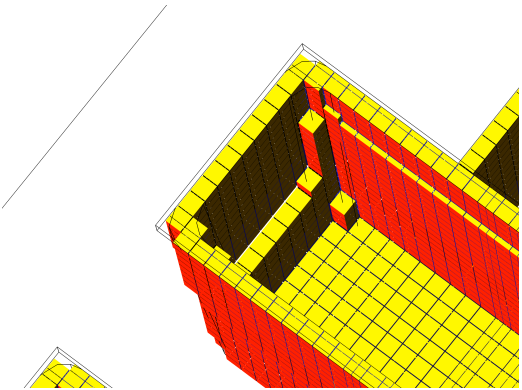

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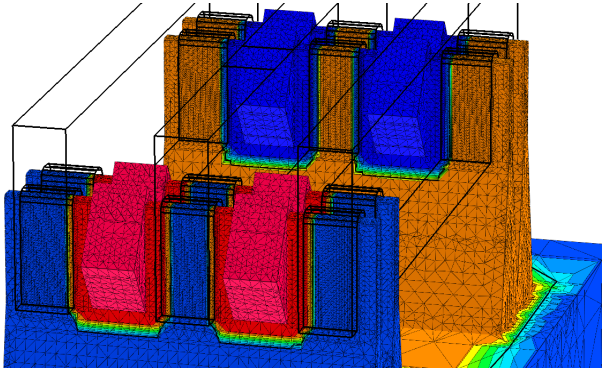
What is Layout-Based Structure Generation?

- Built on a Constructive Solid Geometry (CSG) kernel
- Human-readable/writeable script (*Tech* file) directs CGS kernel based on layout (GDSII file)
- No process details required
- Process-flow aware
- Integrated meshing, high-quality mesh output, no repairs
- 2 $\times$ less mesh points than process emulation
- 5 $\times$ faster device simulation
- 100 % successful convergence

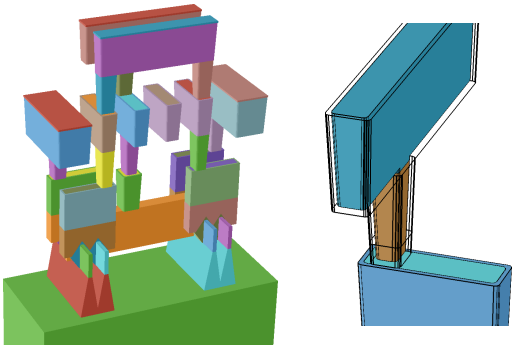
Layout-based structure generation – FEOL

- "TechX" based on IMEC iN14
- Fin tapering
- Rounded corners
- Conformal dielectric layers
- Realistic epi-shapes
- Process-flow awareness:
  - Self-aligned processes
  - Doping distribution

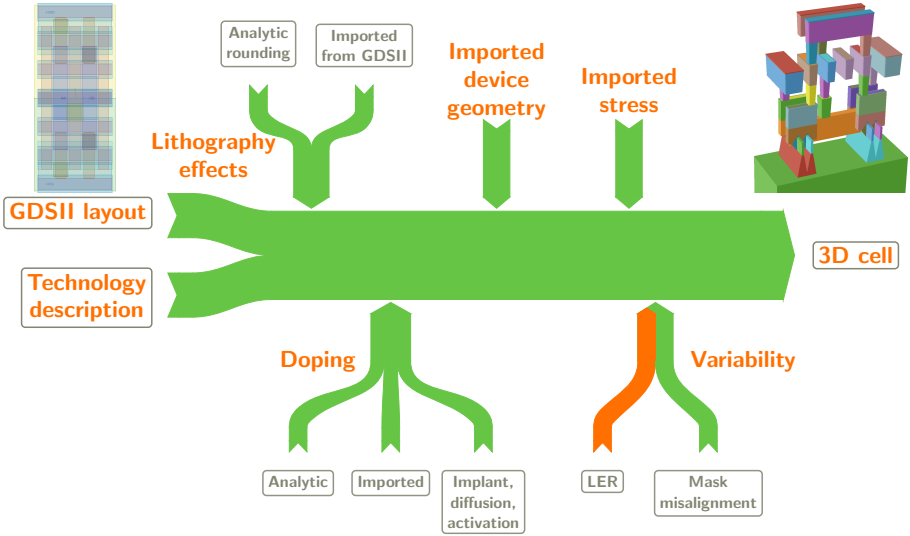


Layout-based structure generation – BEOL

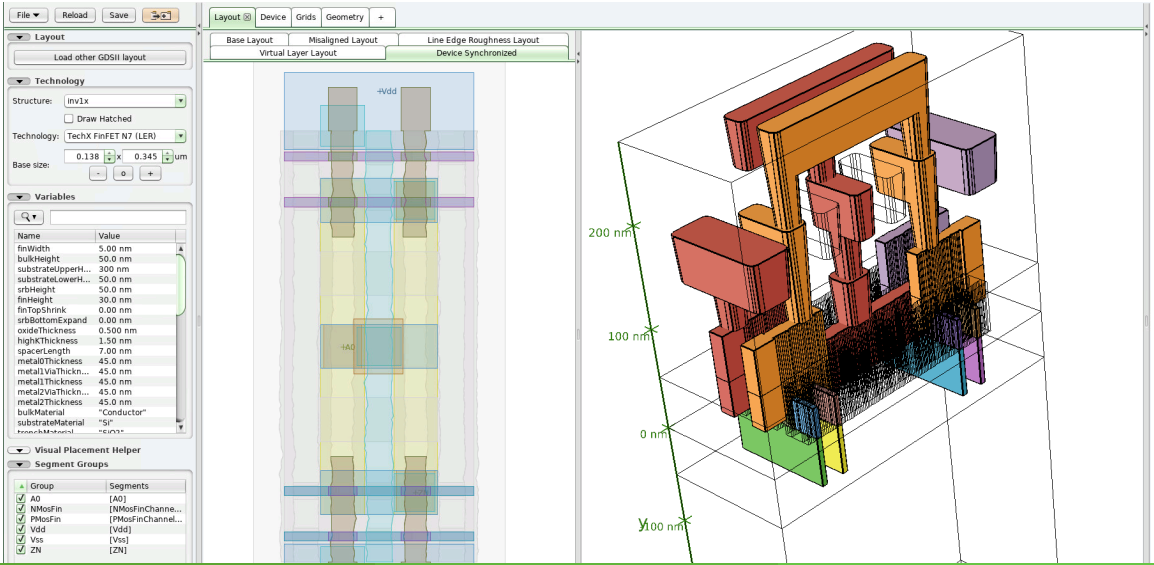
- "TechX" based on IMEC iN14
- Realistic interconnect geometries
- Conformal TiN-barriers
- Cu-fill



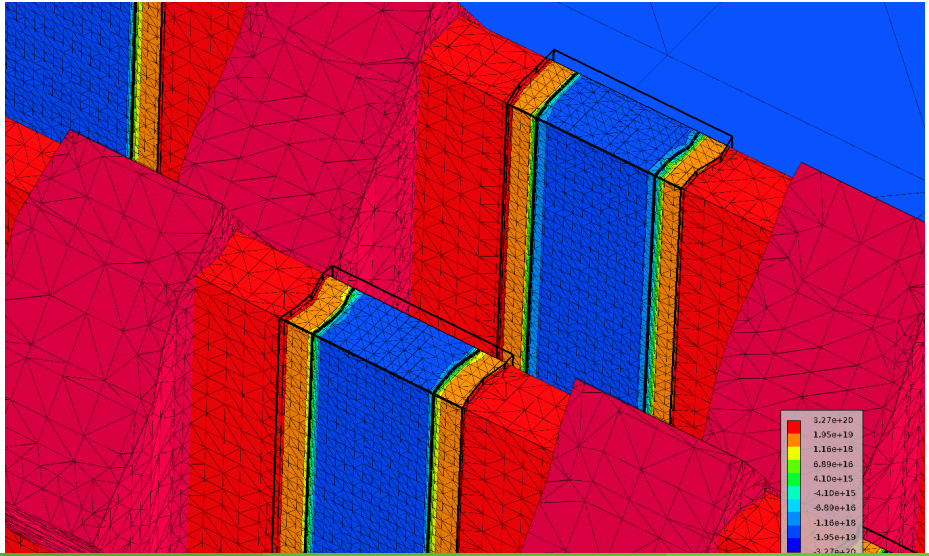
Variability: line-edge roughness (LER)



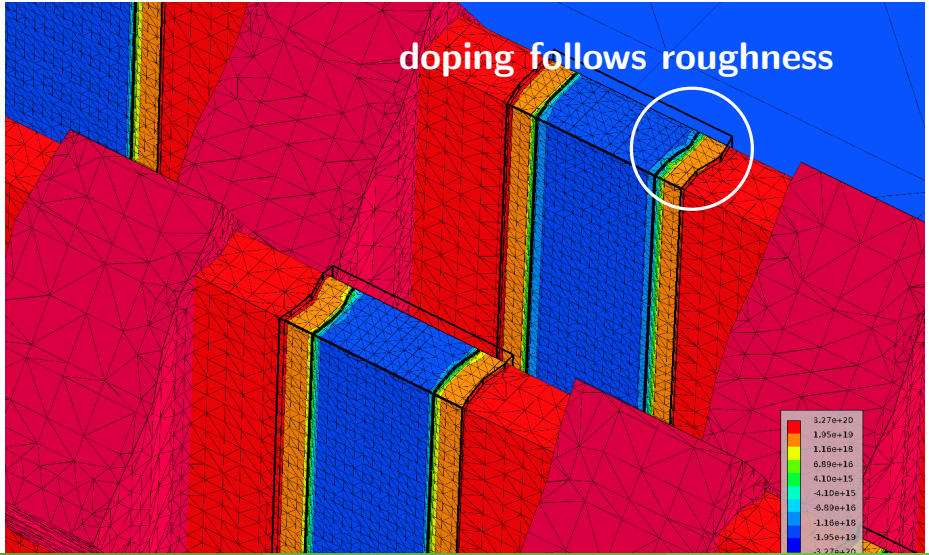
Adding LER to gate lines



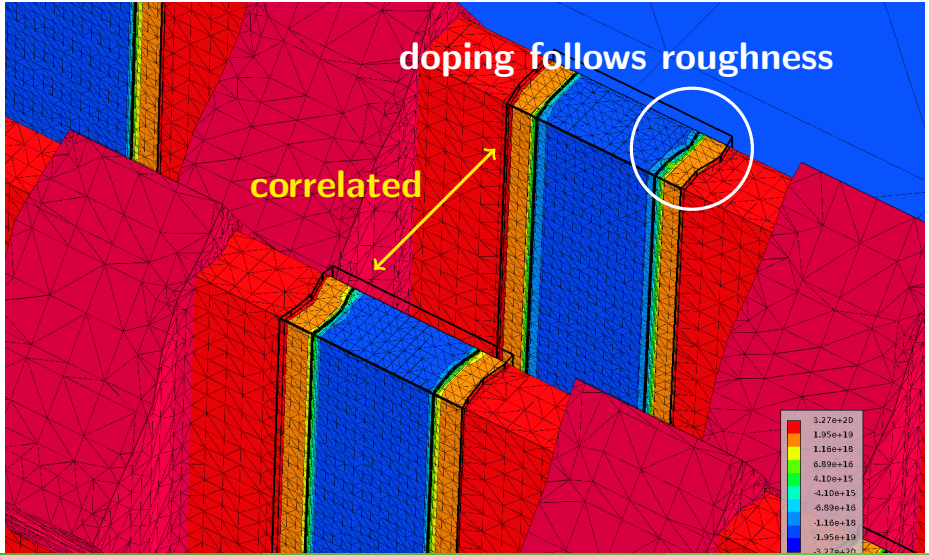
Doping with LER – closeup



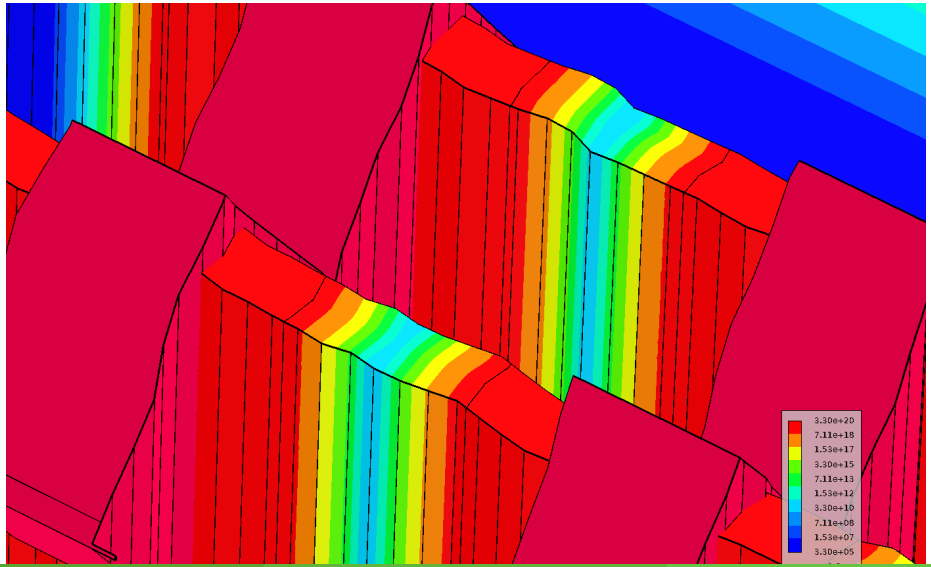
Doping with LER – closeup



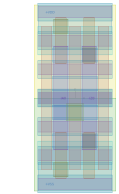
Doping with LER – closeup



Adding LER to fin patterning mask (SADP)



Variability: mask misalignment



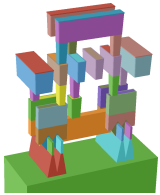
Analytic rounding

Imported from GDSII

Lithography effects

Imported device geometry

Imported stress



GDSII layout

Technology description

3D cell

Doping

Variability

Analytic

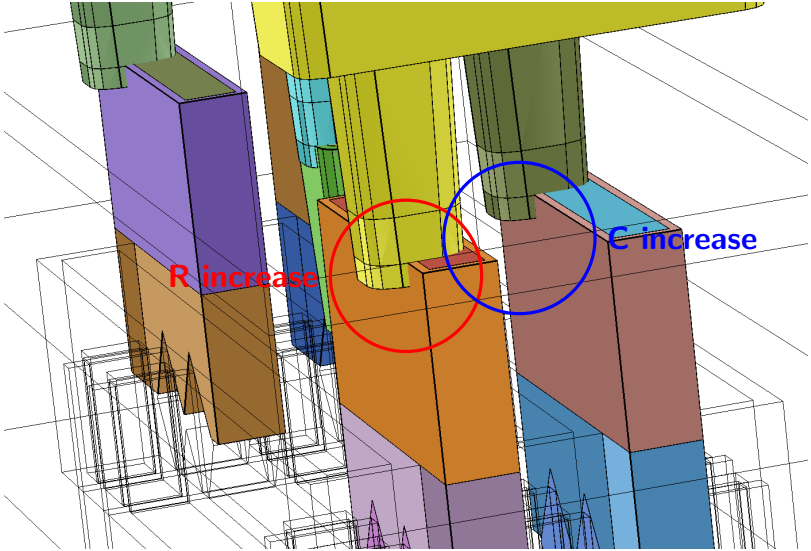
Imported

Implant, diffusion, activation

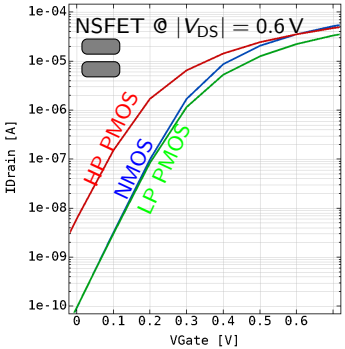
LER

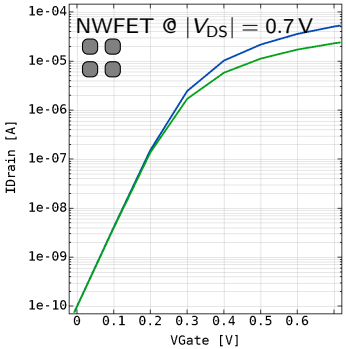
Mask misalignment

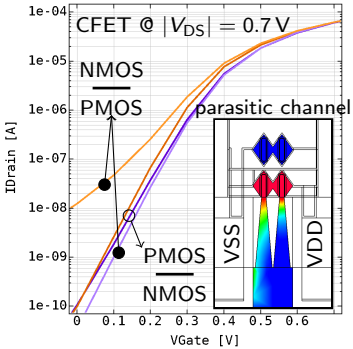
Mask misalignment



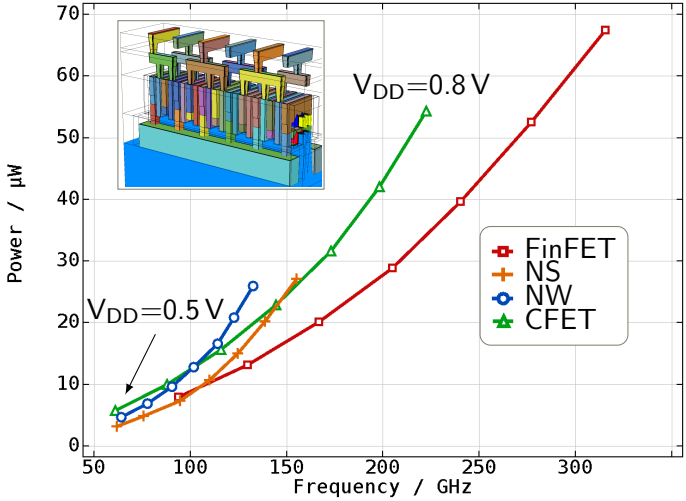
Device simulation – steady-state characteristics



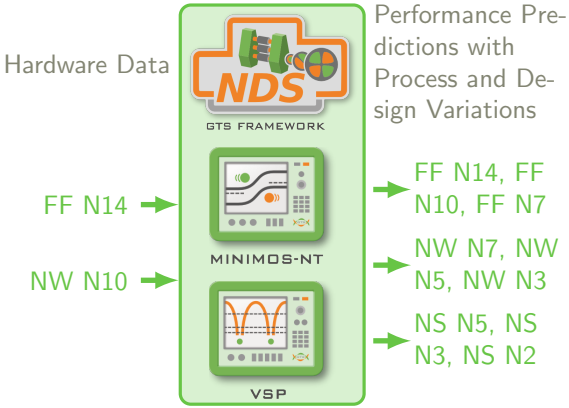


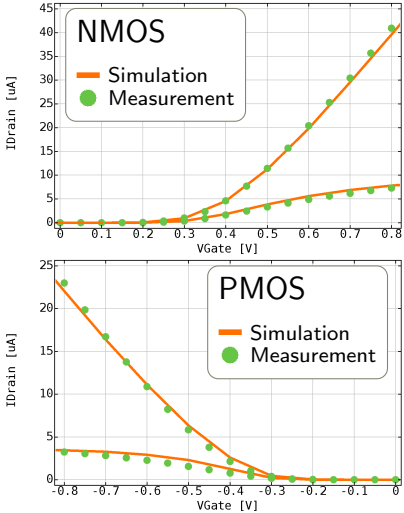


Transient device simulation – power vs. performance

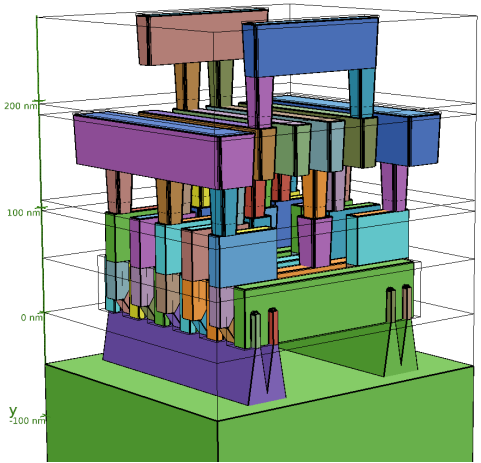


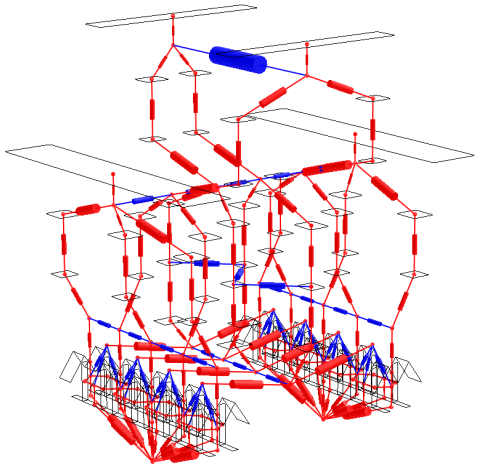
Calibration & prediction



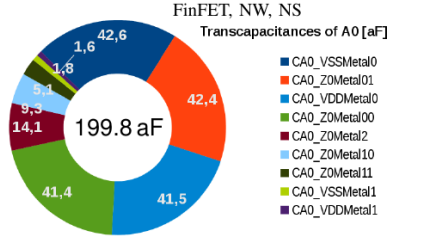


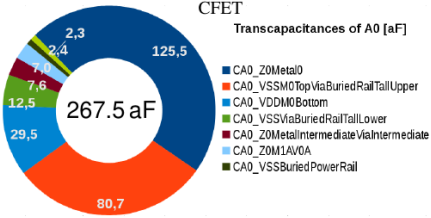
Automated parasitics extraction

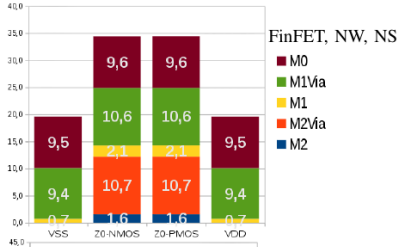


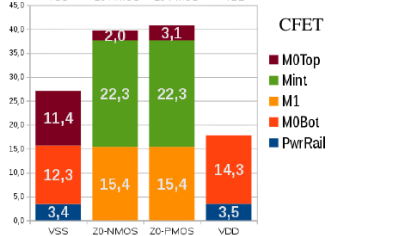


BEOL resistances & capacitances

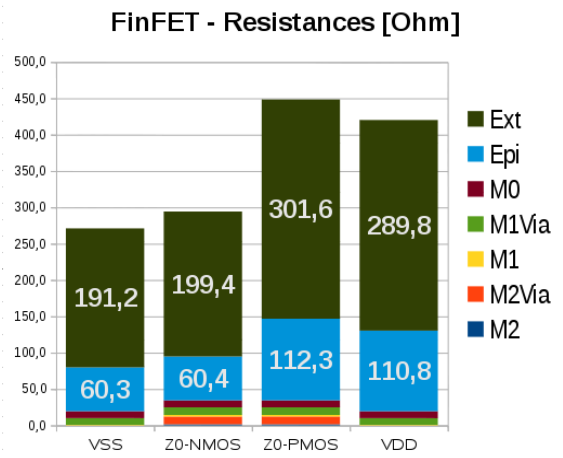


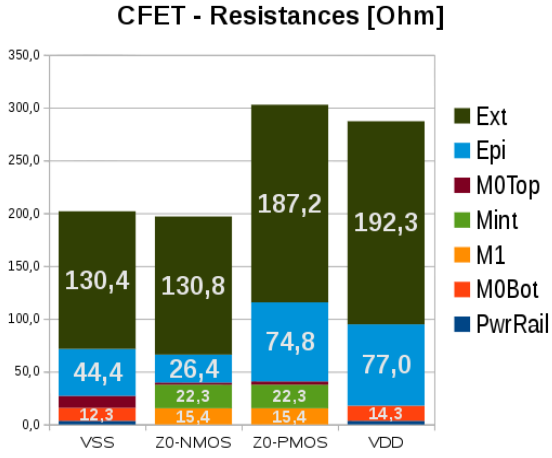






FEOL resistances





Multi-scale self-heating

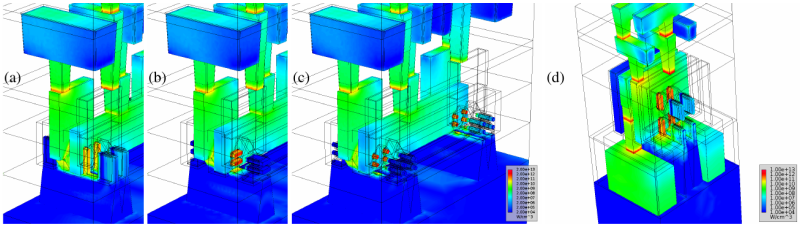


Fig. 9. Average heat generated during one 7 GHz and 1 V pulse of an inverter for (a) FinFET, (b) NS, (c) NW, and (d) CFET technology; As FinFET has better performance and draws more power, more heat is generated compared to NS and NW. Considerable heat contribution arises in the BEOL TiN barriers.

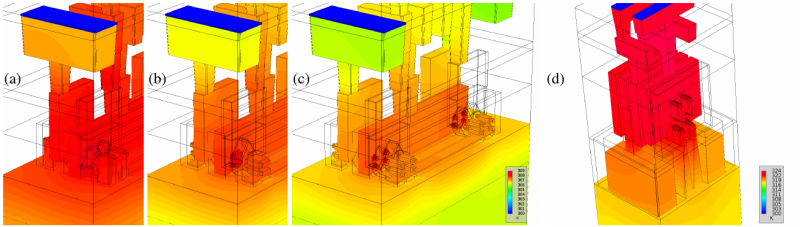


Fig. 10. Temperature in an inverter due to power as dissipated in Fig. 9; Maximum temperature is similar for FinFET (a), NS (b), and NW (c). The slightly higher-powered FinFET distributes heat in the whole cell, contrary to NS and NW. The CFET (d) faces a serious heat challenge due to the high power density.

Modules – summary

- Layout-based structrue generation
  - Rapid prototyping
  - Process-flow awareness
- Device simulation
  - Steady-state, transient, AC
  - Reliability
  - What about calibration?
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