10th International MOS-AK Workshop
Dec. 6, 2017 Silicon Valley

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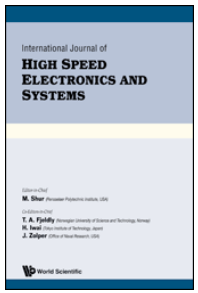

Contact: wladek@mos-ak.org

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Over two decades of MOS-AK in brief

MOS-AK R&D Association

15 subsequent MOS-AK modeling workshops
at ESSDERC/ESSCIRC Conferences

27 international MOS-AK modeling workshops
in Europe, India, USA and China (plans for Brazil)

16 special compact modeling sessions
at MIXDES Conference

50+ active sponsors and technical program promoters

350+ MOS-AK technical CM papers and posters
(available on line www.mos-ak.org)

4 modeling MOS-AK modeling books
http://www.mos-ak.org/books/

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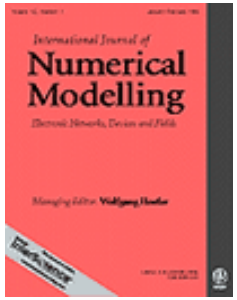
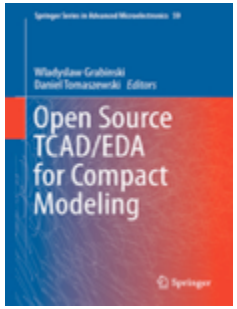
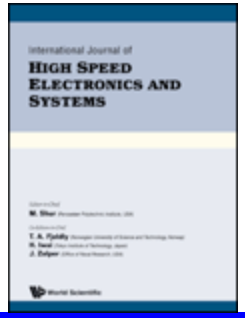
MOS-AK: Recent Publications



Wladek Grabinsk(editor), Mike Brinson, Paolo Nenzi, Francesco Lannutti, Angelos Antonopoulos, Nikolaos Makris and Matthias Bucher
Open source circuit simulation tools for RF compact semiconductor device modelling JNM2013



Open Source CAD for Compact Modeling
Editors: W. Grabinski and D. Tomaszewski
Publisher: Tom Spicer
1st Edition, 2017,
Hardcover; ISBN: xxx-xx-xxx-nnnn-n



Postworkshop publications:
Selected best MOS-AK technical presentation will be recommended for further publication in a special compact modeling issue of the **International Journal of High Speed Electronics and Systems** (IJHSES)

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ESSDERC Track 4: Device and Circuit Compact Modeling

Tuesday September 12, 2017 (11:00-12:20)

Cross-Domain Compact Modelling

Chair: Wladek Grabinski - MOS-AK; Cristell Maneux − LIMS;

[1] *INVITED*: SPICE Modeling in Verilog-a: Successes and Challenges
Colin McAndrew

[2] SPICE Modeling of Light Induced Current in Silicon with 'generalized' Lumped Devices
Chiara Rossi, Pietro Buccella, Camillo Stefanucci, Jean-Michel Sallese

[3] Total Ionizing Dose Effects on Analog Performance of 28 nm Bulk MOSFETs
Chun-Min Zhang, Farzan Jazaeri, Alessandro Pezzotta, Claudio Bruschini, Gulio Borghello, Serena Mattiazzo

Tuesday September 12, 2017 (14:00-15:20)

Parameter Extraction

Chair: Thierry Poiroux - CEA; Marco Bellini − ABB;

[4] Nanometer CMOS Characterization and Compact Modeling at Deep-Cryogenic Temperatures
Rosario Marco Incandela, Lin Song, Harald Homulle, Fabio Sebastiano, Edoardo Charbon, Andrei Vladimirescu

[5] Cryogenic Characterization of 28 nm Bulk CMOS Technology for Quantum Computing
Arnout Beckers, Farzan Jazaeri, Andrea Ruffino, Claudio Bruschini, Andrea Baschirotto, Christian Enz

[6] A New Method for Junctionless Transistors Parameters Extraction
Renan Trevisoli, Rodrigo Doria, Michelly de Souza, Sylvain Barraud, Marcelo Pavanello

[7] Avalanche Compact Model Featuring SiGe HBTs Characteristics Up to BVCBO
Mathieu Jaoul, Didier Céli, Cristell Maneux, Michael Schröter, Andreas Pawlak

Tuesday September 12, 2017 (16:40-18:00)

Modelling of Emerging Devices

Chair: Jean-Michel Sallese - EPFL; Daniel Tomaszewski - ITE;

[8] Equivalent Circuit Model for the Electron Transport in 2D Resistive Switching Material Systems
Enrique Miranda, Chengbin Pan, Marco Villena, Na Xiao, Jordi Suñe, Mario Lanza

[9] Analytical Drain Current Model for Schottky-Barrier CNTFETs
Igor Bejenari, Michael Schroter, Martin Claus

[10] A General Circuit Model for Spintronic Devices Under Electric and Magnetic Fields
Meshal Alawein, Hossein Fariborzi

[11] Compact Physical Model of a-IGZO TFTs for Circuit Simulation
Matteo Ghittorelli, Fabrizio Torricelli, Carmine Garripoli, Jan-Laurens van der Steen, Gerwin Gelinck, Sahel Abdinia

Wednesday September 13, 2017 (14:20-15:40)

Traps and Noise

Chair: Benjamin Iniguez - URV; Sadayuki Yoshitomi - Toshiba;

[12] Modeling of Dynamic Trap Density Increase for Aging Simulation of Any MOSFET Circuits
Mitiko Miura-Mattausch, Hidenori Miyamoto, Hideyuki Kikuchihara, Dondee Navarro, Tapas K. Maiti, Nezam Rohbani

[13] Comprehensive Compact Electro-Thermal GaN HEMT Model
Muhammad Alshahed, Mina Dakran, Lars Heuken, Mohammed Alomari, Joachim Burghartz

[14] Trap-Assisted Carrier Transport Through the Multi-Stack Gate Dielectrics of HKMG nMOS Transistors: a Compact Model
Apoorva Ojha, Nihar Ranjan Mohapatra

[15] A New Verilog-a Compact Model of Random Telegraph Noise in Oxide-Based RRAM for Advanced Circuit Design
Francesco Maria Puglisi, Nicolò Zagni, Luca Larcher, Paolo Pavan

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Technical Presentations

T_0 Welcome and MOS-AK Workshop Opening
Hany Elhak and Wladek Grabinski*
Cadence (US) and *MOS-AK (EU)

T_1 Verilog-A debug tool: AHDL Lint
Jushan Xie, Qingping Wu, Art Schaldenbrand, Andre Baguenier; Cadence (US)

T_2 A Complete Learning-Based Semiconductor Parametric Testing and Device Modeling Ecosystem, from Probing to Simulation
Yanfeng Li, Miao Li, Jian Yao, Riko Radojcic
Platform Design Automation, Inc (CN)

T_3 Generation of HICUM/L2 and HICUM/L0 Geometry Scalable Model Libraries
Didier Celi; STM (F)

T_4 SOI technology platforms for 5G: opportunity of collaboration
Ionut Radu; SOITEC (F)

T_5 An Overview of the HiSIM SOI/SOTB Compact Models
Marek Mierzwinski*, Dondee Navarro**, and Mitiko Miura-Mattausch**
*Keysight Technologies (US), **Hiroshima University (J)

T_6 Featured Circuit Simulation Using SMARTSPICE Compact Models and Verilog-A
Andrei Pashkovich and Bogdan Tudor; SILVACO (US)

T_7 Compact Model Requirements for TCAD Based DTCO
Asen Asenov Glasgow University and Synopsis

T_8 Enablement of compact models for ultra-scaled CMOS technologies
Dmitry Yakimets, Pieter Schuddinck, Doyoung Jang, Marie Garcia Bardon, Neha Sharan, Bertrand Parvais, Praveen Raghavan, and Anda Mocuta
imec (B)

T_9 Rapid Co-optimization of Processing & Circuit Design to Overcome Carbon Nanotube Variations
Gage Hills, Jie Zhang, Max Shulaker, Chi-Shuen Lee, Hai Wei, Arjun Balasingam, H.-S. Philip Wong, Subhasish Mitra Uni.Stanford (US)

T_10 FOSS/H Tools for Compact Modeling
Wladek Grabinski MOS-AK (EU)

T_11 A Normally-on MOSFET Compact Model based on Surface Potential Description
Dondee Navarro, Takahiro Iizuka, Takuya Umeda, Yoko Hirano, Hideyuki Kikuchihara, Mitiko Miura-Mattausch, and Hans Jürgen Mattausch
Uni.Hiroshima (J)

T_12 Aging simulation with variation of several model parameters
Klaus-Willi Pieper Infineon Technologies (D)

T_13 Reliability characterization of discrete devices and modeling circuit level ageing in advanced CMOS technologies
Tanya Nigam and Andreas Kerber GLOBALFOUNDRIES (US)

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MOS-AK: Upcoming Compact Modeling Events

- Spring **MOS-AK** Workshop
  - March 15-16, 2018, Strasbourg (F)
- 3rd Sino **MOS-AK** Workshop
  - June 2018 Beijing (CN)
- MIXDES & Special CM Session
  - June 21-23, 2018 Gdynia (PL)
- 16th **MOS-AK** at ESSDERC/ESSCIRC
  ESSDERC TPC Track 4: Compact Modeling
  - September 3-6, 2018 in Dresden (D)