

Layout-based Modeling Methodology for Millimeter-Wave MOSFETs

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Outline of Presentation

- **Motivation**
- **Proposed Methodology**
- **Results and Discussions**
- **Summary**

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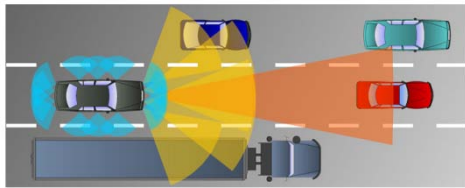
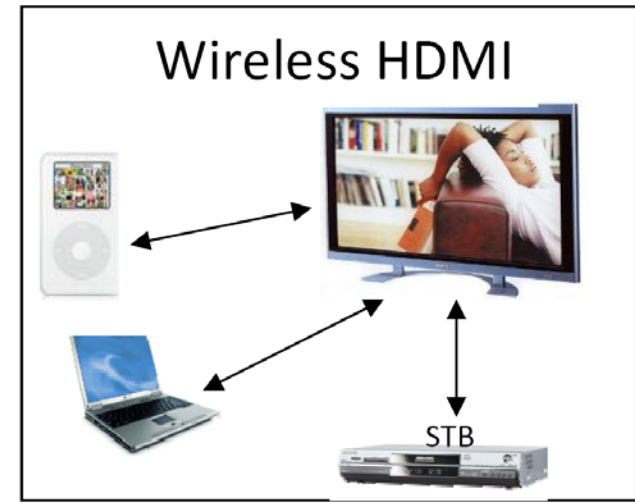
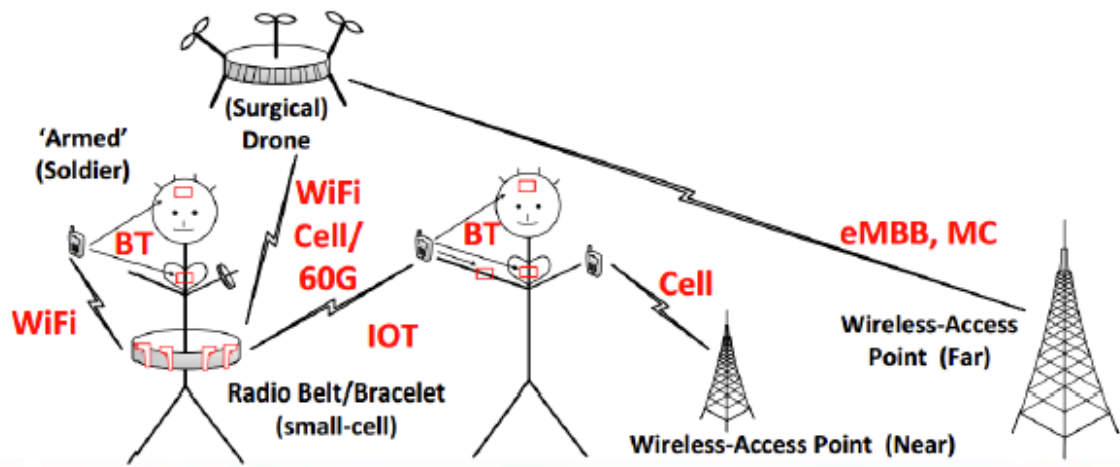


Motivation

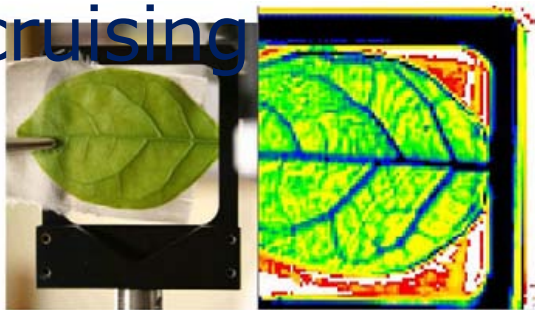
High performance CMOS millimeter-wave applications are emerging in endless stream

- **5G mobile Communication**
- **full-HD video streaming, and high speed wireless links at 60GHz**
- **77-GHz Radar for automatic cruising**
- **Millimeter-wave imaging system for fine resolution using 94-GHz band**

5G mobile Communication



Radar for automatic cruising



THz imaging system



Sync & Go



Motivation

- A versatile model for mm-wave device is still not available in many situations, so accurate device models for efficient CAD simulation is needed.
- The RF model provided by PDK usually targets at low gigahertz applications and does not account for the complex high frequency effects and parasitic effects.
- CMOS circuits are fabricated on a resistive lossy substrate, and parameters associated with substrate parasitics must be added to conventional models.

Motivation

- mm-wave transistors usually adopt a complex multi-finger layout.
- The challenge for modeling of mm-wave FETs mainly arises from that the model is limited to interpolated geometry range set by **the largest and smallest measured devices** due to unpredicted accuracy of extrapolation.
- It's extremely difficult to build a set of equations precisely covering all the parasitic capacitance, resistance of local metal wires, vias and contacts which connect a row of gate fingers, as well as from substrate loss over wide geometry range.

Motivation

- We made the assessment of NMOS multifinger transistors by TSMC 65nm, the mean-square error of Y-parameters between simulation and measurement results are shown.
- The error is a little bit striking.

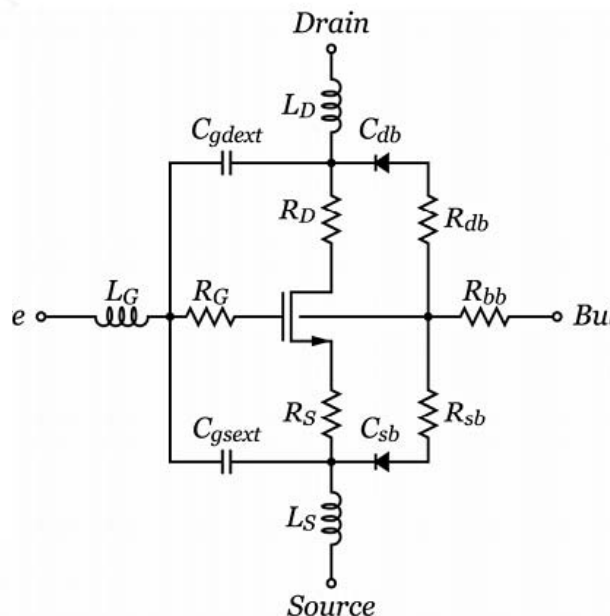
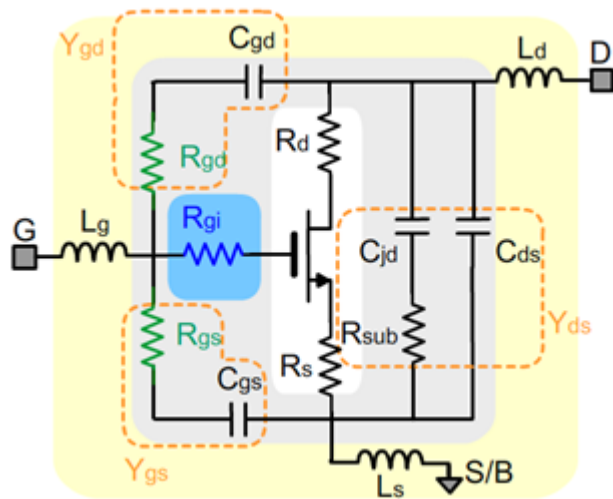
| | | | | | | | | |
|---------------------|------|-------|-------|-------|-------|-------|-------|-------|
| Lr(μm) | 0.06 | 0.06 | 0.06 | 0.06 | 0.06 | 0.06 | 0.12 | 0.24 |
| Wr(μm) | 0.6 | 1 | 4 | 6 | 4 | 4 | 4 | 4 |
| Nr | 16 | 16 | 16 | 16 | 4 | 32 | 16 | 16 |
| Real(Y11)% | 45.9 | 53.4 | 46.1 | 33.2 | 26.5 | 35.2 | 31.1 | 14.8 |
| Real(Y12)% | 45.4 | 188.7 | 372.0 | 750.4 | 124.1 | 348.4 | 396.7 | 420.0 |
| Real(Y21)% | 5.5 | 4.1 | 9.1 | 17.1 | 4.2 | 23.6 | 4.8 | 7.3 |
| Real(Y22)% | 17.9 | 21.4 | 13.2 | 9.8 | 15.9 | 11.9 | 16.7 | 6.1 |
| Imag(Y11)% | 10.9 | 9.3 | 8.6 | 14.5 | 9.9 | 11.4 | 7.2 | 13.9 |
| Imag(Y12)% | 8.6 | 10.4 | 9.3 | 11.6 | 13.0 | 9.0 | 19.1 | 40.7 |
| Imag(Y21)% | 25.9 | 39.7 | 52.7 | 45.5 | 27.1 | 54.9 | 27.7 | 9.2 |
| Imag(Y22)% | 7.3 | 6.9 | 64.7 | 116.3 | 9.4 | 146.2 | 17.4 | 4.1 |

TSMC65nm RF NMOS 0.1~30.1GHz, the mean-square error of Y-parameters between simulation results and measurement.

Motivation

Most of previous models focused on a fixed model, which is usually based on the BSIM enhanced by parasitic sub-circuit.

Designers in many situations have to build a model of their own before diving into the design of integrated mm-wave circuit.



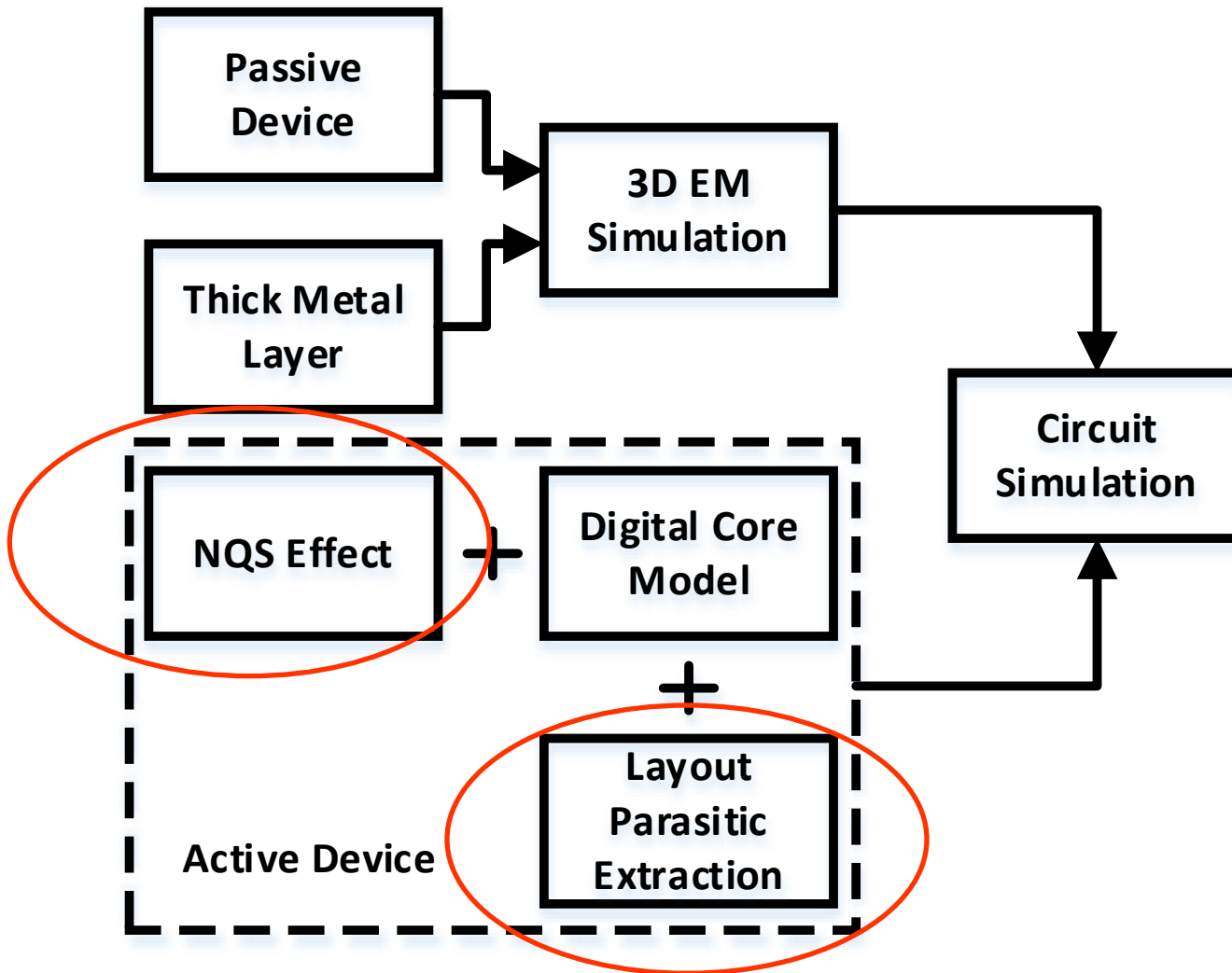
Motivation

- In this work, a novel modeling methodology for millimeter-wave MOSFETs based on **standard digital core model** is proposed and investigated.
- This modeling methodology takes into account the **layout effect** and **NQS effect**.
- The proposed modeling methodology is compared with the measured data and good accuracy is achieved for a standard 90nm and 65nm CMOS technology.
- This proposed model has been successfully applied in 60GHz LNA design.

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Proposed Modeling Methodology



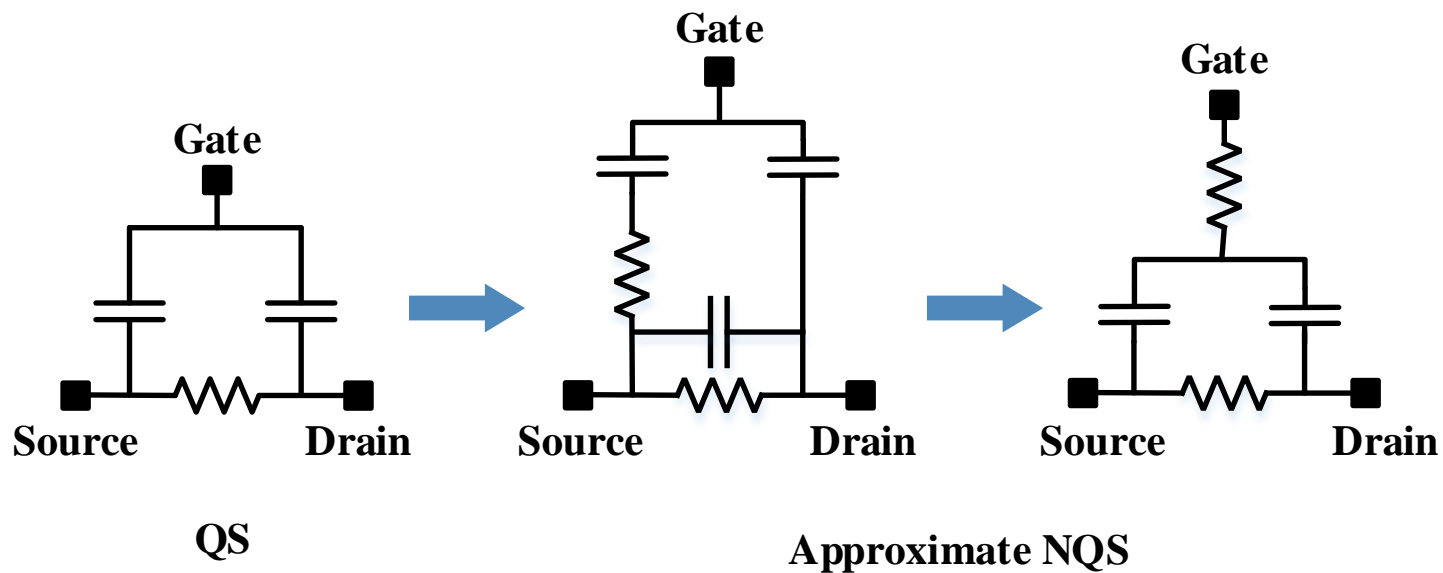
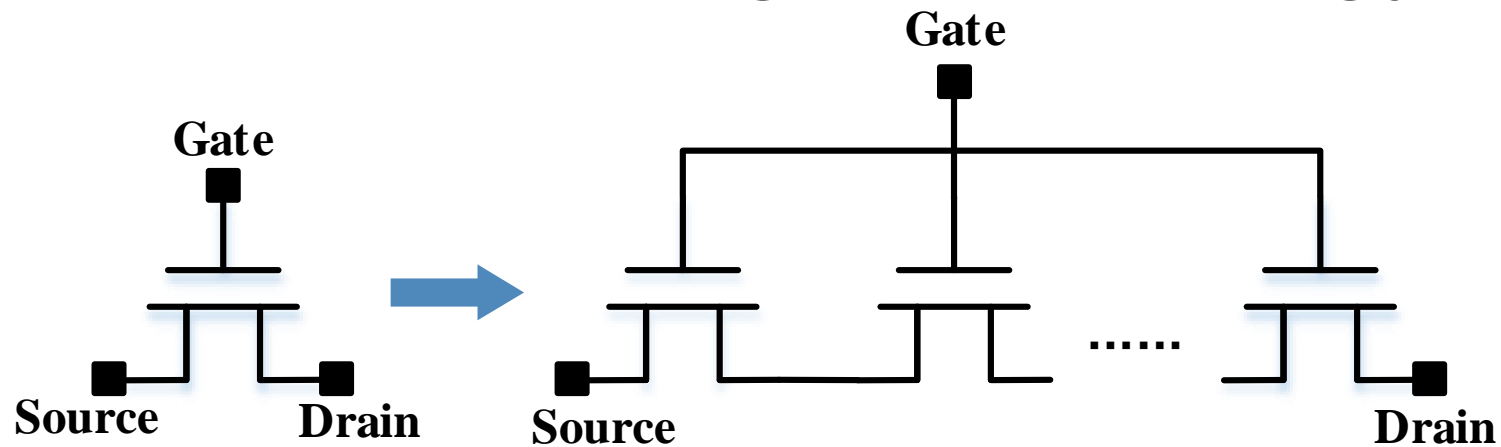
Flow chart of the proposed modeling methodology₂



Proposed Modeling Methodology

- The standard core model aiming for digital circuit analysis is adopted directly. The core nonlinear elements such as gate drain capacitance, gate-source capacitance, output conductance, output transconductance, etc. can be described by BSIM.
- Extrinsic parasitic linear components introduced by device interconnections and related vias can be extracted by using Calibre xRC.
- NQS effect related nonlinear MOSFET characteristics are far more difficult to be determined for mm-wave multi-finger MOSFETs.

Proposed Modeling Methodology



It is first necessary to take into account the distributed nature of the device structure along both its channel length and channel width.



Proposed Modeling Methodology

- For a one-fingered device, the intrinsic gate resistance $R_{g,i}$ is given by

$$R_{g,i} = \frac{R_{g,sq}}{3} \frac{W}{L}$$

Where $R_{g,sq}$ is the DC sheet resistance of the gate material, W is the width of the device, and L is the length of the channel region[1]. The factor 3 accounts for the distributed nature of the intrinsic gate region[2].

- $R_{g,i}$ increases in HF regime, in this work, it can be determined by Calibre extraction for simpliness.

[1] Andrey V. Grebennikov, and Fujiang Lin, An efficient CAD-oriented large-signal MOSFET model, VOL. 48, NO. 10, P1732(2000)

[2] E. Abou-Allam and T. Manku, "A small signal MOSFET model for radio frequency IC applications," *IEEE Trans. Computer-Aided Design*, pp. 437–447, May 1997



Proposed Modeling Methodology

- R_{gs} accounts for the fact that channel charge cannot instantaneously respond to changes in the gate-source voltage.
- The signal applied to the gate suffers an additional equivalent gate resistance from the distributed channel resistance.
- Since the channel conductance seen by the source is related to g_m , we would expect that the channel resistance (R_{gs}) is proportional to $1/g_m$.

$$R_{gs} \propto \frac{1}{g_m}$$

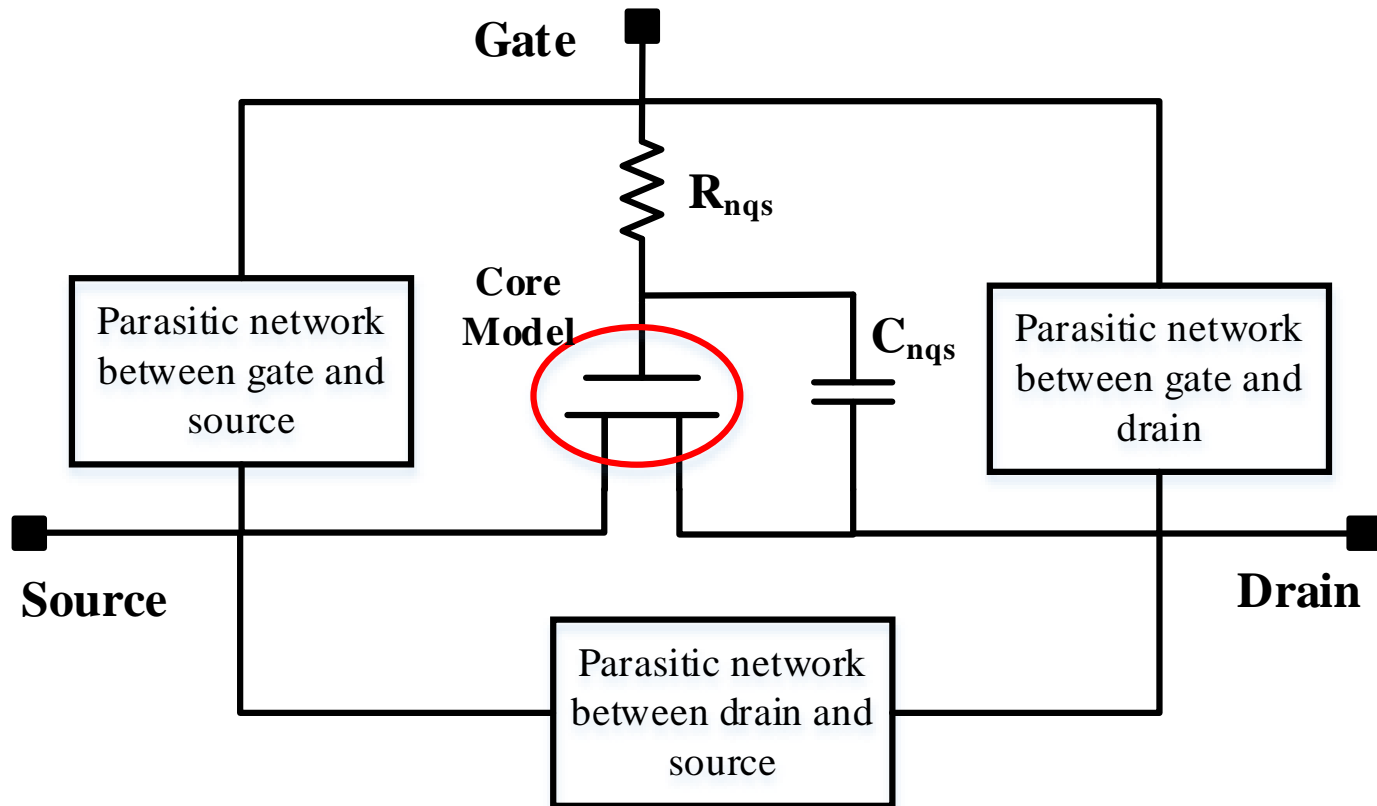
- R_g consists of two parts: the $R_{g,i}$, contributed by the gate resistance and the $R_{g,nqs}$ due to channel charging resistance.



Proposed Modeling Methodology

- The transconductance delay τ is modeled by two ways:
 - included by multiplying g_m by $\exp(j\omega\tau)$.
 - The transconductance delay can also be represented by the transcapacitance C_m .
- It has been known that BSIM model includes an NQS option and has been verified with measurements for devices.
- The NQS effect will equivalently introduce a transcapacitance between the drain and gate as the displacement current from C_{gd} can cancel partially the output current, which is equivalent to an increased delay to the signal.

Proposed Modeling Methodology

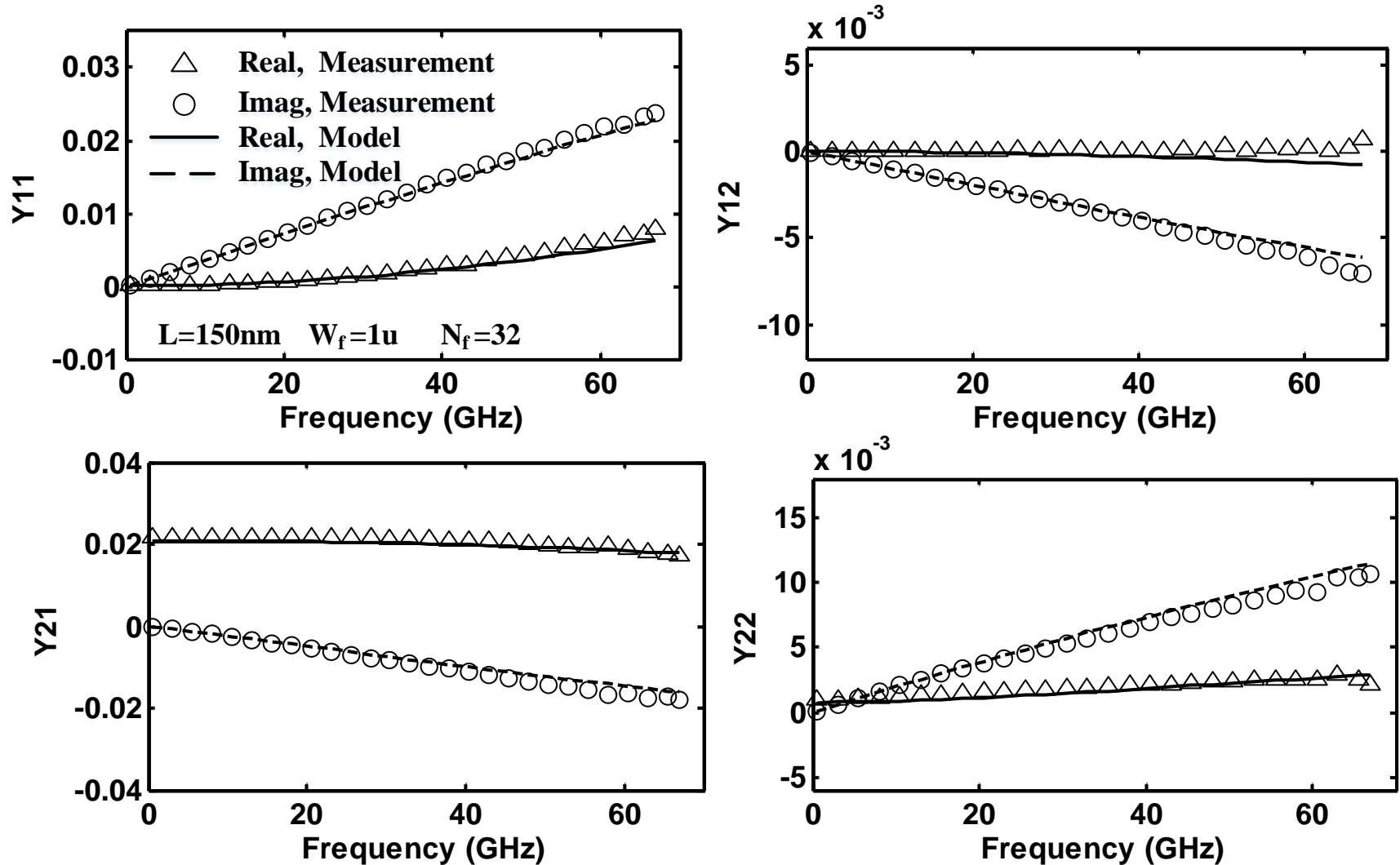


typical equivalent circuit model for mm-wave transistor proposed in this work, after the extraction, we achieve: the $R_{nqs}=1/5g_m$, $C_{nqs}=1/10C_{gg}$.

Outline of Presentation

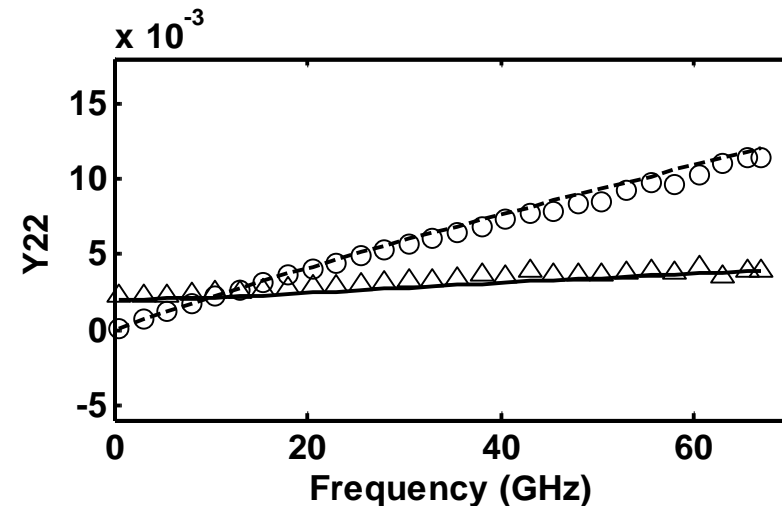
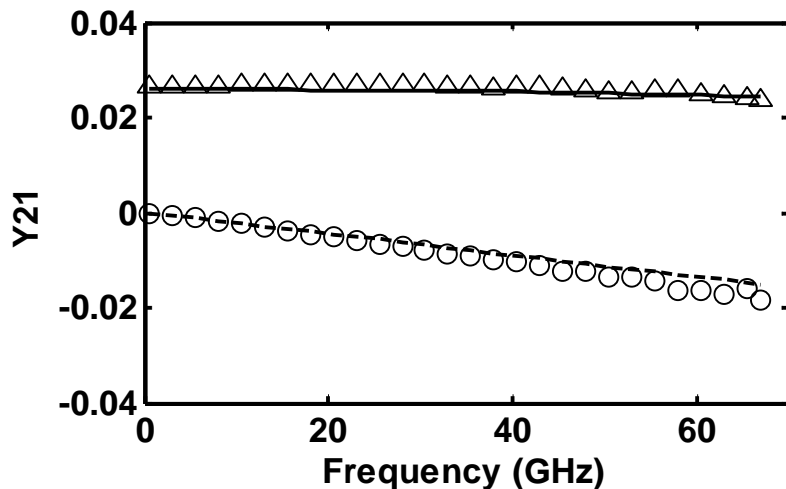
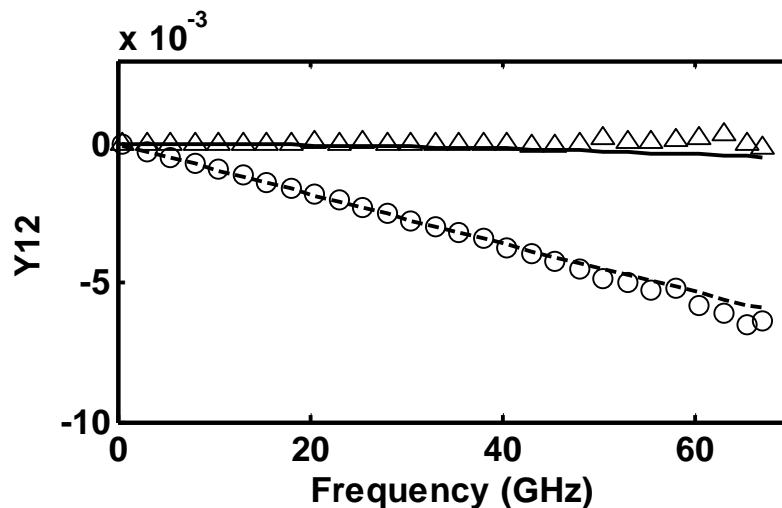
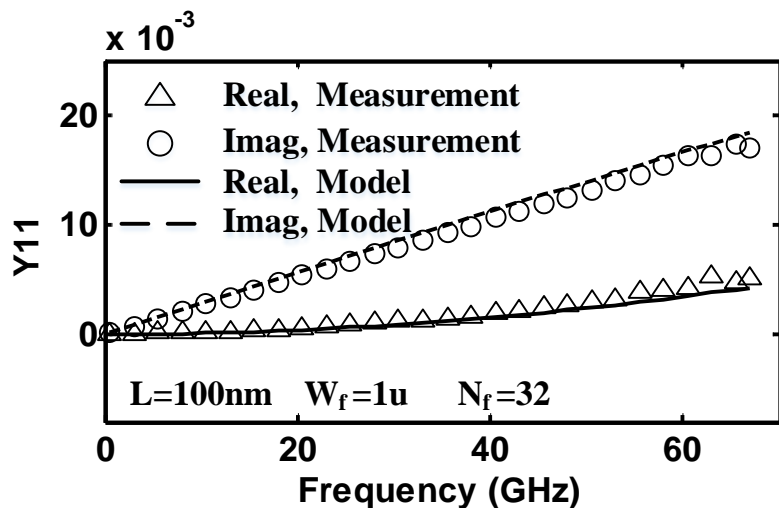
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Results and Discussion



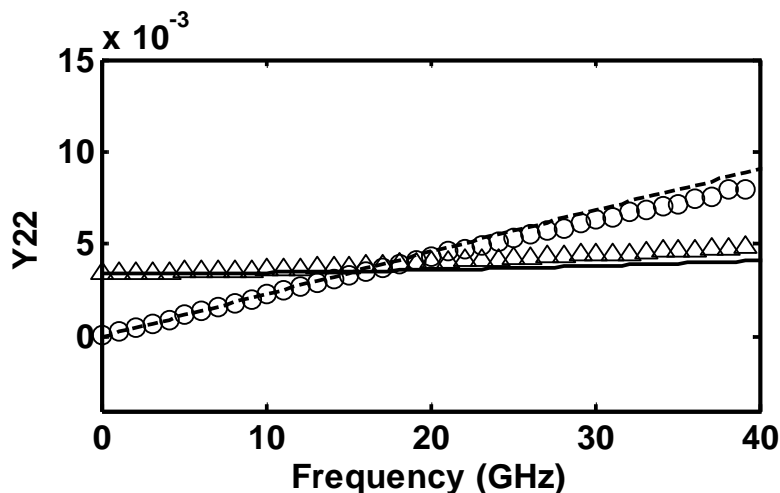
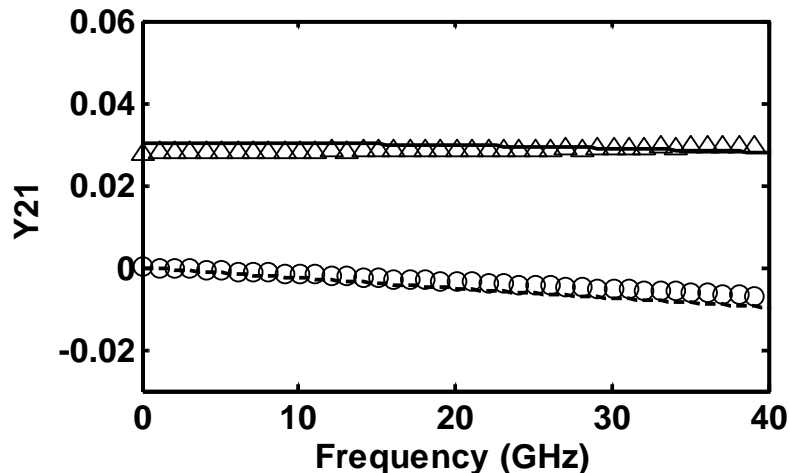
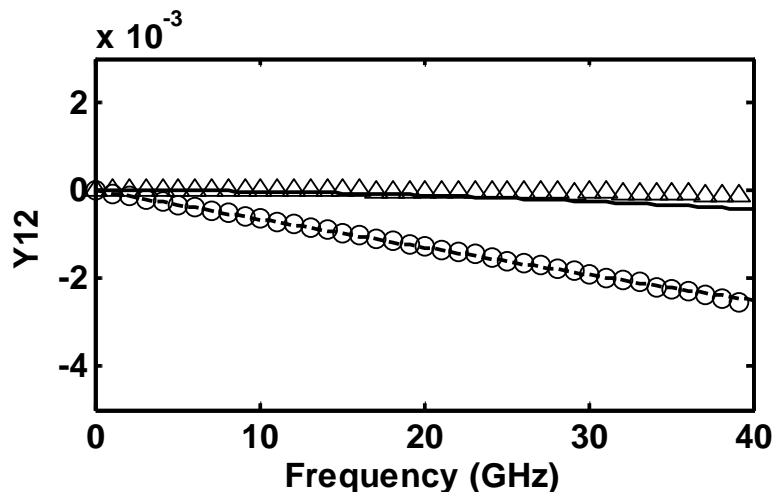
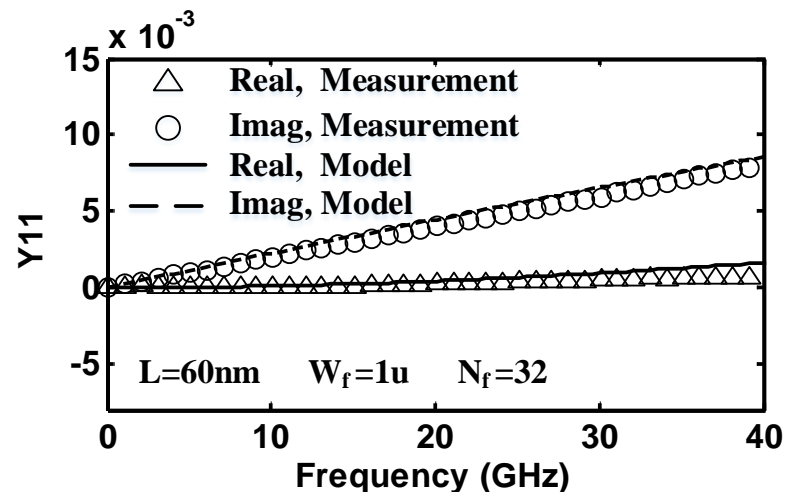
Measured and modeled Y-parameters for MOSFETs with $L=150\text{nm}$, $W_f=1\mu$ and $N_f=32$ (TSMC 90nm).

Results and Discussion



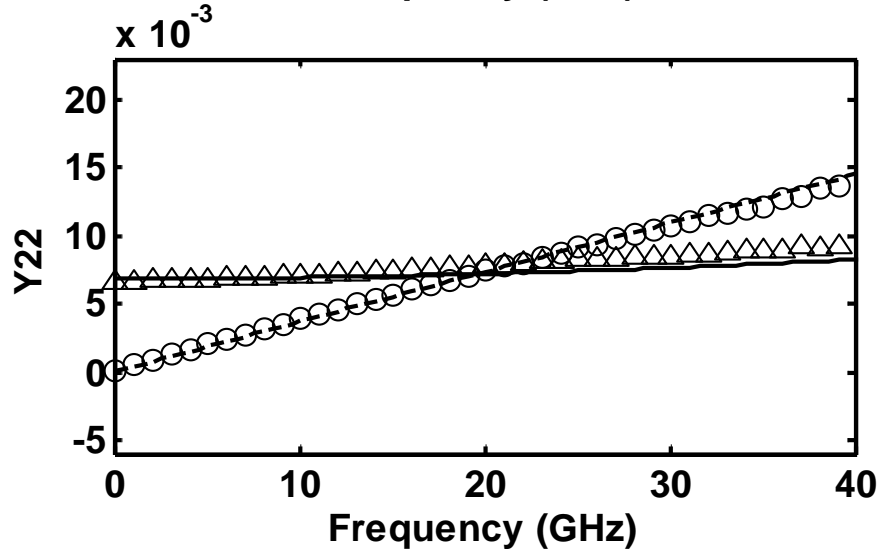
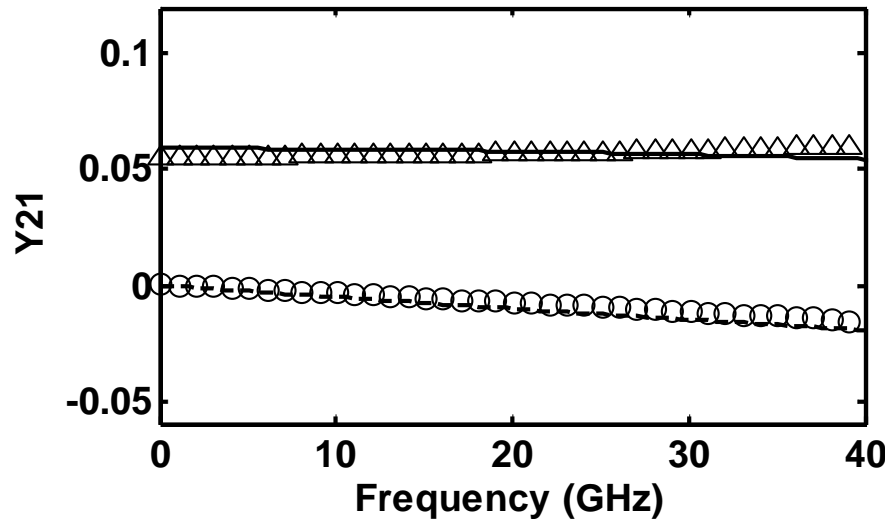
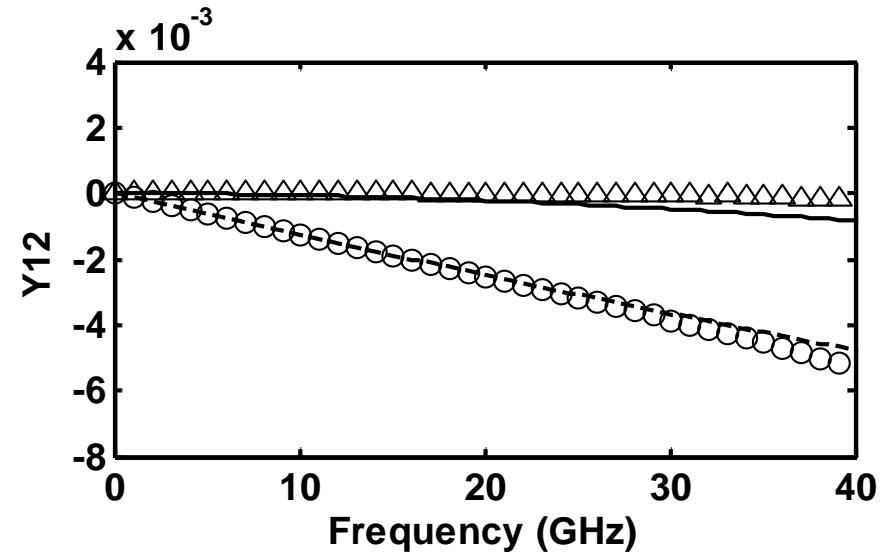
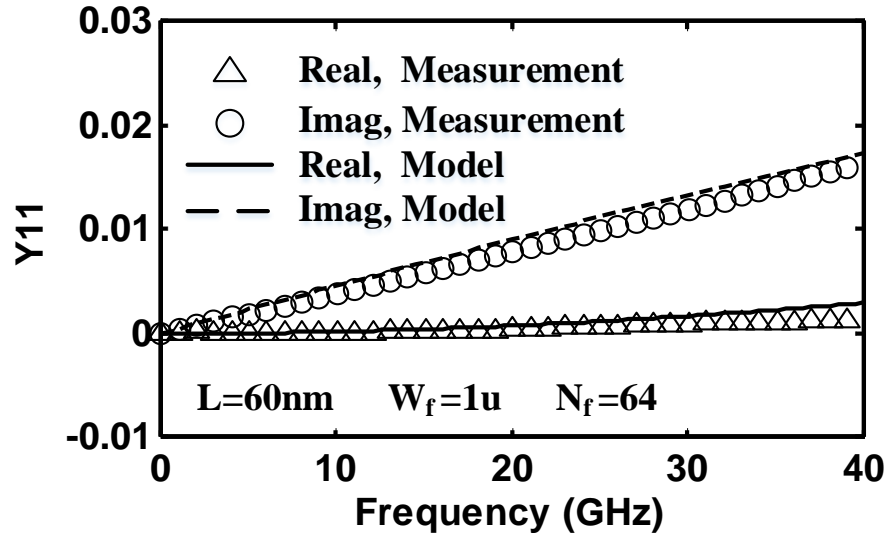
Measured and modeled Y-parameters for MOSFETs₂₁ with $L=100\text{nm}$, $W_f=1\mu$ and $N_f=32$ (TSMC 90nm)

Results and Discussion



Measured and modeled Y-parameters for MOSFETs with $L=60\text{nm}$, $W_f=1\mu$ and $N_f=32$ (SMIC 65nm).

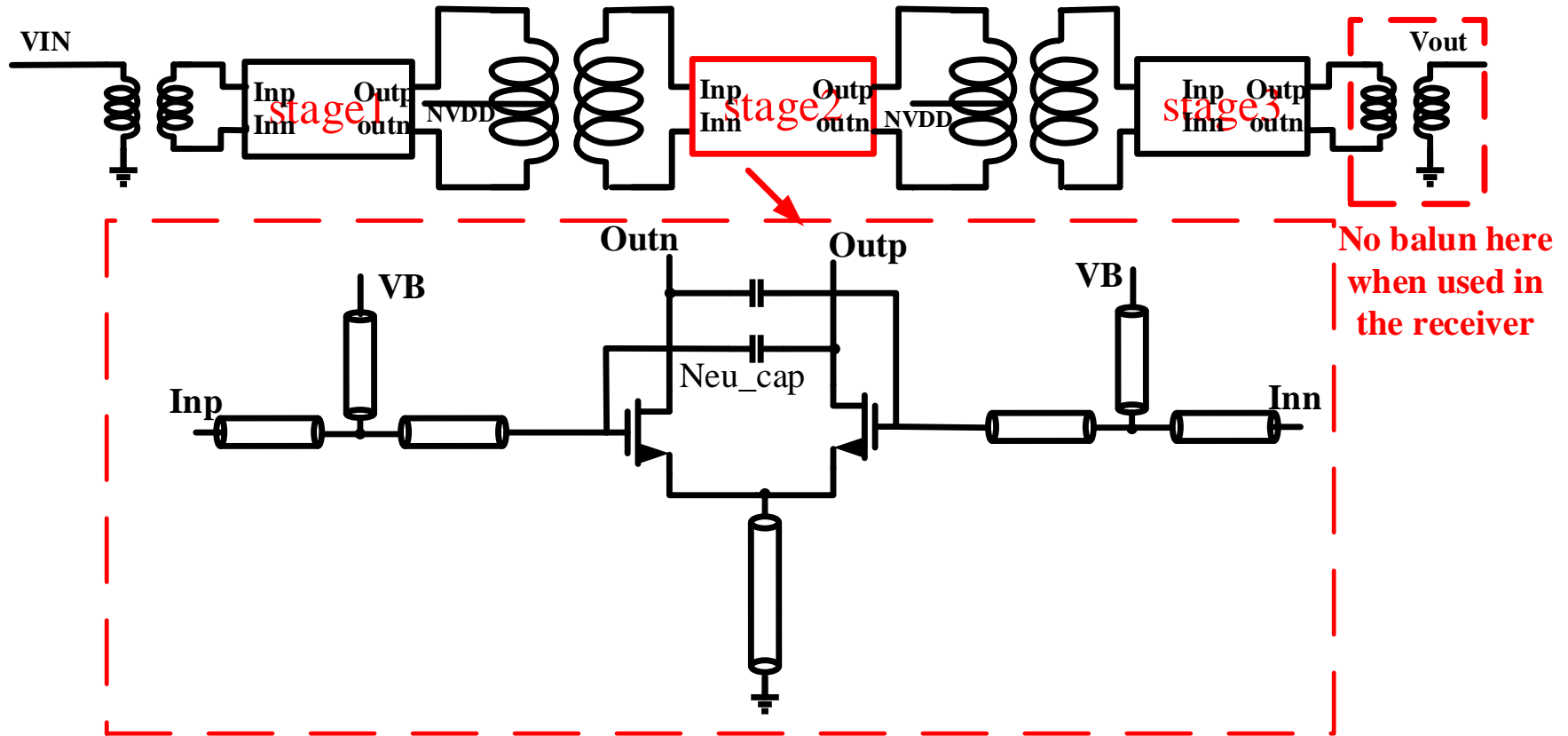
Results and Discussion



Measured and modeled Y-parameters for MOSFETs with $L=60\text{nm}$, $W_f=1\mu$ and $N_f=64$ (SMIC 65nm). 23

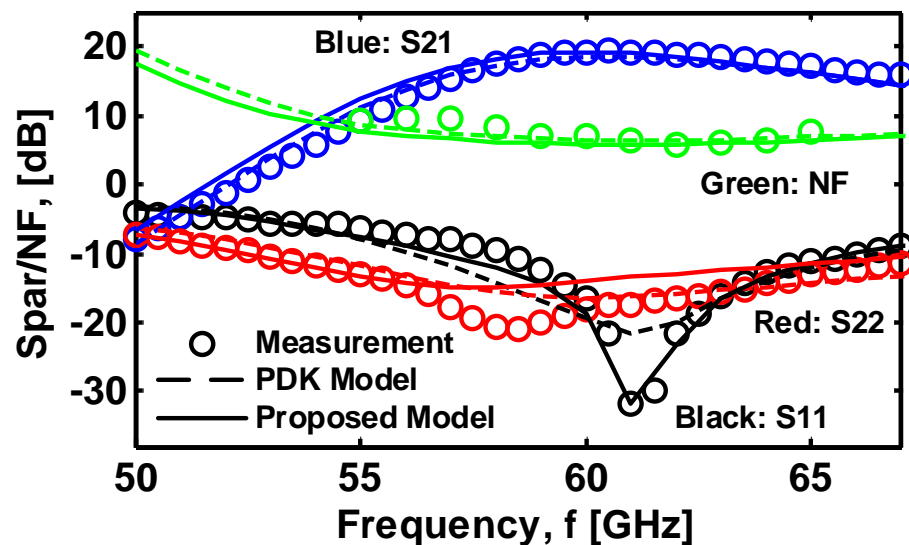
Results and Discussion

The proposed modeling methodology is also used to design a 60GHz low noise amplifier (LNA).

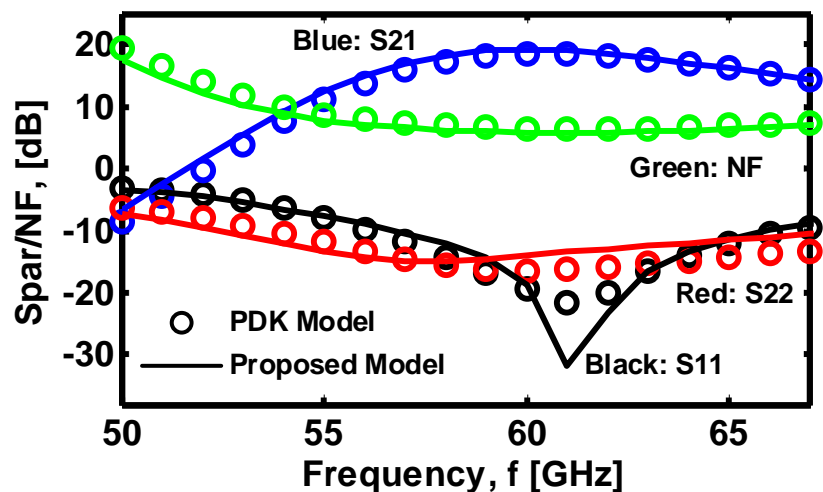


three stage differential structure, transformer are used for interstage match

Results and Discussion



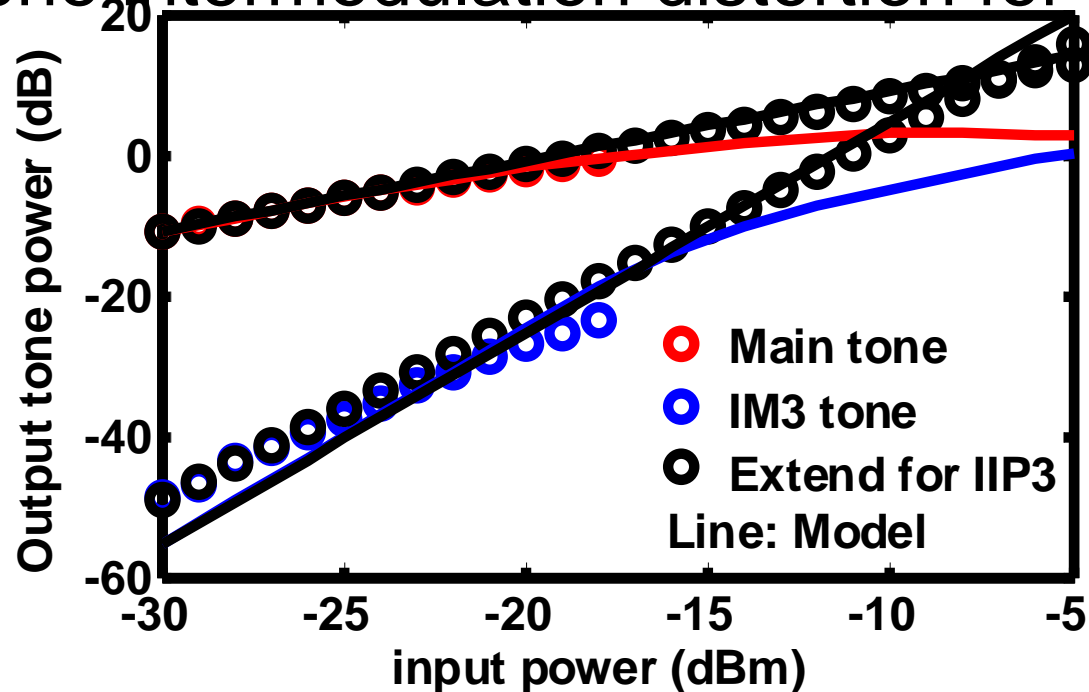
The measurements is in a good agreement with the modeled results with a 0.5 GHz of frequency mismatch. The noise figure (NF) is also well-predicted by the model.



Measured and modeled S-parameters and NF for LNA.

Results and Discussion

Two-tone intermodulation distortion for LNA.



The measured and modeled IIP3 is -7dBm and -8dBm respectively. The input and output power is shown and the measured 1-dB compression point is -16dBm which matches the predicted value based on the proposed modeling methodology. Again we got the satisfied results.

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Summary

- A novel modeling methodology for millimeter-wave MOSFETs based on standard digital core model is proposed and investigated.
- This method takes into account the layout effect and NQS effect, which play a significant role in the millimeter-wave scope.
- The proposed method is compared with the measured data and good accuracy is achieved for a standard 90nm and 65nm CMOS technology.
- This proposed model has been successfully applied in 60G LNA design.
- When you have trouble in choosing HF transistor model, you can try this method.

Thanks for attention!