DOMINO - A European Modelling Initiative for Organic and Oxide Thin Film Transistors

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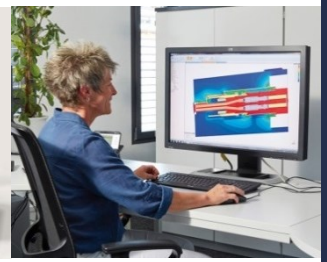
AdMOS Company Information

- AdMOS was founded in 1997 and is located in the high tech region of Stuttgart in Germany. With our team of highly qualified engineers we are focused on:
  - Software development of tools for model parameter extraction of CMOS and other devices.
  - Services around modeling and simulation of complex devices and systems.
  - Design support for RF and high speed devices.
  - Flicker Noise Measurement Systems.



Motivation for TFT compact model research

- The $3Bn printed electronics industry is expected to grow to $45Bn by 2021 and over $300Bn by 2027 (IDTechEx), with over one-third of the market being logic & memory.

- Printed and flexible logic will need to progress from the simple functionality currently possible commercially (fewer than 100 transistors/circuit) to more complex capabilities (>1,000 transistors/circuit).

- It will be essential that these printed circuits are produced at very low cost such that they become ubiquitous within consumer products, novelties, toys and security labels, in addition to higher-end uses such as military and defense

Motivation for TFT compact model research

- Optimised designs will allow efficient circuits to be fabricated, impacting directly on cost.

- However, printed and flexible thin, organic and large area electronics (TOLAE) circuit design is still limited due to:
  - the very small number of designers, usually only linked to technology providers
  - the lack of available complete compact device models to carry out accurate designs of TOLAE circuits.

- The design community at large need a user-friendly integration of high performance OTFT and oxide based semiconductor TFT compact models into industry standard Electronic Design Automation (EDA) circuit design tools to reduce design cycle duration

Project Scope of DOMINO

- Our project aims to fill the gap between printed and flexible TOLAE technology and design by developing organic and oxide based TFT compact model libraries which are:
  - highly predictive
  - generic
  - open-source
  - design-oriented

- They shall be integrated into commercial EDA environments for full large area low cost circuit design for novel printed and flexible applications.
- These model libraries will be released together with parameter extraction standard templates to assist in the fast transfer between initial prototype device measurements to full product design.
- Such a facility will open the opportunity for wide flexible electronics design.

Basic Project Facts of DOMINO

- Exchange of researchers between:
  - academic and industrial partners
  - different European countries

- Education of researchers:
  - Training Courses on Compact Modeling (TCCM),focusing on Flexible Electronics.
  - Two editions:
    - 2016 Tarragona/Spain
    - 2018 Paris/France
  - Online learning

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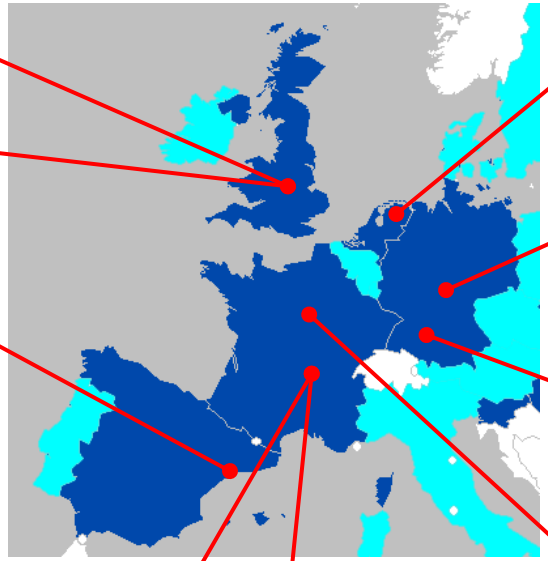
Project Participants

UNIVERSITY OF CAMBRIDGE

SILVACO

UNIVERSITAT ROVIRA i VIRGILI



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THM
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AdMOS

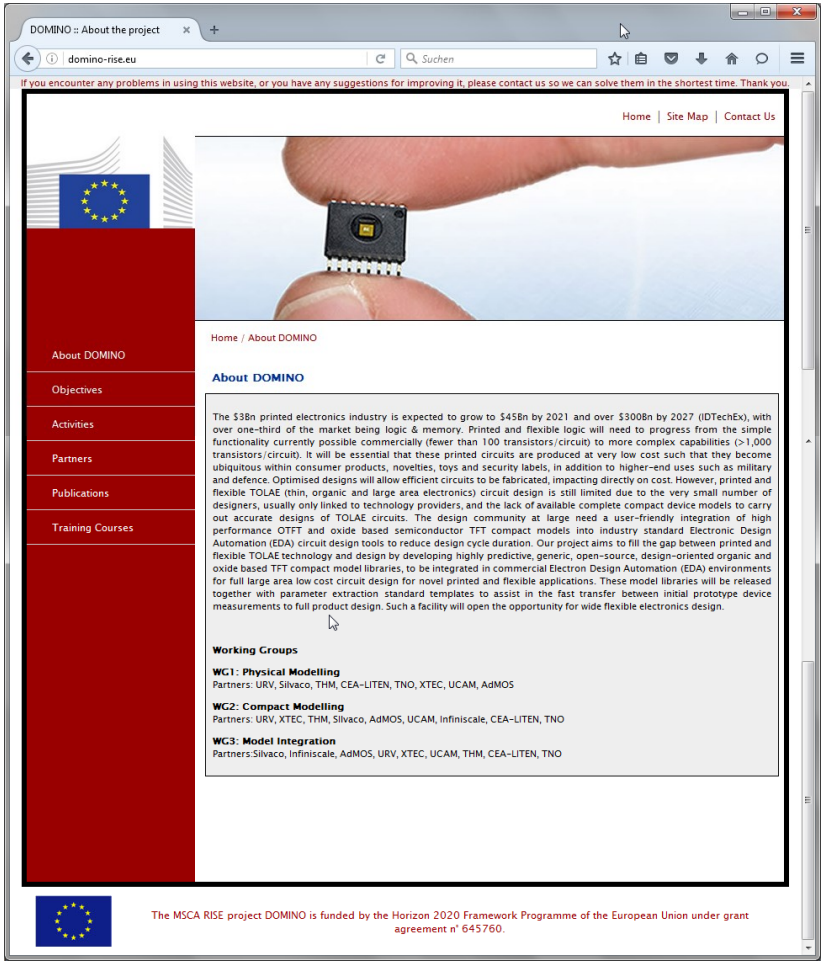
cea
DE LA RECHERCHE À L'INDUSTRIE

infiniscale

ÉCOLE POLYTECHNIQUE

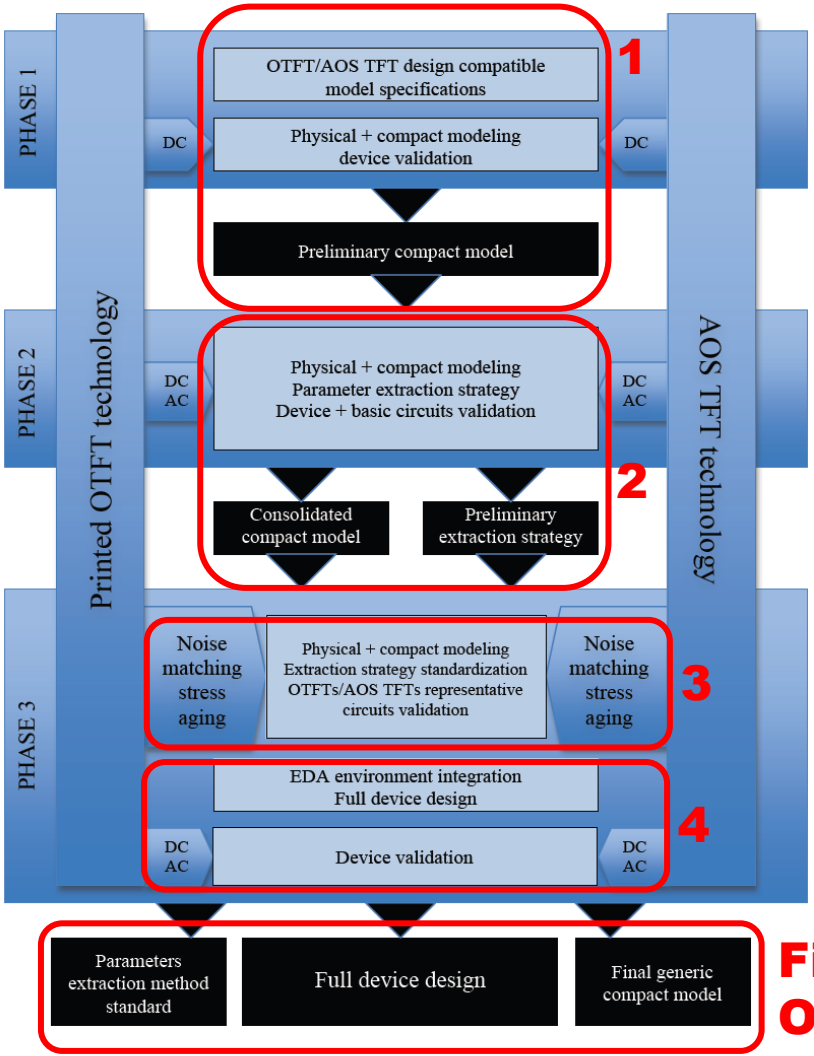
4 Universities, 3 Companies and 2 Research Institutes from 5 European Countries.

Project Web Site



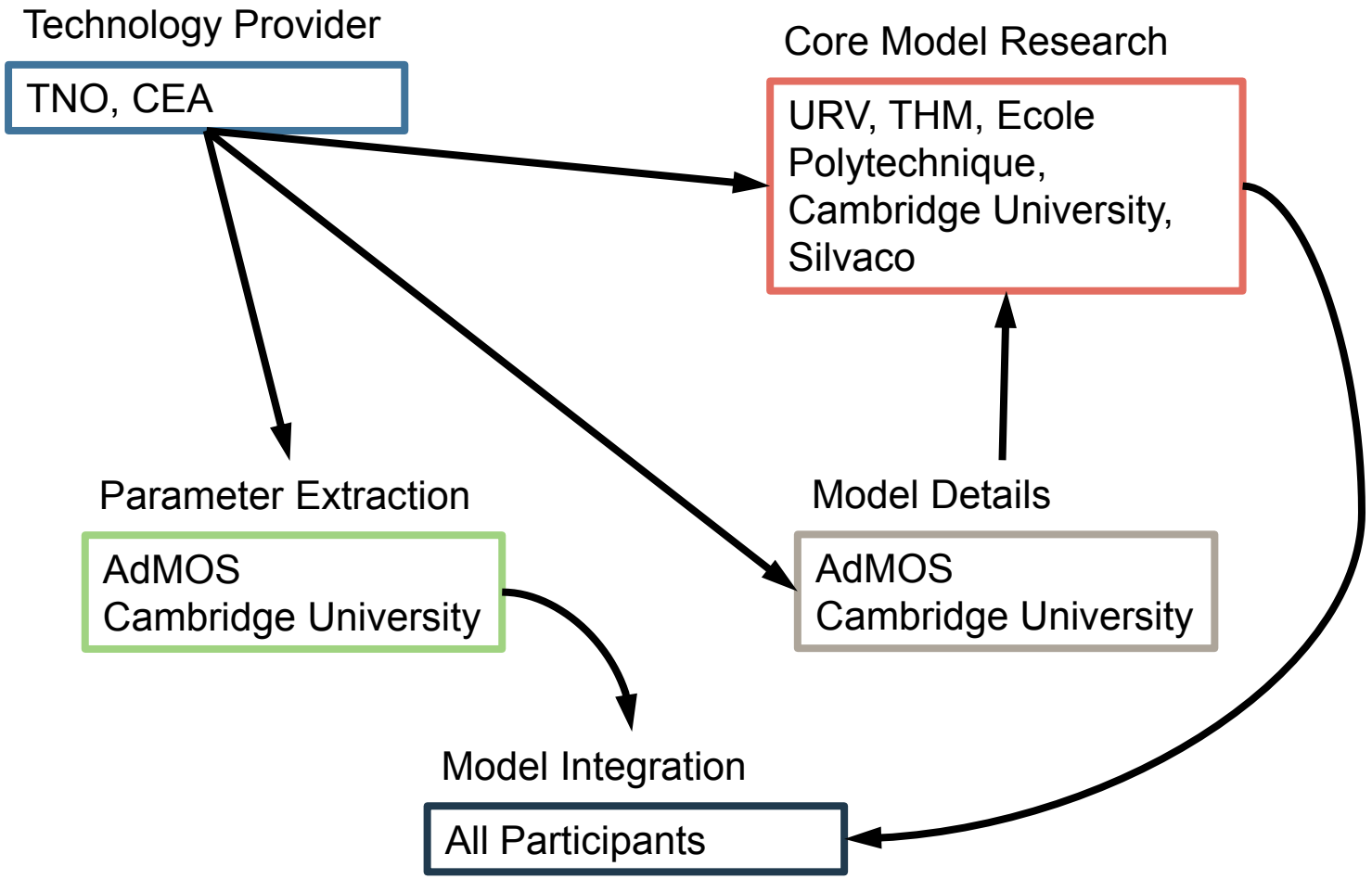
www.domino-rise.eu

Project Scope



Final Outcome

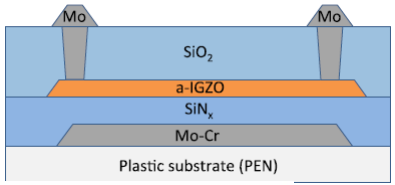
Example Research Work



Technology Provider: TNO and CEA

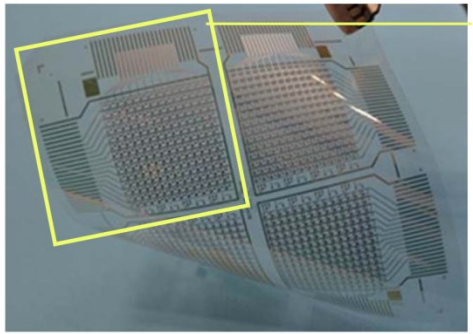
TNO Centre Holst

- Amorphous Indium-Gallium-Zinc-Oxide thin-film transistors (a-IGZO TFTs, AOS TFTs)
- Etch Stop Layer with SiN or SiO_2 gate dielectric



CEA-LITEN

- P-OTFT technologies for stand-alone active matrix for sensors addressing and display



Core Model : OTFTs

Physical DC equations for OTFTs (URV, THM, Silvaco, XTEC):

- Core model based on Variable Range Hopping transport, developed by URV and improved by XTEC.
- Charge-based model with threshold voltage calculation from physical parameters, and considering the charge at shallow traps, deep traps and interface states
- 2D injection model: physics-based modeling of source injection including 2D effects
- Bias-dependent resistance expression incorporated to a formulation based on Variable Range Hopping transport

Empirical model:

- developed by Infiniscale for a fast simulation of new FETd evices without having the need to wait for the explicit compact model development.

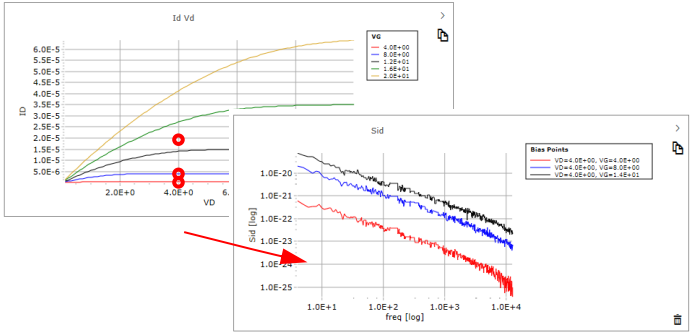
Core Model : AOS TFTs

Physical DC equations for AOS TFTs

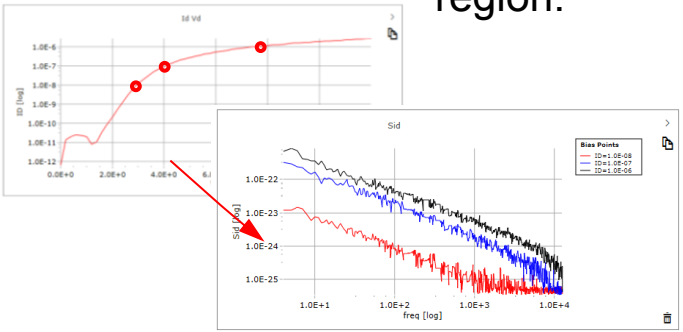
- Analytical core model, developed by URV and Silvaco, based on considering deep states (with exponential DOS) , tail states (with exponential DOS) and drift/diffusion transport of free carriers, with an improved model of channel length modulation.
- Alternative Mobility model based on Trap Limited Conduction (TLC) and percolation, with a Gaussian DOS. Final formulation similar to the above explained one. Developed by Cambridge University.
- Physical modeling and extraction method of the threshold voltage by Cambridge University

Model Details: Noise - AdMOS

Noise in saturation region.



Noise in subthreshold / linear region.



Strategy:

- Evaluate different OTFT and oxide TFT technologies to find out what noise components will be necessary in a compact model:
  - Flicker noise ✓
  - Channel noise is below the system noise floor
  - No burst or Random Telegraph Signal noise
- Next steps:
  - Include noise formulations into compact models in Verilog-A formulation and evaluate performance versus technologies and a wide range of dimensions.
  - Derive appropriate parameter extractions

Training Course on Compact Modeling (TCCM)

- 2 Training Courses on Compact Modeling are held during the project:
  - Tarragona, Catalonia. Spain, June 27-28, 2016
  - Paris, France, June 2018
- They consist of a set of lectures addressing relevant topics in the compact modeling of advanced electron devices.
- Most of the courses will target compact modeling issues applicable to many electron devices.
- In this edition, emphasis will be given on OTFTs and AOTFTs, the targets of the DOMINO project

Summary

- We could get insight into an joint European research project with the focus on compact simulation models for Amorphous Oxide TFT as well as Organic TFT.
- The outcome of this project is not only basic research but should be usable models for the design community of TFT based electronics.
- Therefore, the participation of device manufacturers, research focused universities and application oriented EDA companies can be a benefit to promote the new simulation models.

Thanks for your kind attention and many thanks to MOS-AK committee and simtac for the invitation to China !

Conference Presentations

[1] S. Jung et al. “Modeling Organic Field Effect-Transistors with Power-Law Dependent Mobility and Contact Resistance”, International Thin-Film Transistor Conference (ITC), Hsinchu, Taiwan, February 25-26 (2016)

[2] S. Jung et al., “Self-consistent Parameter Extraction Method for Organic-Field Effect Transistors with Powerlaw Dependent Mobility”, Materials Research Society Fall Meeting, Boston, USA, Nov 29-Dec 4 (2015)

[3] S. Jung et al. “N-type Organic Field-Effect Transistors with High Performance and Low Operation Voltage”, International Conference on Organic Electronics (ICOE), Erlangen, Germany, June 15-17 (2015)

[4] S. Jung, et al. “Fundamental Difference in the Electrical Characteristics of Organic Rectifying Diodes under Non-degenerate and Degenerate Regime Related with a Gaussian Density-of-States”, European Materials Research Society Spring Meeting (E-MRS), Lille, France, May 11-15 (2015) Young Scientist Award

[5] S. Jung et al. ,“Defining the Injection Barrier at Metal/Organic Semiconductor Interface with a Gaussian Density-of-States”, International Thin-Film Transistor Conference (ITC), Rennes, France, February 26-27 (2015)

[6] F. Hain, C. Lammers, F. Horst, F. Hosenfeld, B. Iniguez, A. Kloes. Continuous Charge-Based Current Model for Organic TFT Derived From Gaussian DOS. Proceedings ICOE 2015, Erlangen,2015

Journal Articles

[1] S. Jung et al., “A TIPS-TPDO-tetraCN Based n-Type Organic Field-Effect Transistor with a Cross-linked PMMA Polymer Gate Dielectric” (Under revision at Applied Materials and Interfaces)

[2] S. Jung et al., “Injection barrier at metal/organic semiconductor junction with a Gaussian density-of-states”, Journal of Physics D: Applied Physics 48, 395103 (2015).

[3] S. Lee and A. Nathan, “Conduction threshold in accumulation-mode IGZO thin film transistors,” Scientific Reports 6,22567 (2016).

[4] X. Cheng, S. Lee, G. Yao, and A. Nathan, “TFT compact modelling,” IEEE Journal of Display Technology (to appear).

[5] X. Cheng, S. Lee, and A. Nathan, “TFT Small Signal Model and Analysis,” IEEE Electron Device Letter (in revision).

[6] S. Lee and A. Nathan, “Physical definition of threshold voltage and related analysis in TFTs,” IEEE Electron Device Letter (submitted).

[7] O. Moldovan, A. Castro-Carranza, A. Cerdeira, M. Estrada, P. Barquinha, R. Martins, E. Fortunato, S. Mijalkovic, B. Iñiguez, “A Compact Model and Direct Parameters Extraction Techniques For Amorphous Gallium-Indium-Zinc-Oxide Thin Film Transistors,” Solid-State Electronics (revised version submitted)