A New Surface Potential-based Compact Model for IGZO TFTs in RFID Applications

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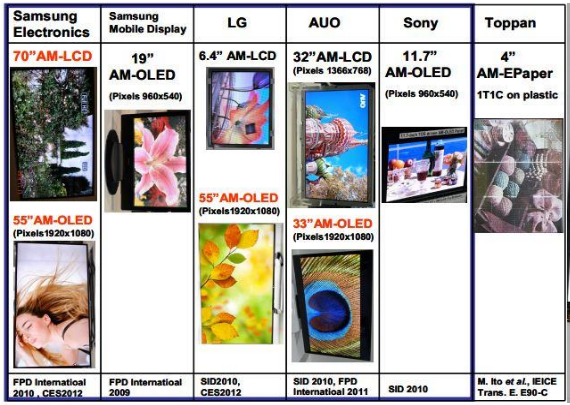
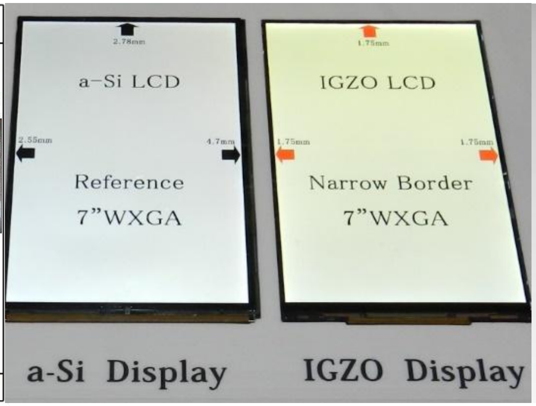
Outline

- Introduction of IGZO TFT
- Multiple Trapping and Release Theory
- Surface Potential and Model Equations
- RFID Circuit simulation
- Summary

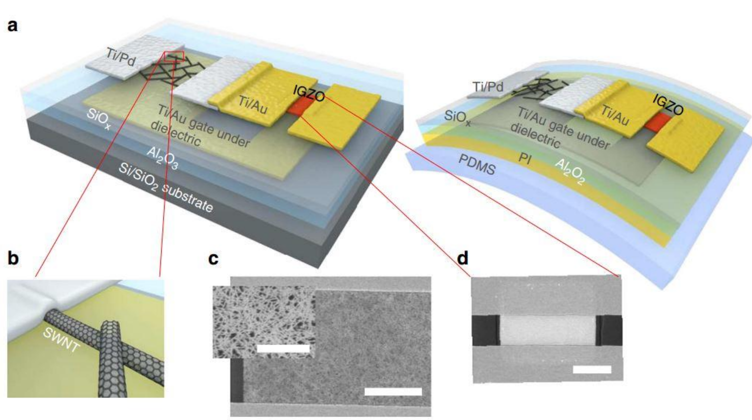
IGZO TFT application-Display

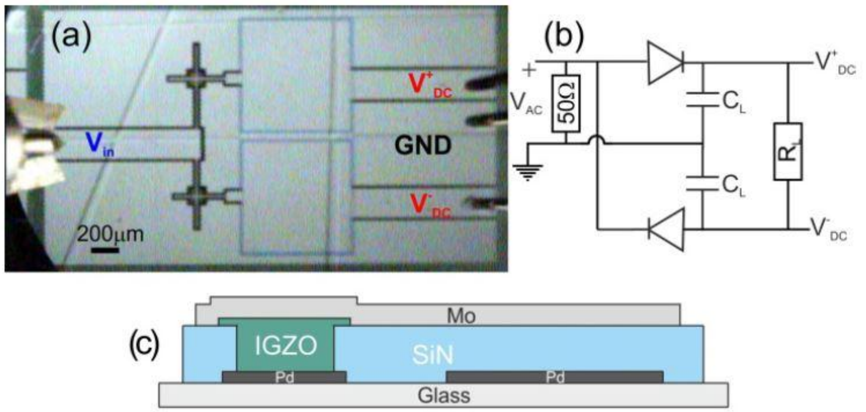




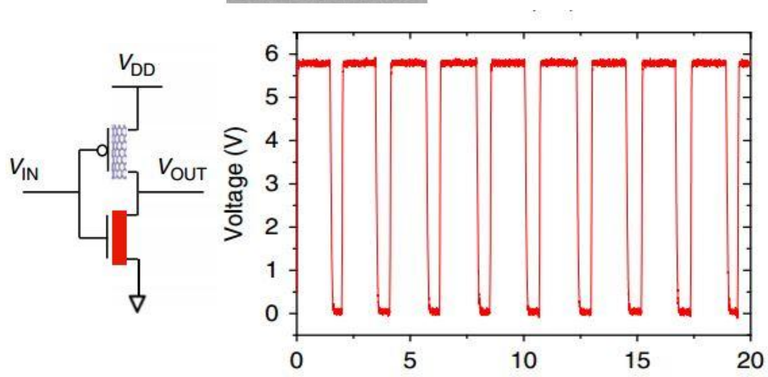
	a-Si	LTPS	a-IGZO	Organic
Mobility(cm^2/Vs)	~0.5	~100	10~80	5~6
Uniformity	Good	Poor	Good	Poor
Reliability	Poor	Good	Good	Poor
Cost	Low	High	Low	Low

IGZO TFT application-Flexible Circuit





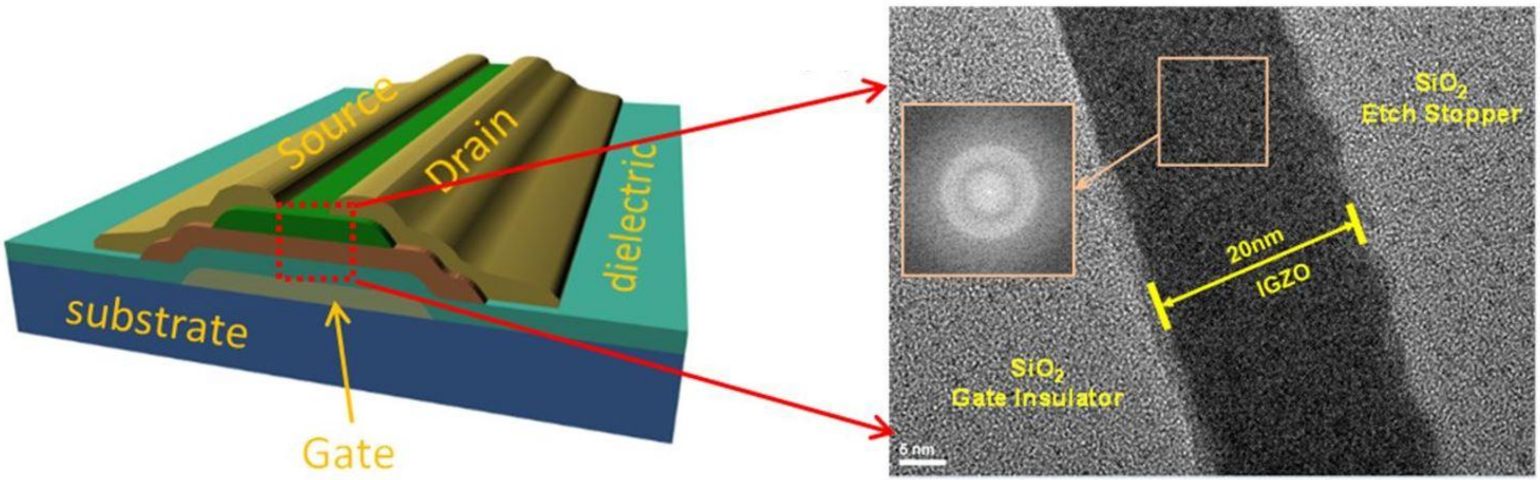
Adrian Chasin, et al., “An Integrated a-IGZO UHF Energy Harvester for Passive RFID Tags”

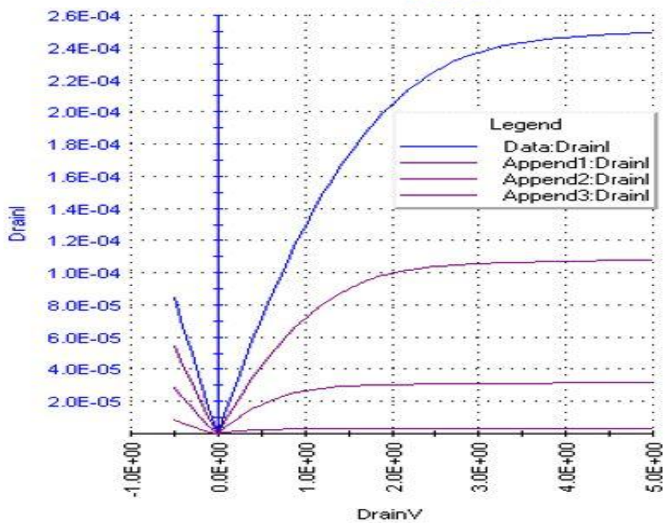


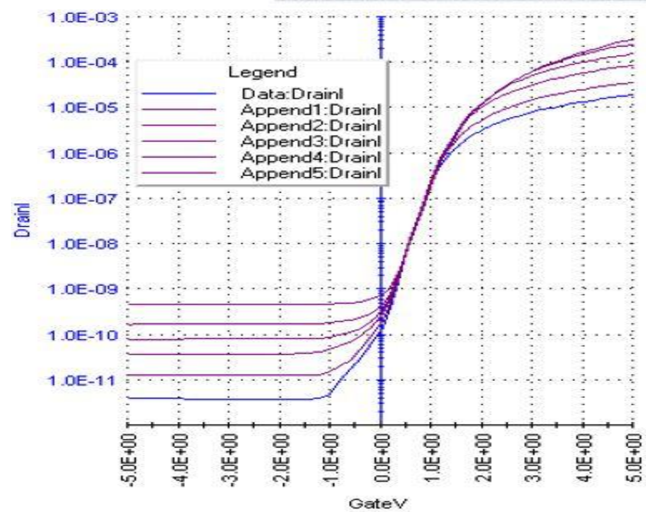
Haitian, et al., “Large-scale complementatry macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors”

- ◆Flexible
- ◆Transparent
- ◆Room temperature process
- ◆Low cost

IGZO TFT Structure







S/D: CrAu

L= 5um

T=294K

Motivation

- IGZO TFT is an excellent candidate for display and flexible circuit application
- Circuit designers need accurate but fast compact model
- The charge transport mechanism in IGZO is different from a-Si and organic

More physical meaning. Without numerical calculation.

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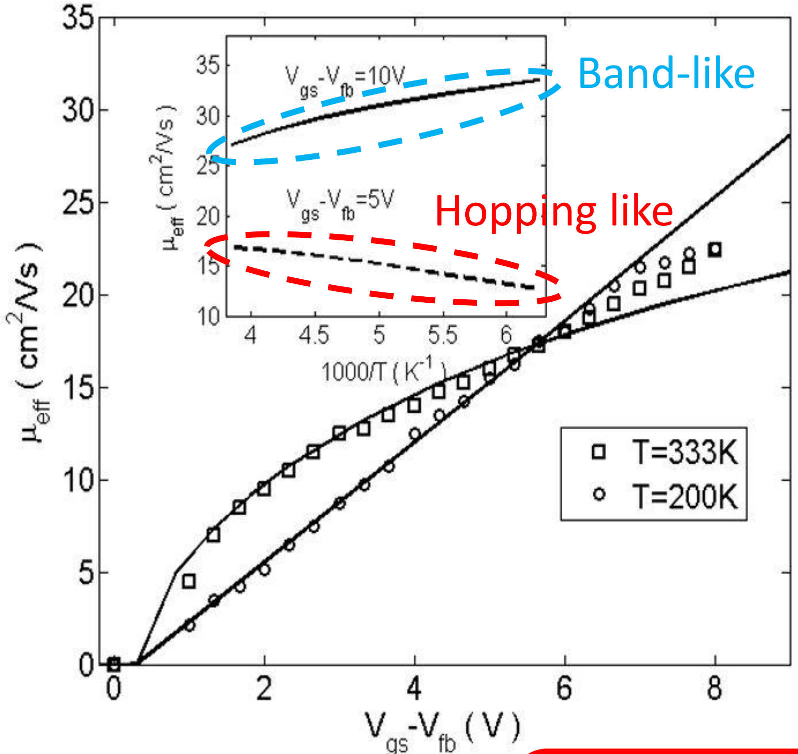
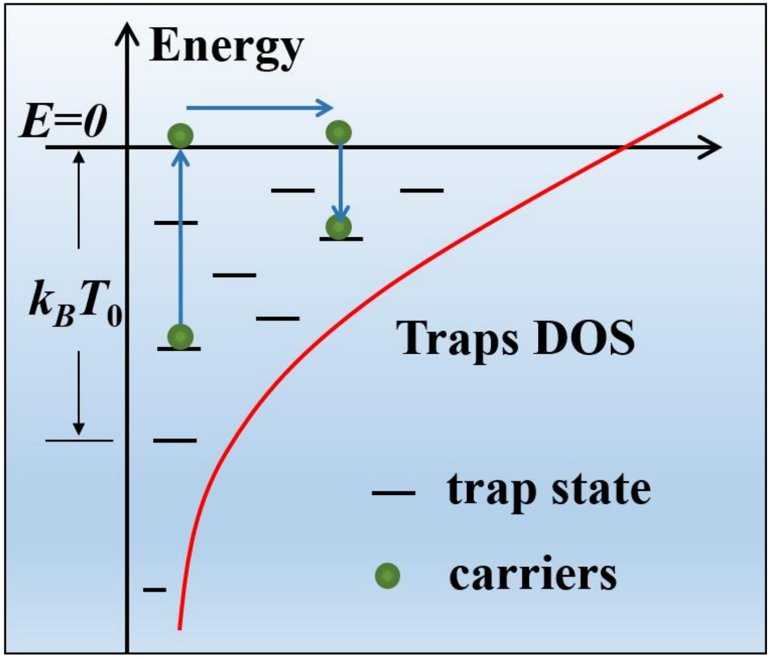
- ☐ Introduction of IGZO TFT
- ☐ **Multiple Trapping and Release Theory**
- ☐ Surface Potential and Model Equations
- ☐ RFID Circuit simulation
- ☐ Summary

Multiple-trapping and release theory





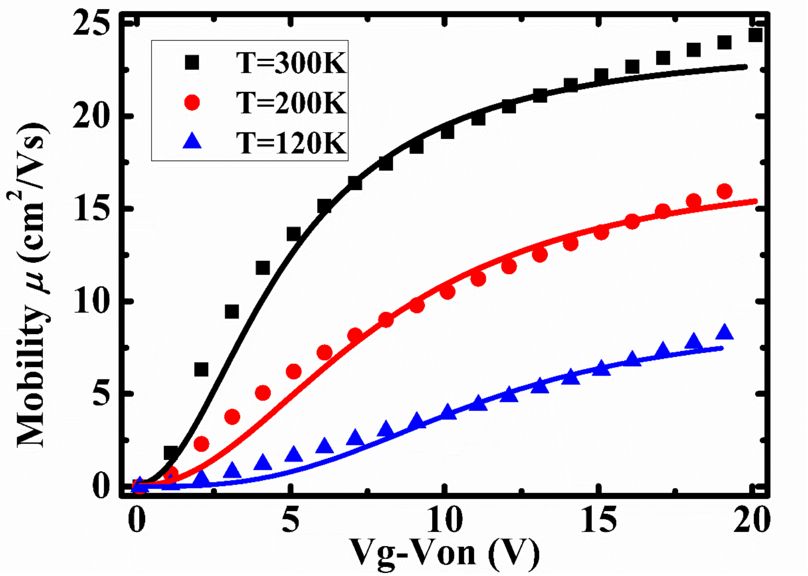
$$\mu_{eff} = \mu_e \frac{n_e(\varphi_s)}{n_e(\varphi_s) + n_t(\varphi_s)}$$

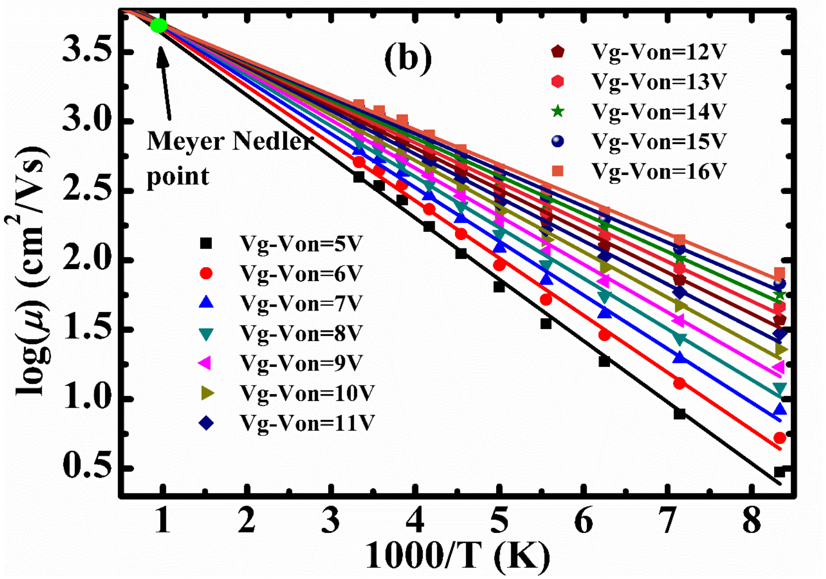
Effective mobility

Free carrier density

Trapped carrier density

Multiple-trapping and release theory





Gate voltage and temperature dependent mobility, Mobility vs. Temperature, at different Gate Voltage

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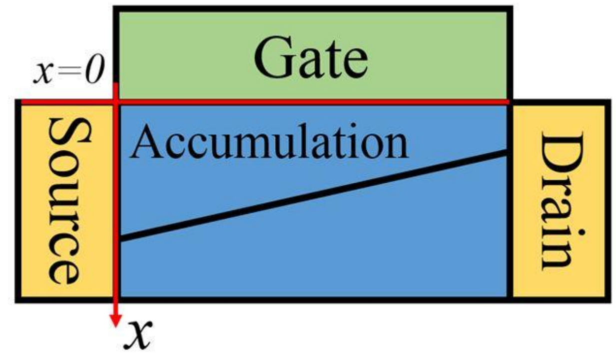
Analytical Surface Potential Solution

- **Density of total carrier**

$$n(\mathrm{x}) = n_e(\mathrm{x}) + \int_{-\infty}^{0} \frac{g(\mathrm{E})}{1+\exp(\frac{E-E_F(\mathrm{X})}{k_B T})} dE$$



- **Poisson's Equation**

$$\frac{d^2\varphi(x)}{dx^2} = -\frac{q}{\varepsilon_s} n(x)$$

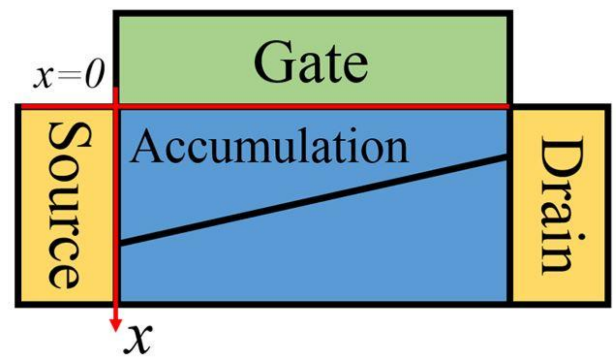
$$2\,(\partial\psi/\partial x)\,(\partial^2\psi/\partial x^2) = \partial\,(\partial\psi/\partial x)^2\,/\partial x$$

- **Gauss Law**

$$C_i\left(V_g - V_{FB} - \varphi_s\right) = \varepsilon_s F(0)$$

F(0): The electric field at the interface x=0

Analytical Surface Potential Solution



- **Density of states in IGZO**

$$g(E) = \frac{N_t}{k_B T_{TA}} \exp\left(\frac{E}{k_B T_{TA}}\right)$$

- **Trapped carrier density**

$$n(x) \approx \int_{-\infty}^{0} \frac{g(E,x)}{1+\exp\left(\frac{E-E_F(\mathrm{x})}{k_B T}\right)} dE = N_t k_B T_{TA} \Gamma\left(1 - T/T_{TA}\right) \Gamma\left(1 + T/T_{TA}\right)$$

- **Final Surface Potential Equation**

Free carrier | Trapped carrier

$$C_i\left(V_g - V_{FB} - \varphi_s\right) = \sqrt{q\varepsilon_s\left(\nu_0 \tau_0 N_t \frac{k_B T}{q} \exp\left(\frac{E_{F0}+q\varphi_s}{k_B T}\right) + N_t \frac{k_B T_{TA}}{q} \Gamma\left(1+\frac{T}{T_{TA}}\right) \Gamma\left(1-\frac{T}{T_{TA}}\right) \exp\left(\frac{E_{F0}+q\varphi_s}{k_B T_{TA}}\right)\right)}$$

Analytical Surface Potential Solution

■ Taylor expansion

$$(x-xg)=G_T\left[\exp(x-xn)\right]^{\frac{T_{TA}}{T}}+G_{TA}\exp(x-xn) \quad x=\frac{\varphi_s}{2k_BT_{TA}/q}, xg=\frac{V_g-V_{FB}}{2k_BT_{TA}/q}, xn=\frac{V_{CH}}{2k_BT_{TA}/q}$$

$$x_i=xg\{[(xg+1)^2+2xn+2\log(\frac{xg}{G_t})]^{\frac{1}{2}}-xg-1\}$$

■ Schroder series modification

$$f=(xg-x)-G_{TA}\exp(x-xn)-G_T\left[\exp(x-xn)\right]^{\frac{T_{TA}}{T}}$$

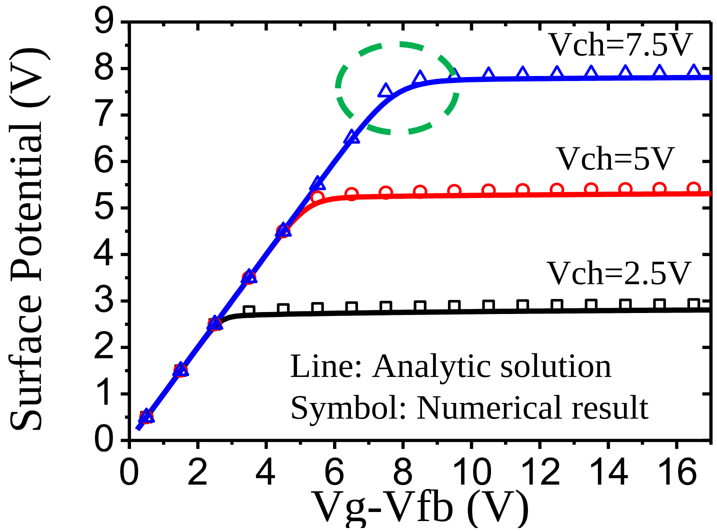
$$x=x_i-\frac{f}{\partial f}-\frac{\partial^2 f}{2\partial f}\left(-\frac{f}{\partial f}\right)^2+\frac{(3\partial^2 f)^2-\partial f\partial^3 f}{6(\partial f)^2}\left(-\frac{f}{\partial f}\right)^3$$

$$\Delta=x-x_i=-\frac{f}{\partial f}\left[1+\frac{\partial^2 f}{2\partial f}\frac{f}{\partial f}\right] \Rightarrow$$

$$x=x_i+\Delta$$

$$\varphi_s=x\cdot 2\frac{k_BT_{TA}}{q}$$

Maximum error : 0.03mV



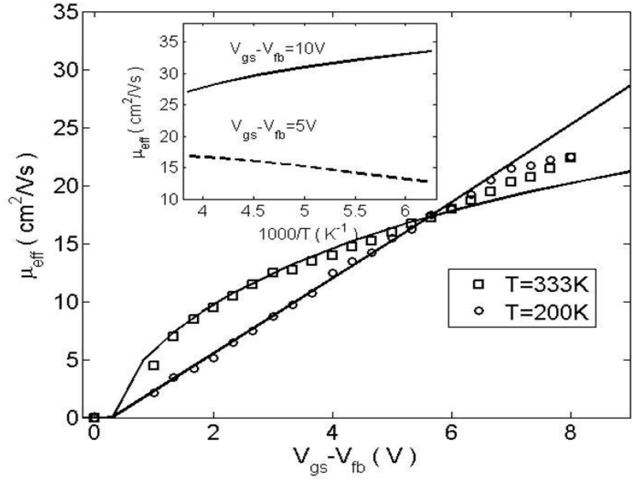
Fully analytical without adding new fitting parameters

Model equations

■ Effective Mobility Equation

$$\mu_{eff} = \frac{\mu_e}{1+\frac{1}{v_0\tau_0}\Gamma(1-T/T_{TA})\Gamma(1+T/T_{TA})exp\left(\frac{E_{F0}+q\varphi_s}{k_B T_{TA}}\left(1-\frac{T_{TA}}{T}\right)\right)}$$

$$\mu_{eff} \propto (V_g - V_{fb})^{2(\frac{T_{TA}}{T}-1)}$$

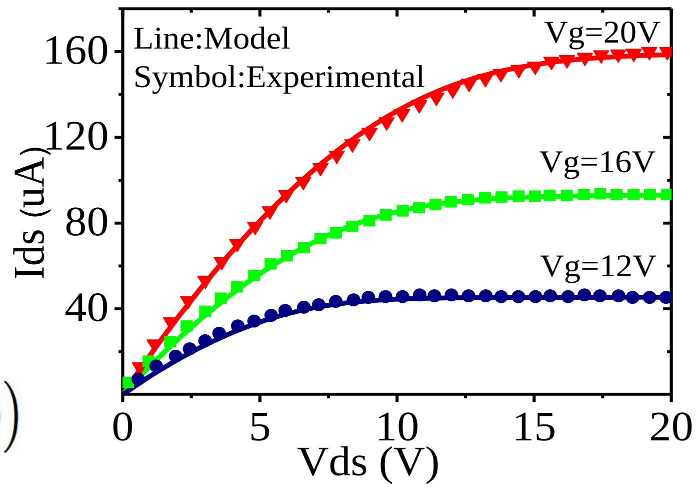


■ Drain Current Equation

$$I_{ds} = -\mu_{eff} W Q_i \frac{dV}{dy} = -\mu_{eff} W Q_i \left(2\Phi_t \frac{C_{ox}}{Q_i} + 1\right)\frac{d\Phi}{dy}$$

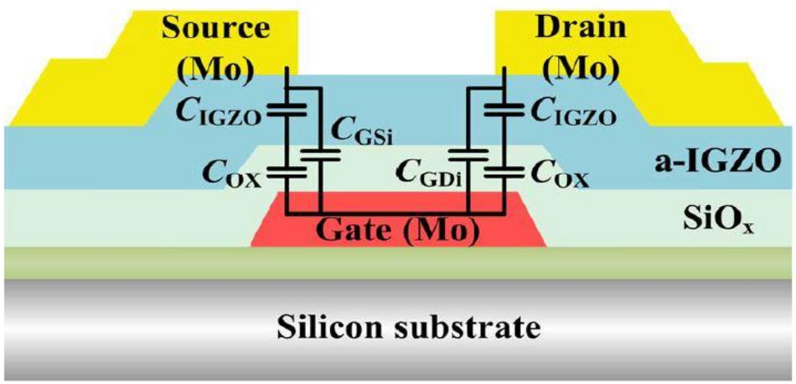
Integrate from Φ_{SS} to Φ_{SD}

$$I_{ds0} = \mu_{eff}\frac{W}{L}\Big(2\Phi_t C_{ox}(\Phi_{sd} - \Phi_{ss}) - 0.5 * \left(\left(V_g - V_{fb} - \Phi_{sd}\right)^2 - \left(V_g - V_{fb} - \Phi_{ss}\right)^2\right)\Big)$$



Model equations

■ Capacitance Equations



Intrinsic Capacitance	Extrinsic Capacitance
$C_{Gi} = \frac{\partial Q_G}{\partial V_G}\Big\vert_{V_S, V_D = const}$ [F]	$C_G = C_{Gi} + 2C_{OV}$ [F] $C_{GD} = C_{GDi} + C_{OV}$ [F] $C_{GS} = C_{GSi} + C_{OV}$ [F]
$C_{GSi} = \frac{\partial Q_S}{\partial V_G}\Big\vert_{V_S, V_D = const}$ [F]	**Overlap Capacitance (C_{OV})**
$C_{GDi} = \frac{\partial Q_D}{\partial V_G}\Big\vert_{V_S, V_D = const}$ [F]	$C_{OV} = C_{OX} // C_{IGZO}$ [F] $C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} \times WL_{OV}$ [F] $C_{IGZO} = \frac{\varepsilon_{IGZO}}{T_{IGZO}} \times WL_{OV}$ [F]

Minkyung Bae, et al., “Analytical Current and Capacitance Models for Amorphous IGZO Thin-Film Transistors”

$$Q_g = WLC_{ox}\frac{2/3[A^2+B^2+AB]}{A+B}$$

where $A = V_g - V_{fb} - \Phi_{ss}$ and $B = V_g - V_{fb} - \Phi_{sd}$

$$Q_d = WLC_{OX}\frac{2}{15}\frac{[2A^3+4A^2B+6AB^2+3B^3]}{(A+B)^2}\ ;\ Q_s = -Q_d - Q_g$$

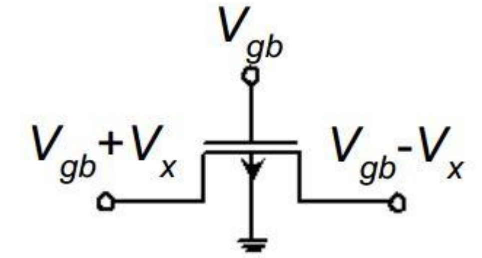
$$C_{i,j} = \pm\frac{\partial Q_i}{\partial V_j}$$

Ward’s charge-partitioning scheme

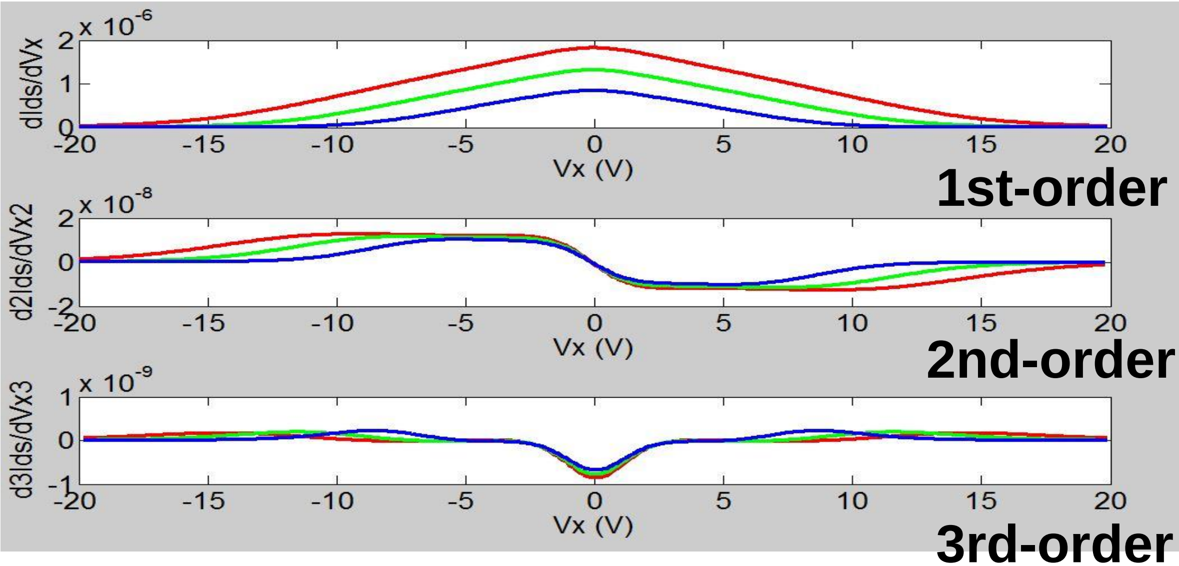
Gummel Symmetry Test

Key requirements for GST

- **Odd function**
- **Nonsingular for nth-order derivative**

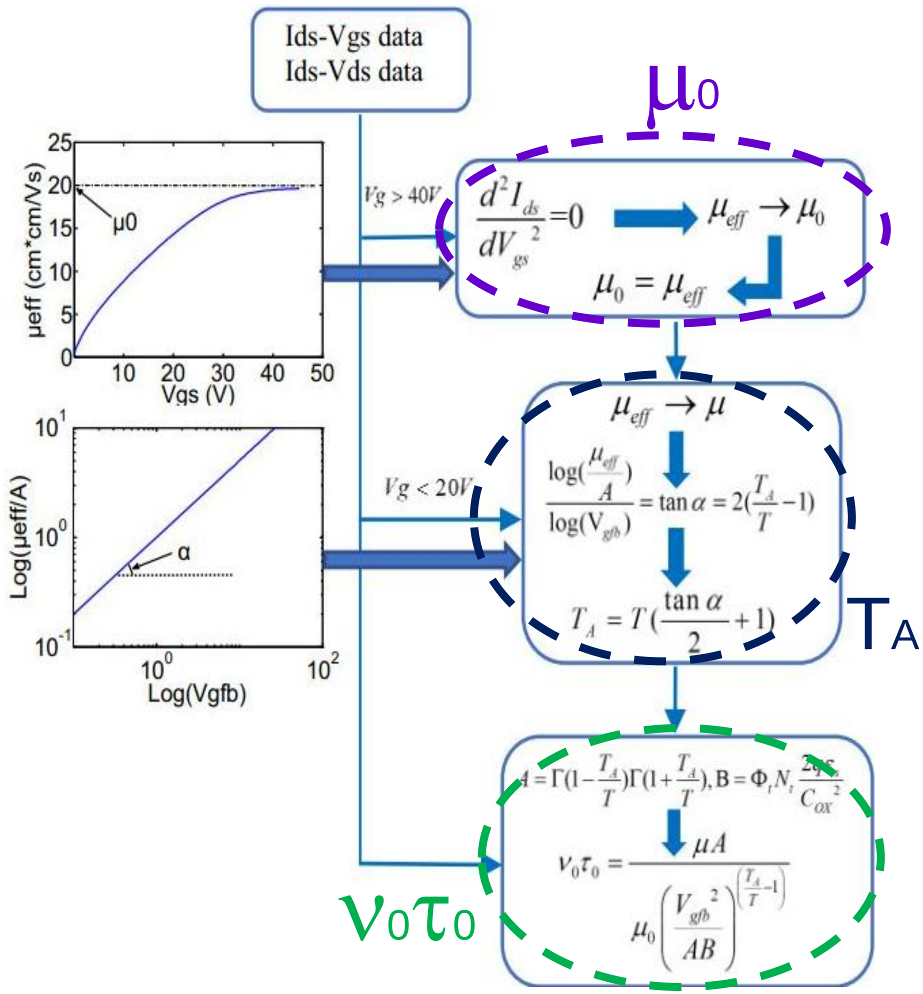


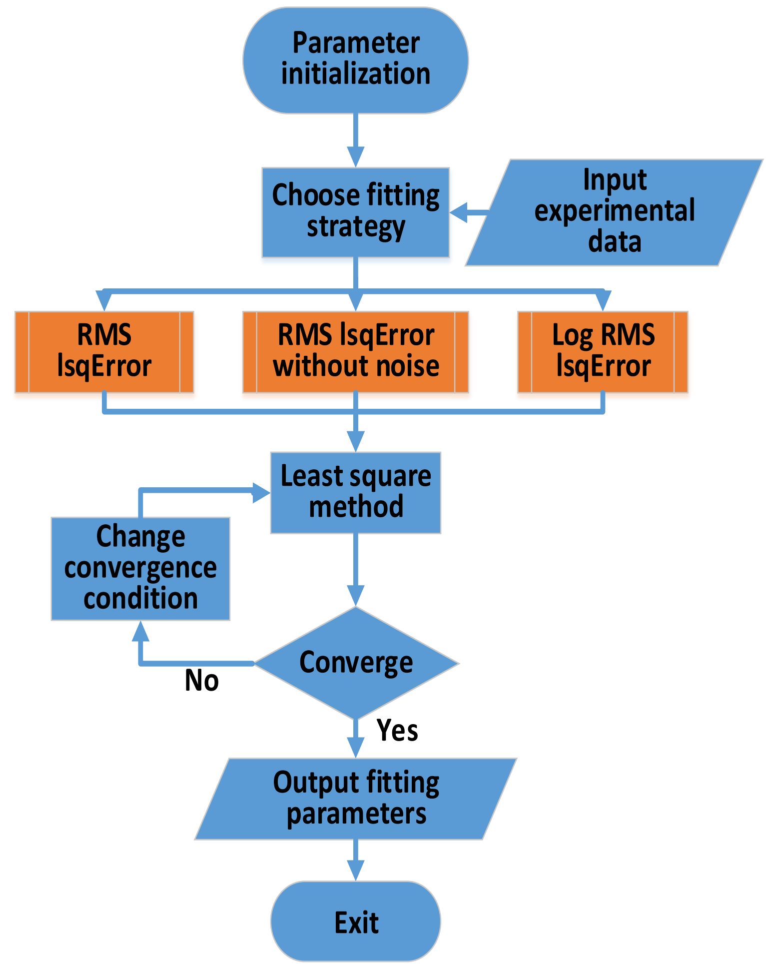
Gummel Symmetry Test circuit



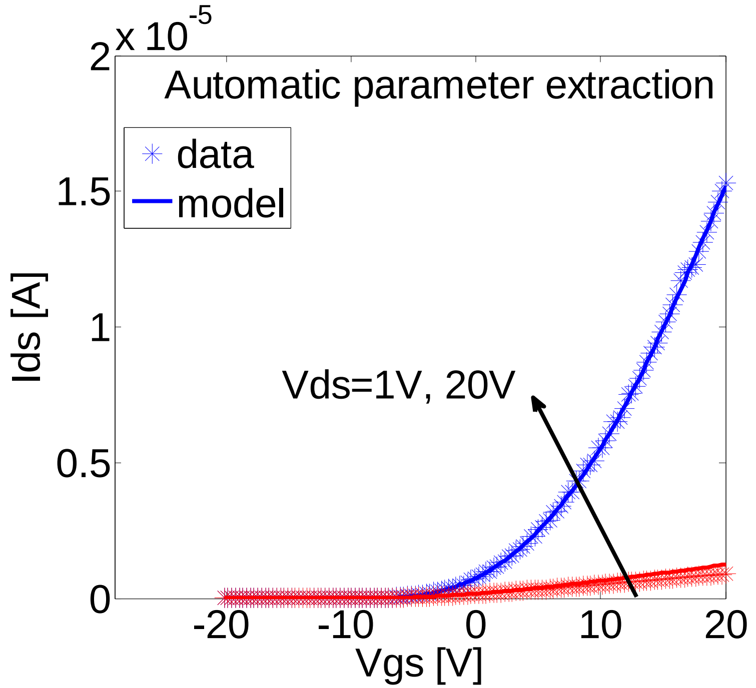
All derivatives are continuous at Vds=0

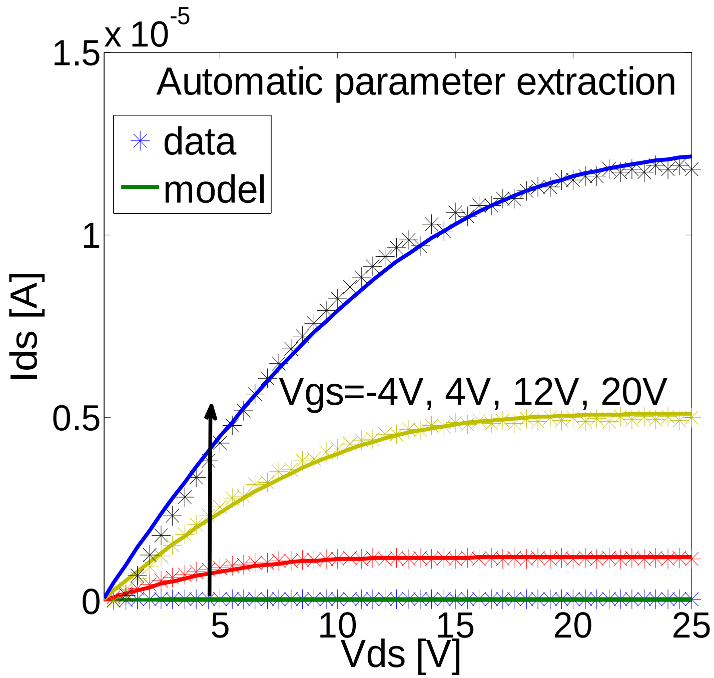
Parameters extraction





Parameters extraction



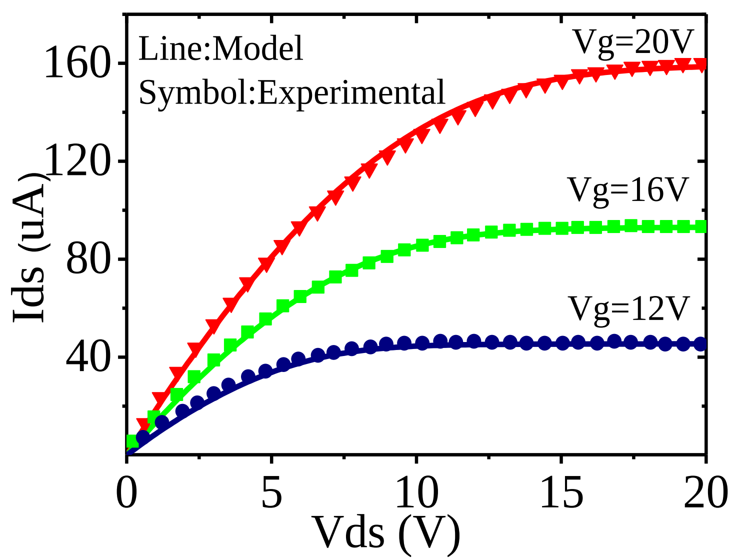


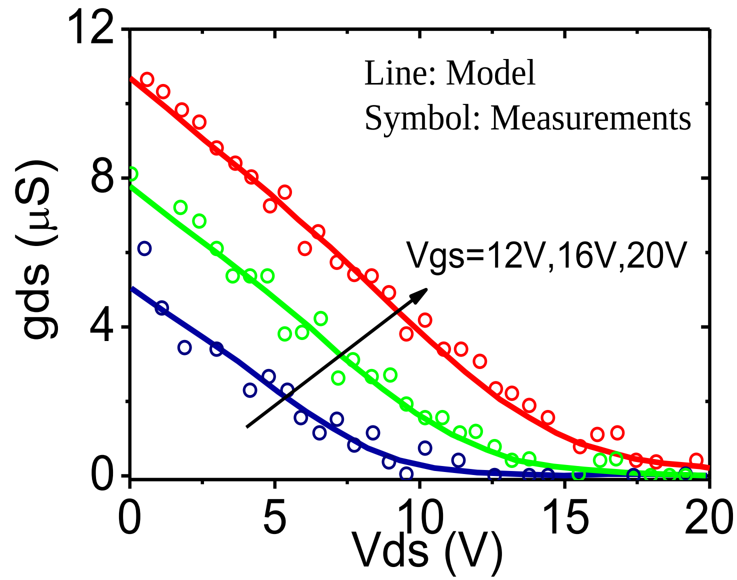
Parameter	Extracted value	Parameter	Extracted value
T_A (K)	405	$v_0\tau_0$	1
n	5	C_{OX} (F/cm^2)	8.85×10^{-8}
m	1	V_{fb} (V)	0.5
ss	2.75	μ_0 (cm^2/Vs)	19.7

Accurate & Rational

Model results

Output and gds-Vds curves

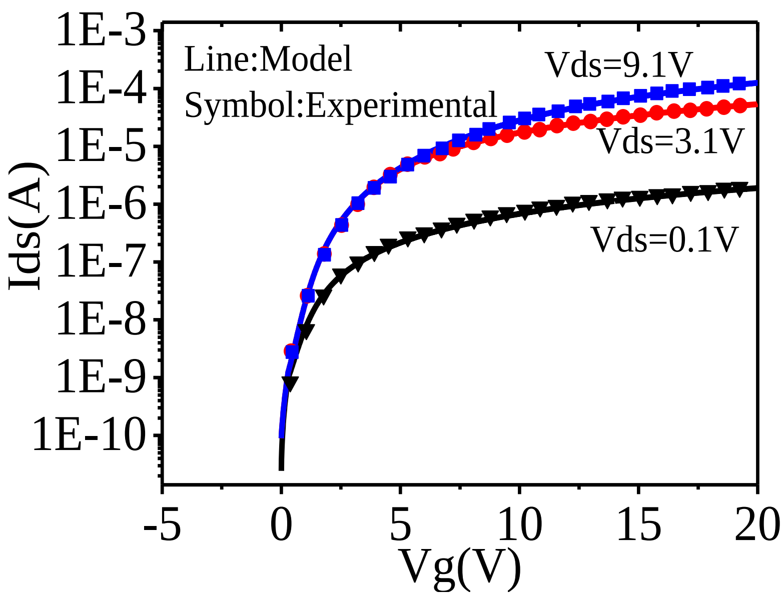


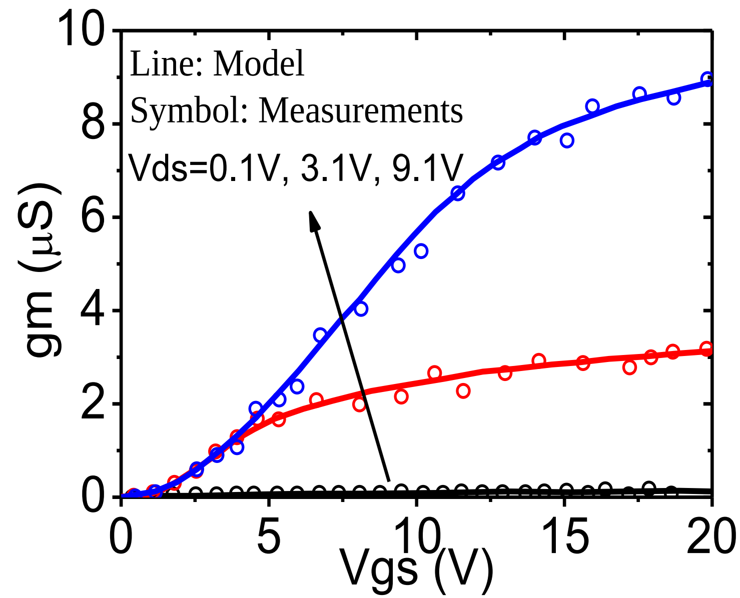


Comparison between the calculation and experimental data for output characteristics of IGZO under different gate voltages and g_{ds}-V_{ds} curves.

Model results

Transfer and trans-conductance curves

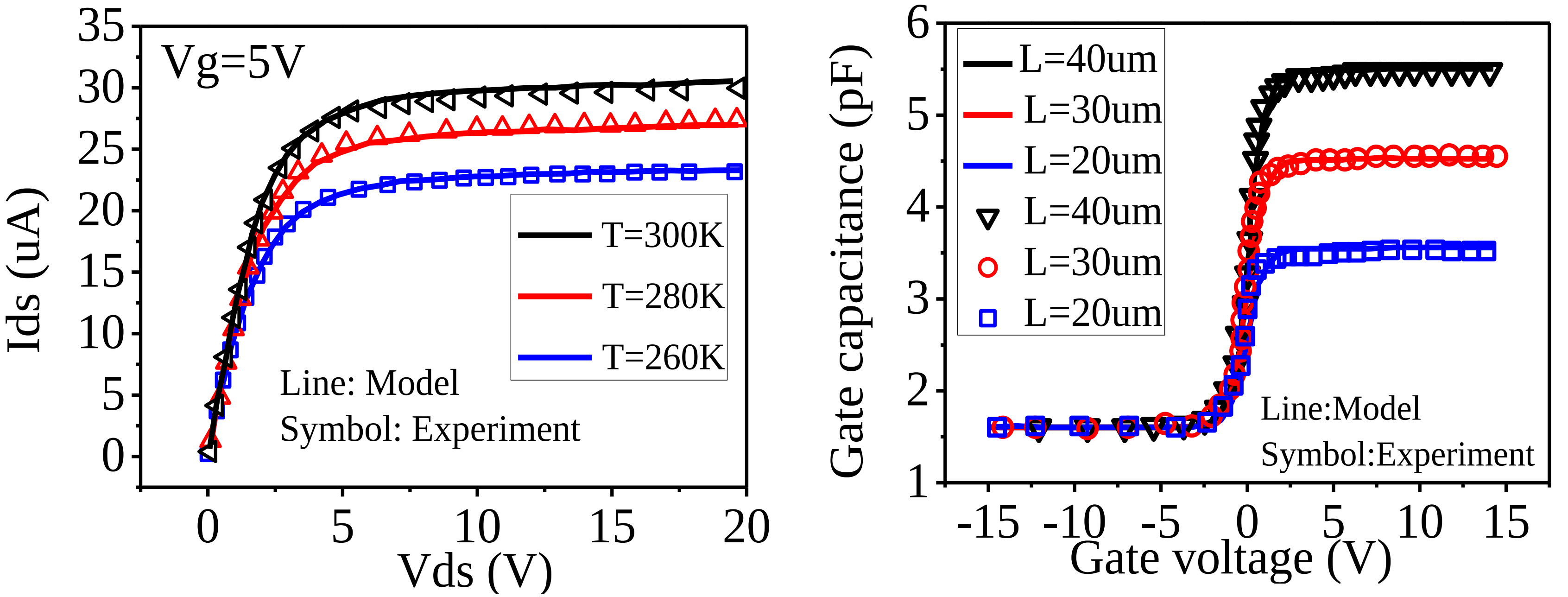




Comparison between the calculation and experimental data for transfer characteristics of IGZO under different drain-source voltages and transconductance curves.

Model results

Temperature and gate capacitance curves



Model results and experimental data a good agreement

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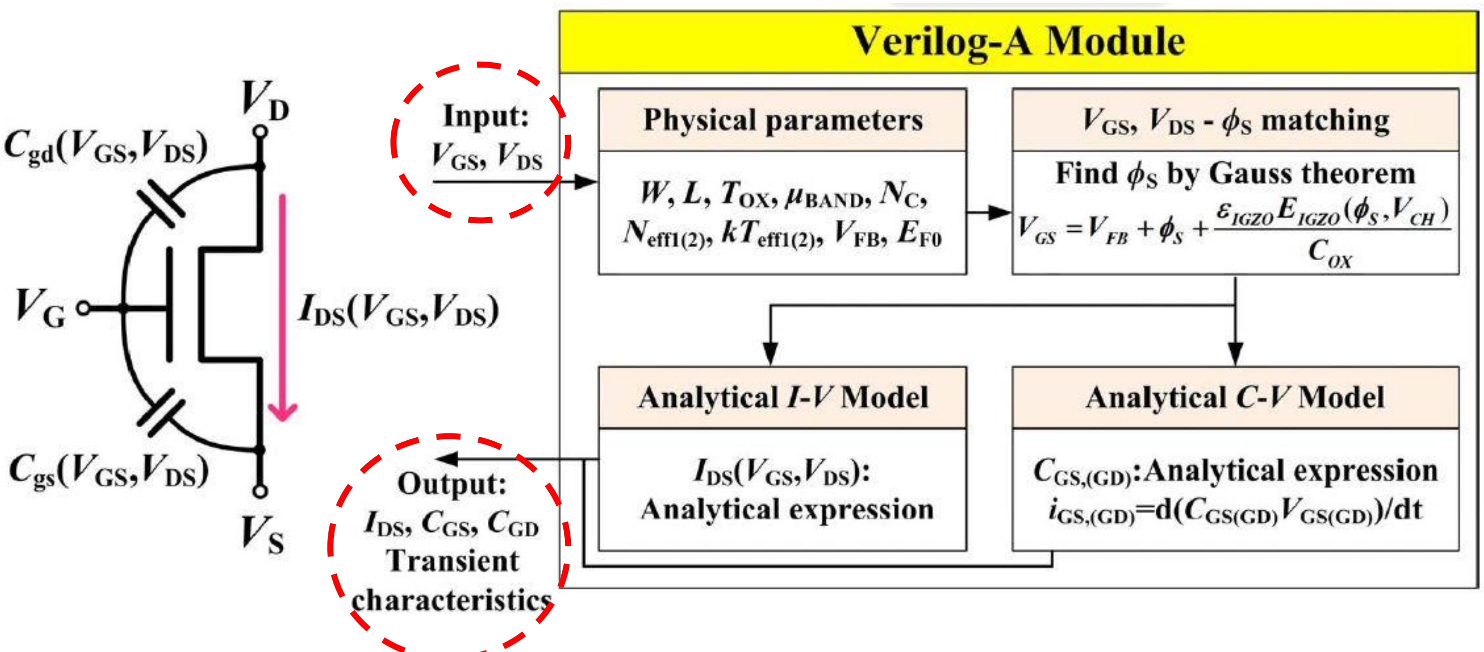
RFID circuit simulation

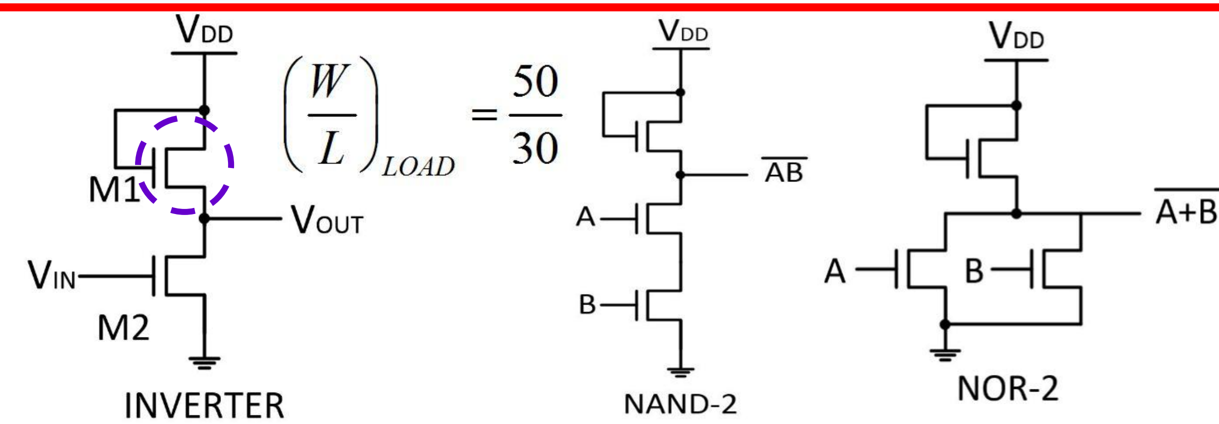
Verilog-A Module

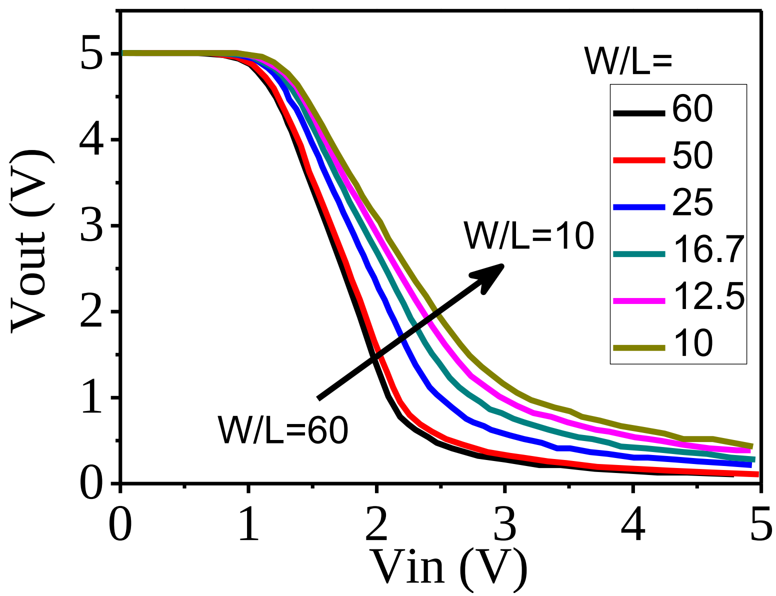


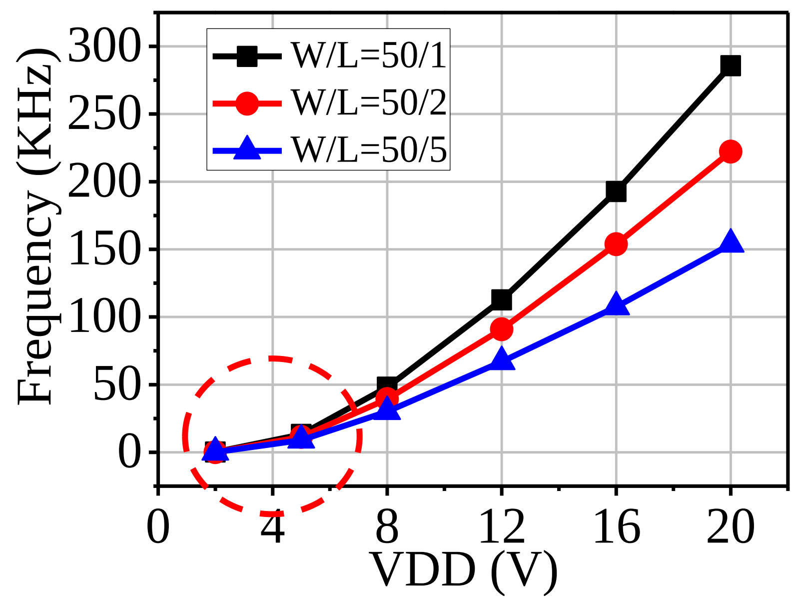
Minkyung Bae, et al., “Analytical Current and Capacitance Models for Amorphous IGZO Thin-Film Transistors”

Simulation results & discussion

Pseudo -CMOS



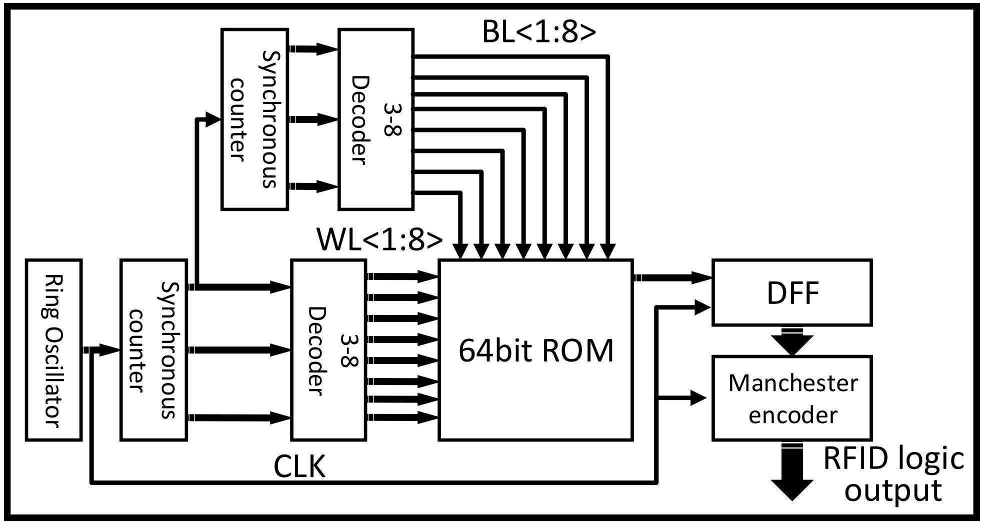




RFID circuit simulation

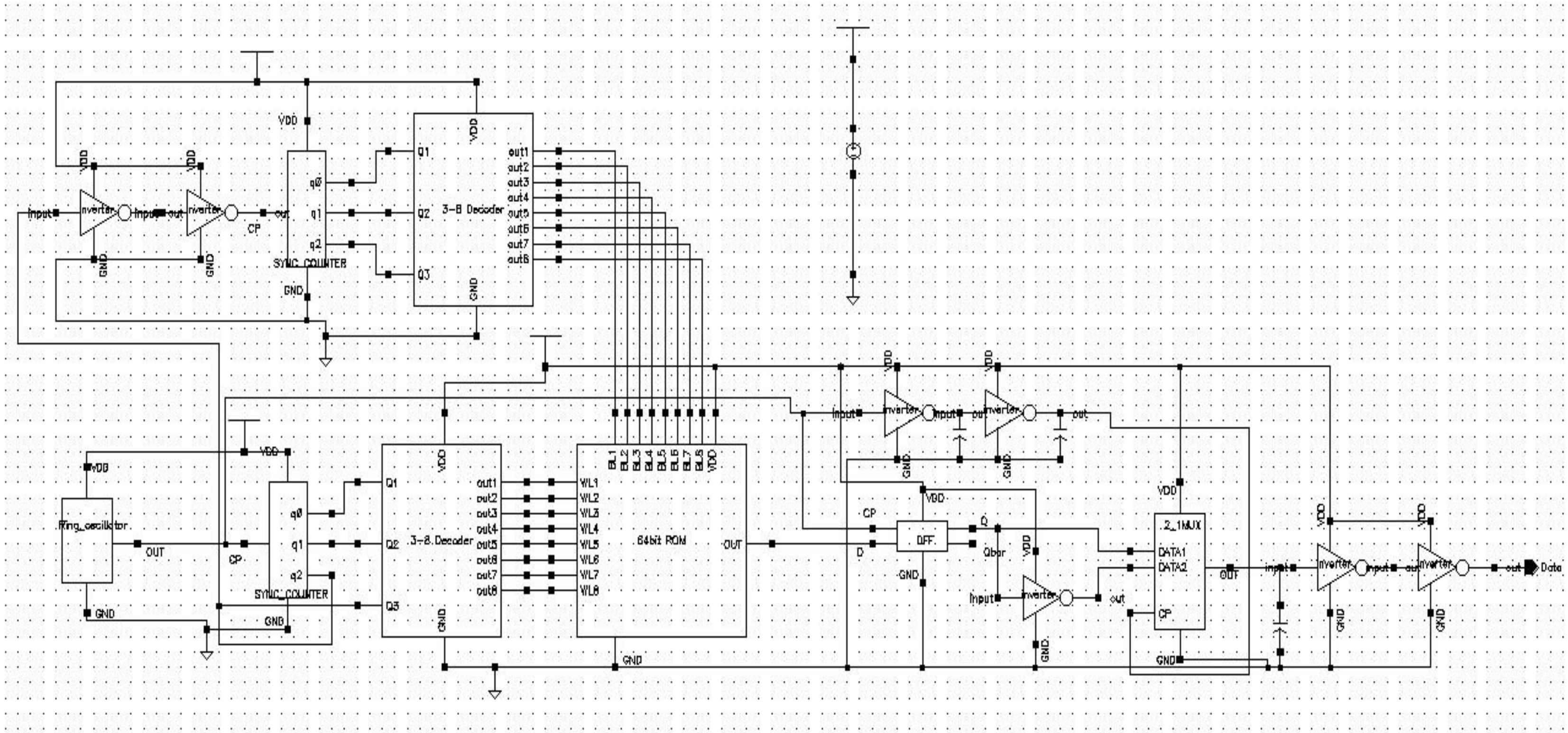
RFID digital circuit block

- Ring Oscillator
- Synchronous Counter
- 3-8 Decoder
- 64bit ROM
- Manchester Encoder



RFID circuit simulation

Schematic diagram

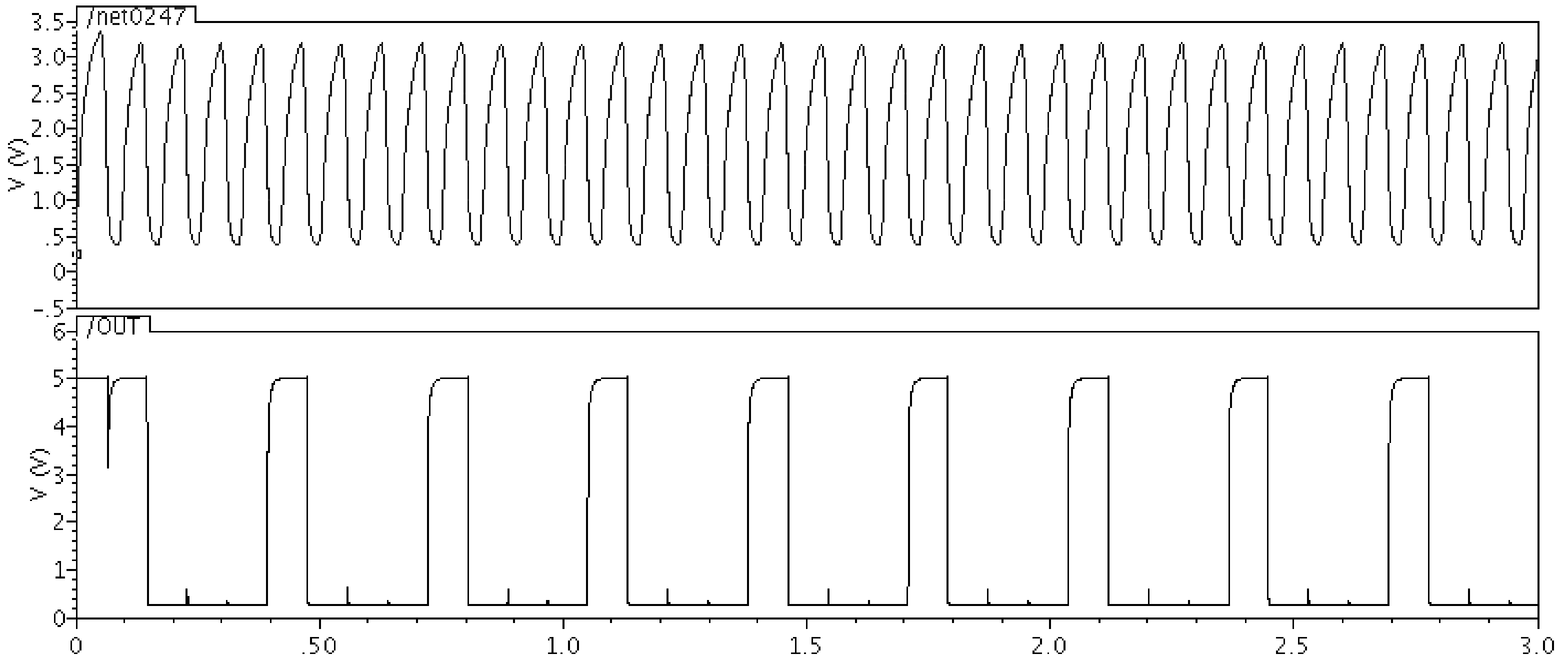


Simulation results & discussion

Failure situation 1:

- **V_{dd}=5V**
- **Driver transistor W/L=35**

Minimum power consumption



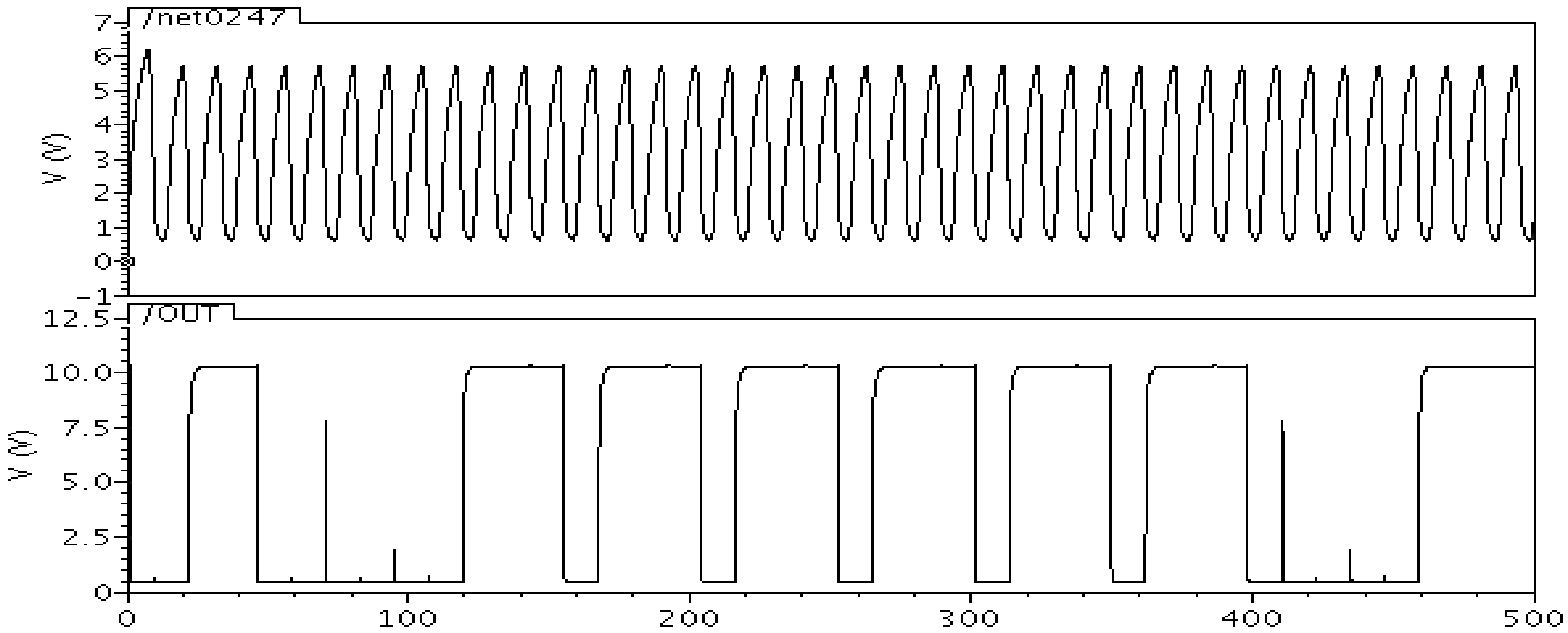
10000000 11000000 11100000 11110000 11111000 11111100 11111110 11111111

Simulation results & discussion

Failure situation 2:

- V_{dd}=12V
- Driver transistor W/L=50

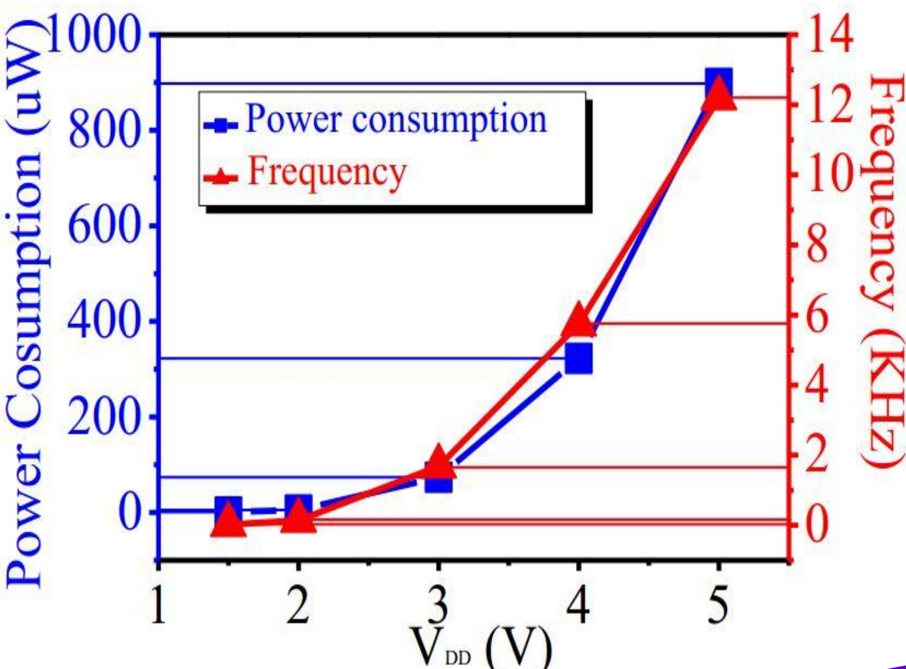
Maximum Clock Frequency

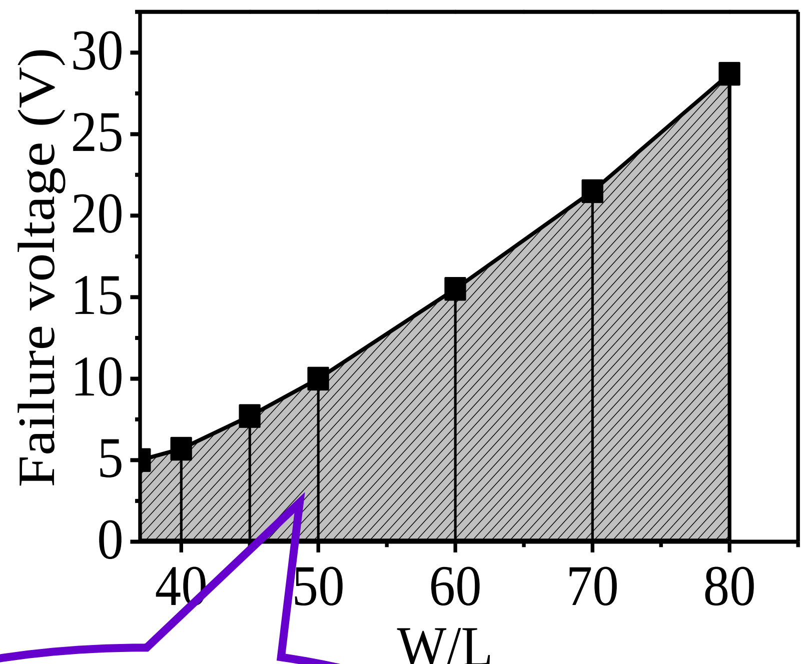


10000000 11000000 11100000 11110000 11111000 11111100 11111110 11111111

Simulation results & discussion

Failure voltage at different W/L of driver transistor

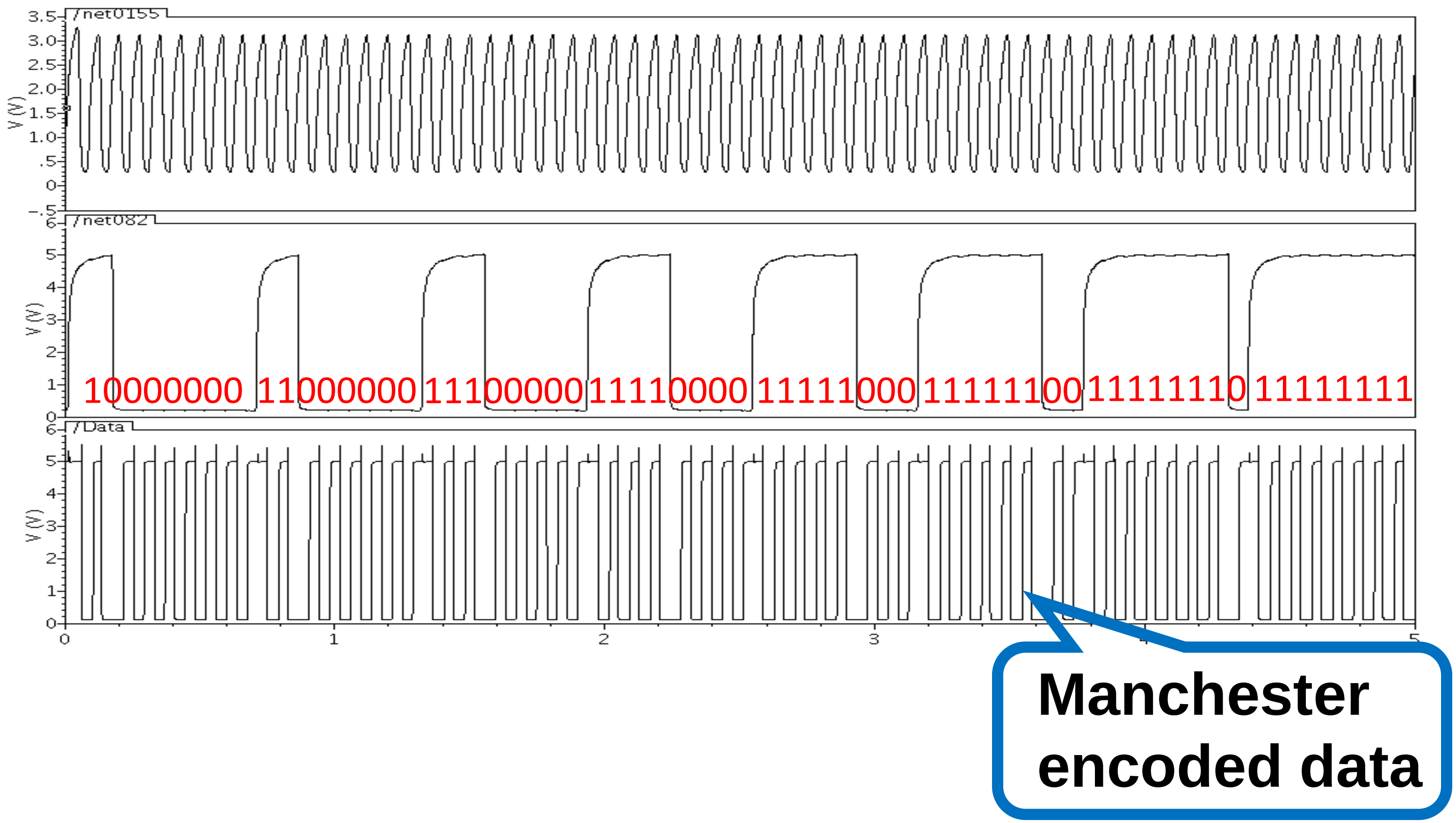




The shaded area shows available region for V_{DD} and W/L.

Simulation results & discussion

RFID circuit simulation results



Summary

- Incorporated multiple-trapping and release theory into compact modeling
- Proposed a new method for calculating surface potential analytically
- Developed the parameter extraction program for IGZO TFT compact model
- RFID circuit design based on developed model
- Discussed the maximum operating frequency and minimum power consumption in particular situation

Thanks for your attention!

Q & A