

Research progress of SOI devices and modeling in SIMIT

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Shanghai Institute of Microsystem and Information Technology
Chinese Academy of Sciences**

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■ Introduction of SOI Group

□ Research results

- ✓ DC Device Model
- ✓ RF Device Model
- ✓ Research of SOI Device
- ✓ Fruits of international cooperation

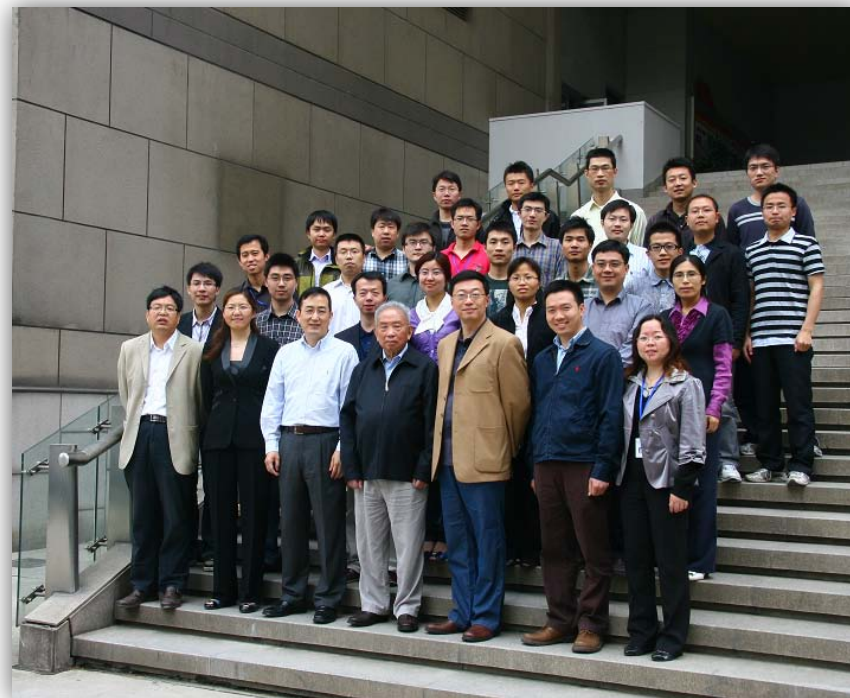
□ Summary



Prof. Xi Wang
Academician of the
Chinese Academy of
Sciences



Prof. Shichang Zou
Academician of the
Chinese Academy of
Sciences



- ◆ **Total 78 people**
- ◆ **14 professors**
- ◆ **10 associate Professors**
- ◆ **38 graduate students**

- ◆ SIMIT research teams are actively driving new SOI technology development, e.g. material, device, process, design services, products etc., help to build up SOI ecosystem.

SOI Material

- SiGe, Strain SOI
- GaN, Graphene

SOI Design Service

- Process, Device, Modeling
- PDK, Library, IP

SOI Circuit

- ASIC, FPGA, ADC, Switch

SOI Photonics

- AWG, MMI, High-end microprocessor

Achievements

100+ papers published, 150+ patents applied (including 50+ international), within the last 5 years.

the Prize of National Science & Technology Advancement (1st grade)



SOI Roadmap in SIMIT

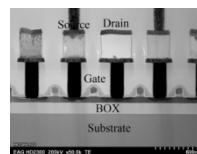
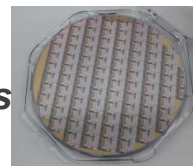


PD SOI Technology

FD SOI Technology

Technology

0.13um SOI Logic Process
0.2um SOI RF Process



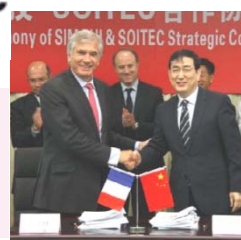
Substrates



Simox



SINGUI



Smart cut



1980s

2000s

2014s

Model Laboratory - Hardware



- ◆ Laboratory has the ability to test DC, RF and flick noise.



Electromagnetic shielding room



Cascade Summit 12000 B-M



Agilent B1500A



Agilent B1542A



Cascade EDGE Module



Agilent N5244A PNA-X

Model Laboratory - Software



◆ Laboratory has a complete EDA solution for device modeling.

✓ Sentaurus TCAD Tool

SENTAURUS PROCESS SIMULATION AND STRUC



SENTAURUS GRID GENERATION



SENTAURUS DEVICE SIMULATION



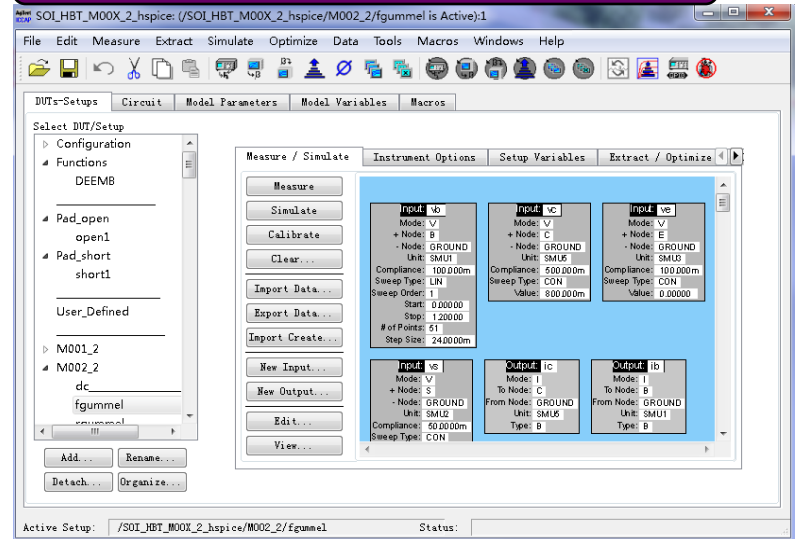
✓ Cadence Tool

cadence

Custom IC Design Tools
Virtuoso® Front to Back Design Environment

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✓ Agilent Model Tool



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Version 2010.1.0

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■ Introduction of SOI Group

■ Research results

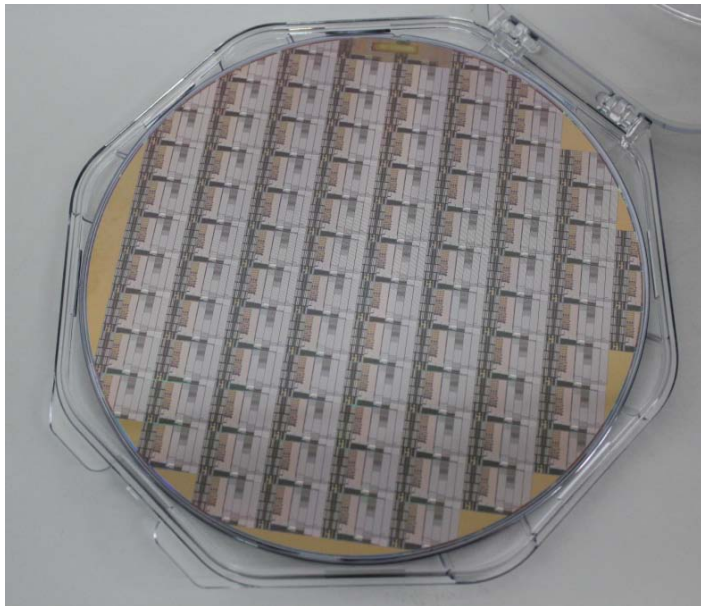
- ✓ DC Device Model
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□ Summary

DC Device Model



- ◆ We have extracted a complete DC Device Model for 0.13 um SOI Technology.



Golden Wafer for SOI Device modeling

Device	•MOS (FB, TB, HB) , BJT, Resistor, Diode, MIM
Level	•70 (BSIM4SOI)
Effects	•FBE/GIFBE, SHE, Gate-leakage, GIDL
Geometry	•Core: L[0.13~10um], W[0.15~100um] •IO: L[0.35~10um], W[0.3~100um]
Temp.	•-55~125°C
Voltage	•Gate: [-1.32~1.32V](core) / [-3.63~3.63V](IO) •Drain: [0~1.32V](core) / [0~3.63V](IO)
Corner	•TT, FF, SS, FS, SF

The contents of 0.13 um SOI model library

- ◆ All corner of model have correct trend, without warning and error. We have an detailed QA report of 0.13 um SOI Model.

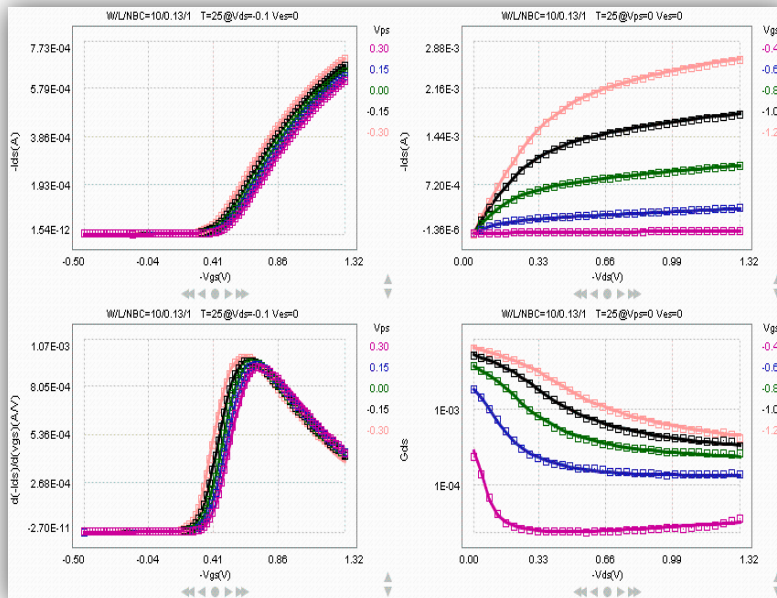
Model Target:

Accuracy: $\Delta V_{tlin} < 5mV$, $\Delta I_{dsat} < 2\%$

Physical: Cover most physical effects (FBE/SHE)

Scalable: Model QA pass from W_{max}/L_{max} to W_{min}/L_{min}

Convergence: We have successfully simulated ring oscillator



Device	ΔV_{tlin}	ΔI_{dlin}	ΔI_{dsat}
Target	< 5mV	< 3%	< 3%
TB Core	< 5mV	< 1%	< 1%
FB Core	< 5mV	< 1%	< 1%
TB IO	< 5mV	< 2%	< 2%
FB IO	< 5mV	< 2%	< 2%

Ring Oscillator Results



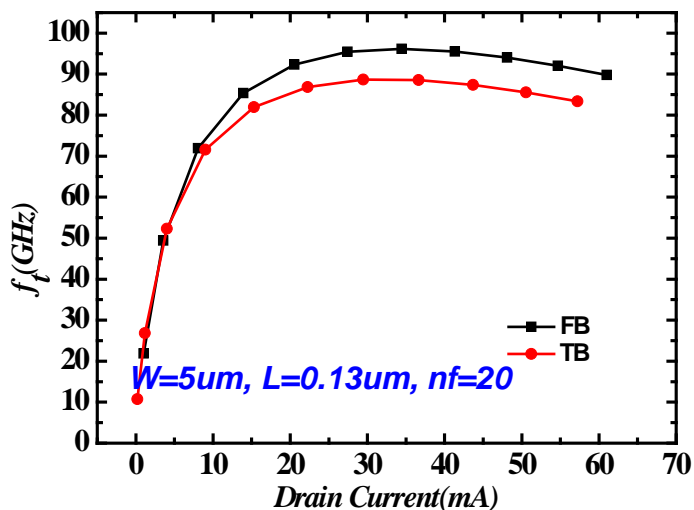
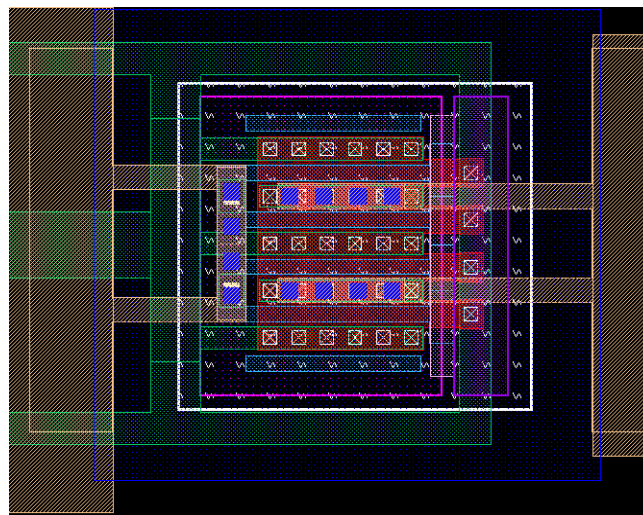
- ◆ We have designed ring oscillator for the verification of SOI Model. As shown in the table, the simulation error is less than 10%.

Ring Oscillator	Wp/Wn	Lp/Ln	FO	FF	Simulation Delay	Test Delay	Accuracy
1.2V_FB_INV	3/2	0.13/0.13	1	6	19.3	18.9	1.9%
	2/1	0.13/0.13	1	6	21.7	21.8	-0.8%
	3/2	0.13/0.13	3	5	40.4	38.7	4.5%
1.2V_TB_INV	3/2	0.13/0.13	1	6	25.6	25.1	2.1%
	2/1	0.13/0.13	1	6	29.2	29.7	-1.8%
	3/2	0.13/0.13	3	5	52.8	50.2	5.3%
3.3V_FB_INV	3/2	0.30/0.35	1	6	41.1	39.9	3.1%
	2/1	0.30/0.35	1	6	45.2	44	2.8%
	3/2	0.30/0.35	3	5	88.8	86.3	2.8%
3.3V_TB_INV	3/2	0.30/0.35	1	6	41.9	44	-4.6%
	2/1	0.30/0.35	1	6	47.3	49.8	-4.9%
	3/2	0.30/0.35	3	5	95.4	99.5	-4.1%

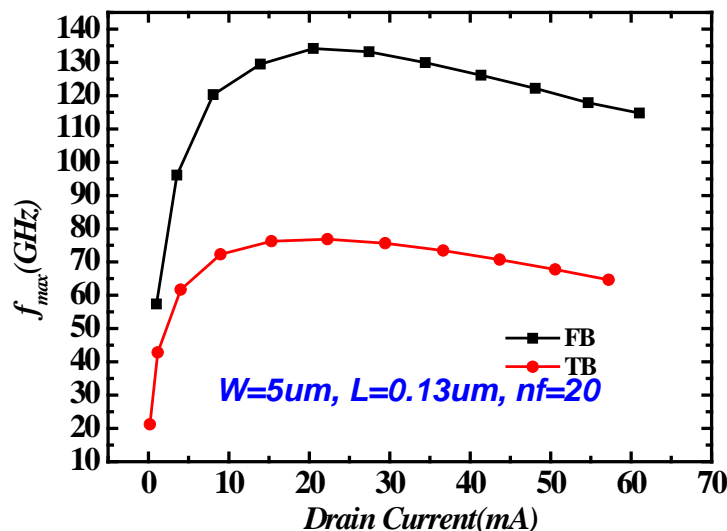
RF MOSFET

- ◆ We have designed RF test structure of SOI MOSFETs.
- ◆ The peak cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) of TB Ncore are 87 and 75 GHz.

- ✓ Core: FB Ncore, FB Pcore, TB Ncore, TB Pcore;
- ✓ IO: FB NIO, FB PIO, TB NIO, TB PIO;
- ✓ Finger: 4, 20, 60, 120;



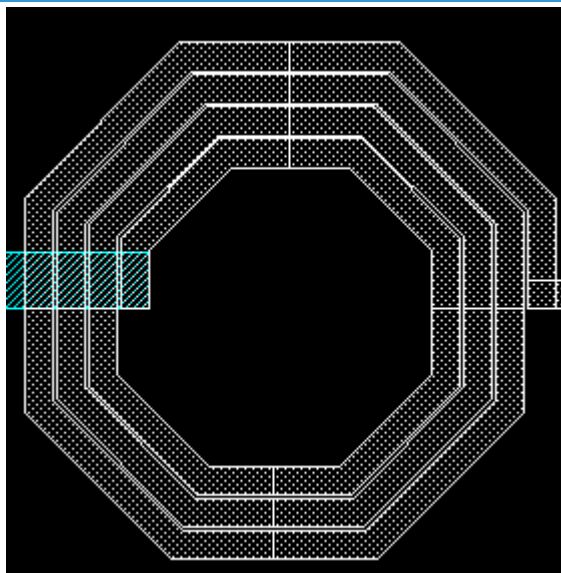
f_T characteristics of SOI Ncore device



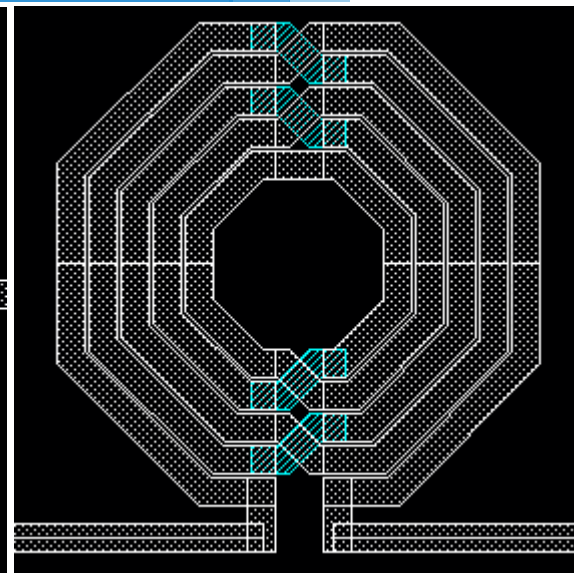
f_{MAX} characteristics of SOI Ncore device

Inductor

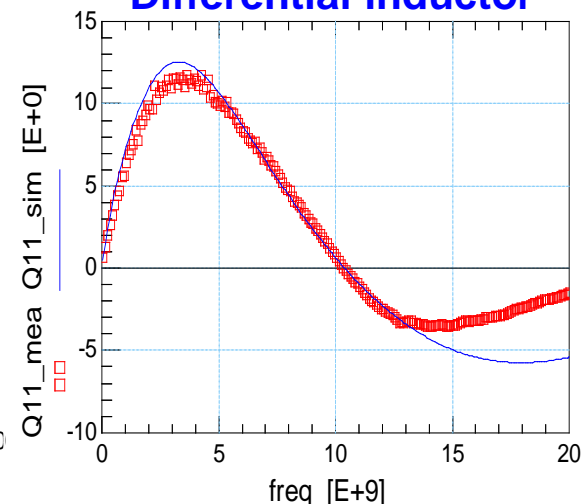
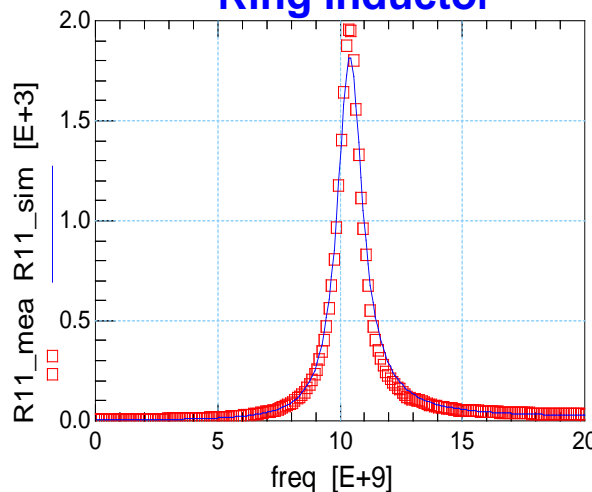
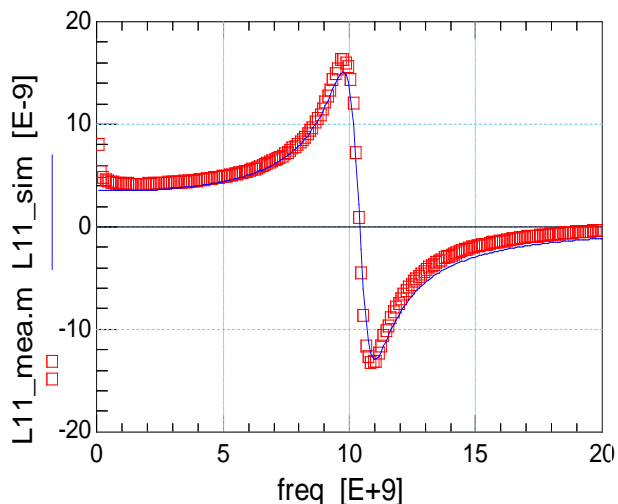
- ◆ We have designed Inductor test structure.
- ◆ The peak of Q factor is 16 in standard inductor with $N=5.5$, $W=9\mu\text{m}$, $S=2\mu\text{m}$, $D=255\mu\text{m}$.



Ring inductor



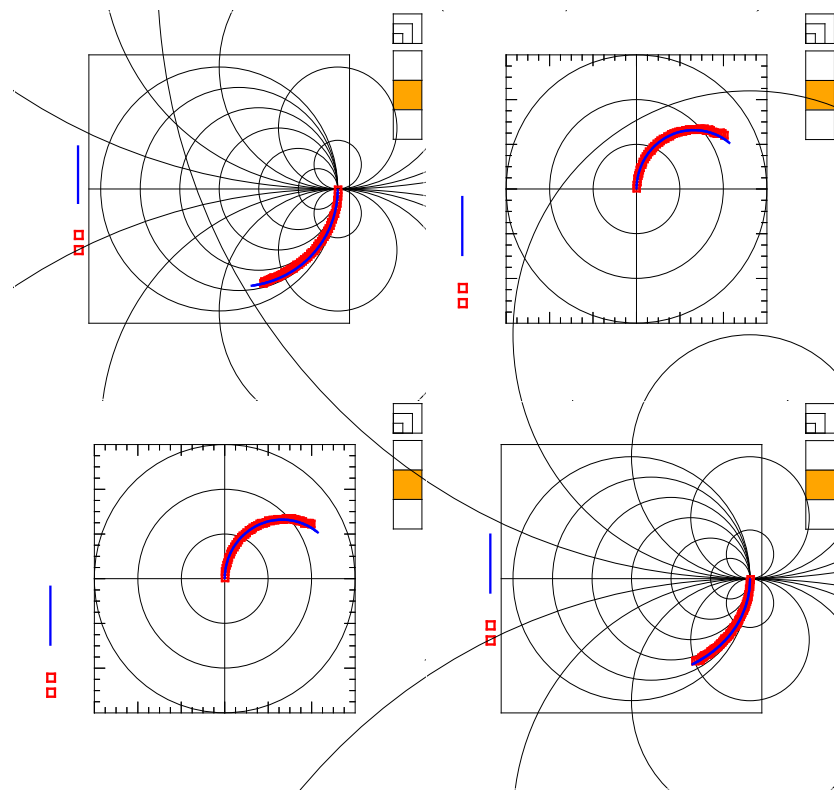
Differential inductor



RF characteristics of 0.13 μm SOI standard Inductor with $N=5.5$, $W=9\mu\text{m}$, $S=2\mu\text{m}$, $D=255\mu\text{m}$.

◆ We have extracted RF Device Model for 0.13 um SOI Technology.

Device	<ul style="list-style-type: none">• MOS (TB, HB) , Inductor, Resistor,• Varactor, MIM, MOM
Level	<ul style="list-style-type: none">• 70 (BSIM4SOI)
Effects	<ul style="list-style-type: none">• FBE/GIFBE, SHE, Gate-leakage, GIDL
Geometry	<ul style="list-style-type: none">• Core: L[0.13~0.75um], W[1.5~8um]• IO: L[0.35~0.75um], W[1.5~8um]
Temp.	<ul style="list-style-type: none">• -55~125°C
Voltage	<ul style="list-style-type: none">• Gate: [-1.32~1.32V](core) / [-3.63~3.63V](IO)• Drain: [0~1.32V](core) / [0~3.63V](IO)
Corner	<ul style="list-style-type: none">• TT, FF, SS, FS, SF



Simulation result of RF NMOS

Application of SOI Model



- ◆ 0.13 um SOI model was applied to SOI Library and ASIC circuit design.
- ◆ The model has become an important part of 0.13 um SOI technology platform, which provides a powerful guarantee for the SOI high reliability circuit design.



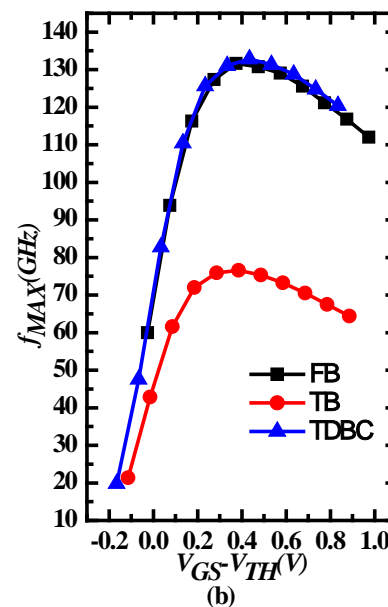
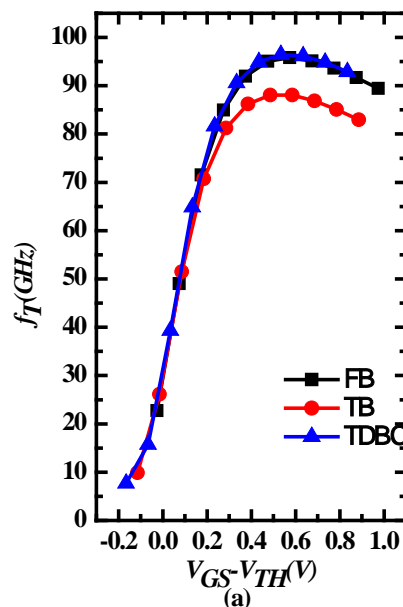
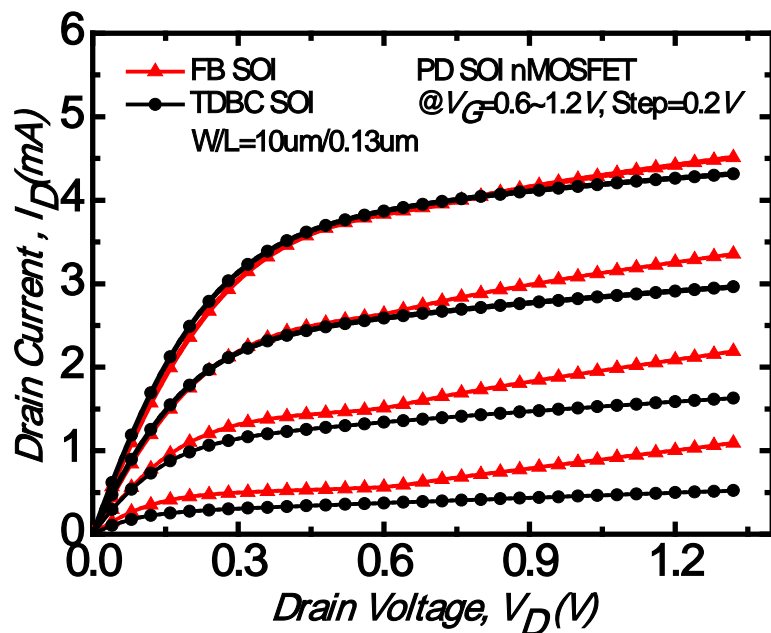
ASIC Chip Verification

Chip Parameters	Performance
Working Frequency	50Mhz
Chip Scale	> 2M gates
Chip Area	8mm x 9mm
Dynamic Power	250mA

Novel Body Contact Structure



- ◆ TDBC SOI devices without floating-body effects are successfully demonstrated, which represent an improvement of 10% for the f_T and of 90% for the f_{MAX} compared with conventional T-gate body-contact devices.



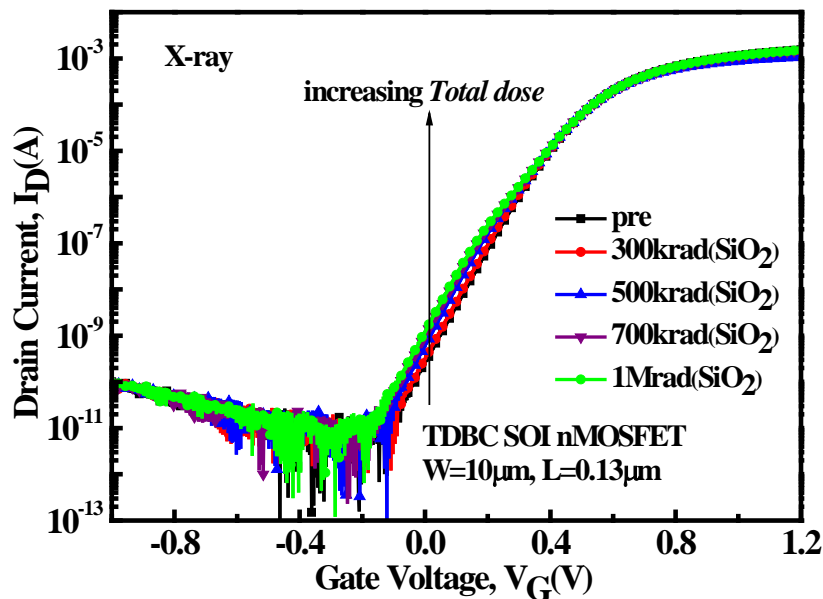
Kink are perfectly suppressed in TDBC devices

Superior RF performance of TDBC devices

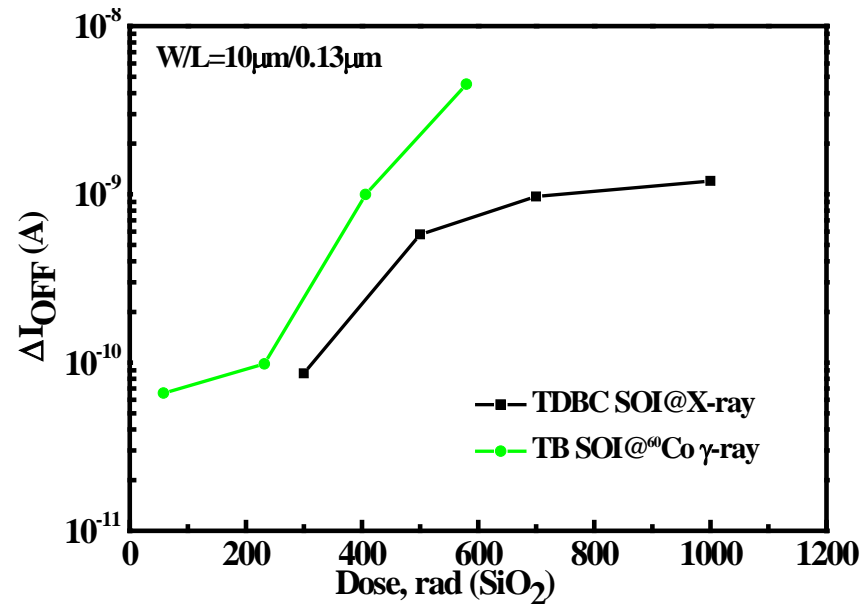
- Jing Chen, Jiexin Luo et al., *IEEE Electron Device Letters*, 32(10), 1346, 2011
- Jiexin Luo, Jing Chen et al., *IEEE Transactions on Electron Devices*, 59(1), 101, 2012
- Kai Lu, Jing Chen et al., *IEEE Electron Device Letters*, 35(1), 15, 2014

Total Dose Effects of TDBC Device

- ◆ TDBC contact makes these SOI transistors strongly resistant to back channel radiation effects.



Total Dose Effects of TDBC SOI Ncore



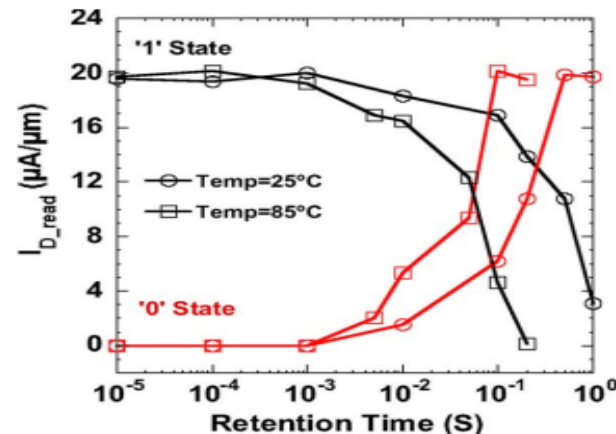
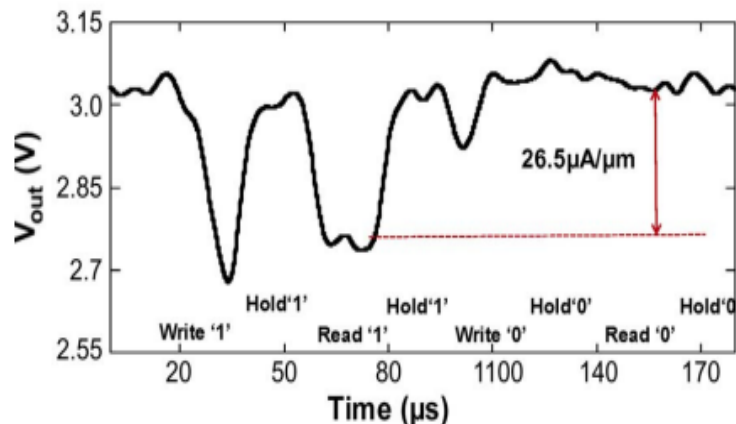
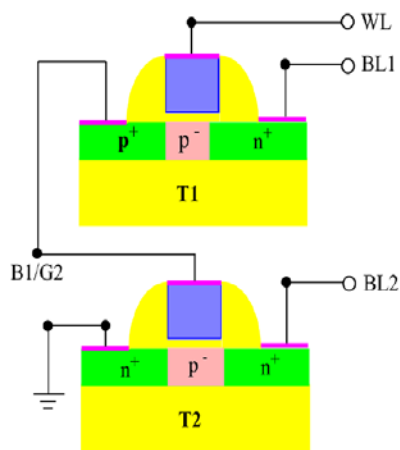
Total Dose Effects of TDBC and TB SOI

Cooperated with E. X. Zhang and D. M. Fleetwood, Vanderbilt University, USA

Jiexin Luo, Jing Chen et al., *IEEE Transaction on Nuclear Science*, 61(6), 11, 2014

Floating-Body/Gate Cell

- ◆ We have experimentally demonstrated a novel capacitorless DRAM cell named FBGC on planar SOI CMOS technology .
- ◆ FBGC has large noise margin and long retention time, also shows excellent endurance nondestructive read characteristics and low-power operation.



Schematic structure of FBGC

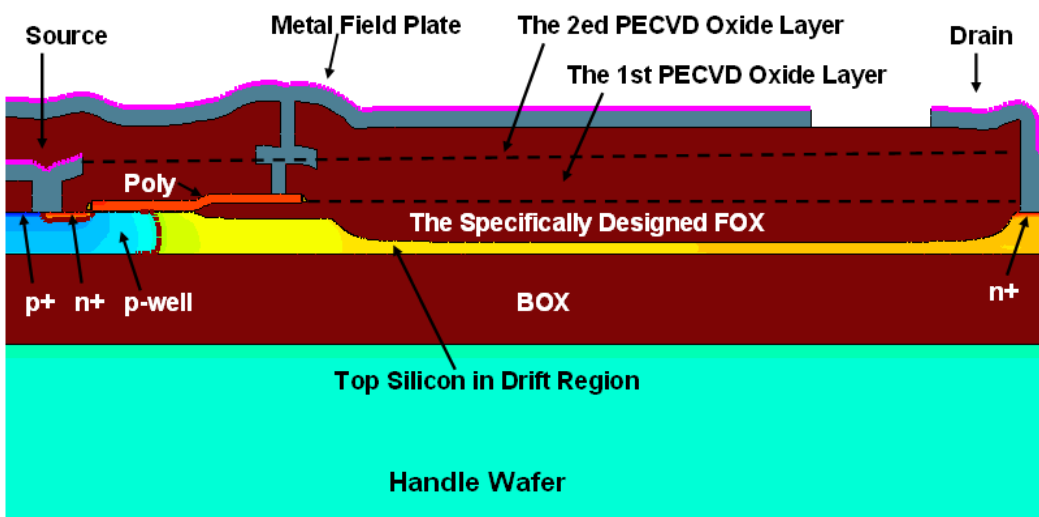
FBGC has large noise margin (26.5uA/um) and long retention time (560ms)

Cooperated with Zhichao Lu and Jerry G. Fossum, University of Florida, USA

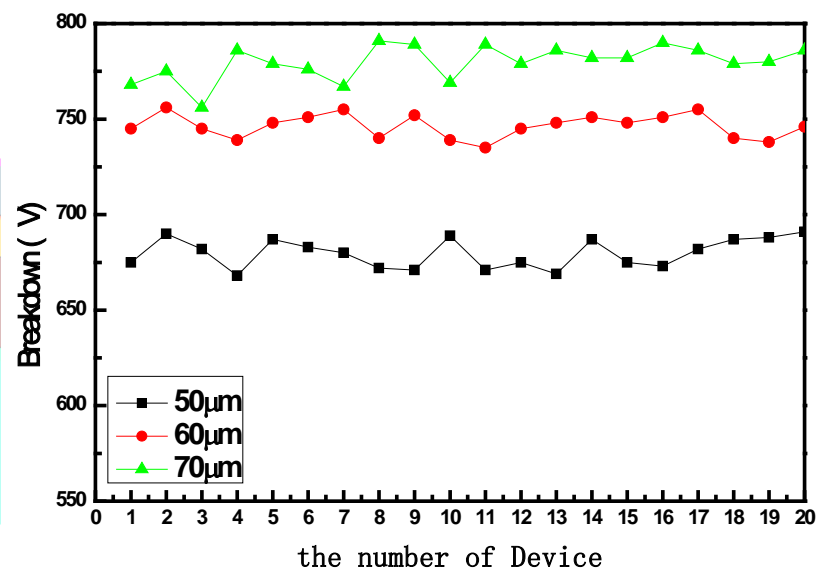
Qingqing Wu, Jing Chen et al., *IEEE Electron Device Letters*, 33 (6), 743, 2012

SOI LDMOS device

- ◆ SOI LDMOS devices was successfully fabricated, the off-state breakdown voltage can reached to 750V.



Schematic structure of SOI LDMOS

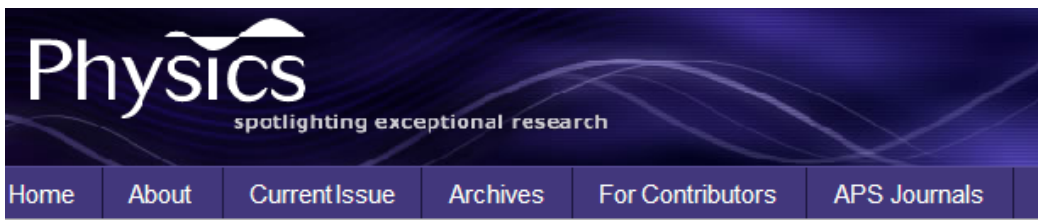


The off-state breakdown voltage of SOI LDMOS

Zhongjian Wang, Xinhong Cheng et al., *Microelectronic Engineering*, 91, 102, 2012

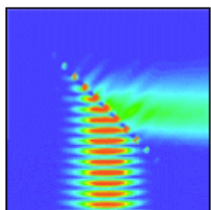
- ◆ It is expected to find applications in designing compact optical components to achieve the on-chip beam steering in photonic circuits.

**Physical Review Letters
(2011.5.20), Editor's Suggestion**



APS » Journals » Physics » Synopses » Sharp turn ahead for light beams

Sharp turn ahead for light beams



Credit: J. Du et al., Phys. Rev. Lett. (2011)

Optical Beam Steering Based on the Symmetry of Resonant Modes of Nanoparticles

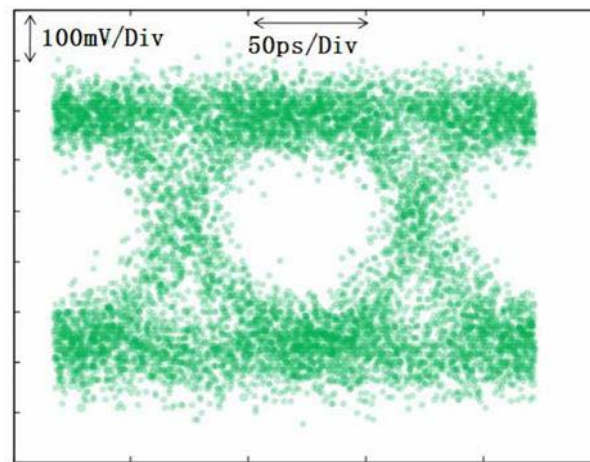
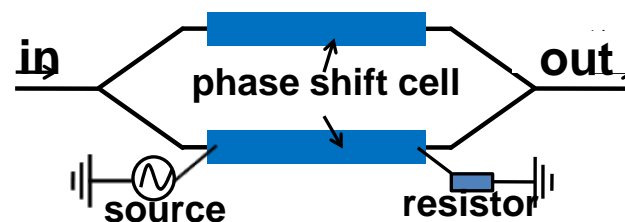
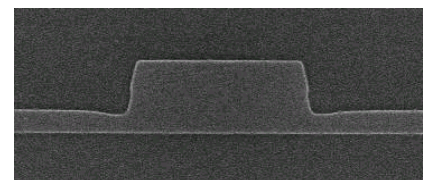
Junjie Du, Zhifang Lin, S. T. Chui, Wanli Lu, Hao Li, Aimin Wu, Zhen Sheng, Jian Zi, Xi Wang, Shichang Zou, and Fuwan Gan

Phys. Rev. Lett. **106**, 203903 (Published May 20, 2011)

Optics

Over the last decade, the field of optics has been turned on its head by artificial materials that bend light in ways that no natural material can. In a new development, theorists have shown that a carefully designed array of tiny rods can deflect a light beam at a sharp angle. As explained in *Physical Review Letters*, this unique light response is due to interference in

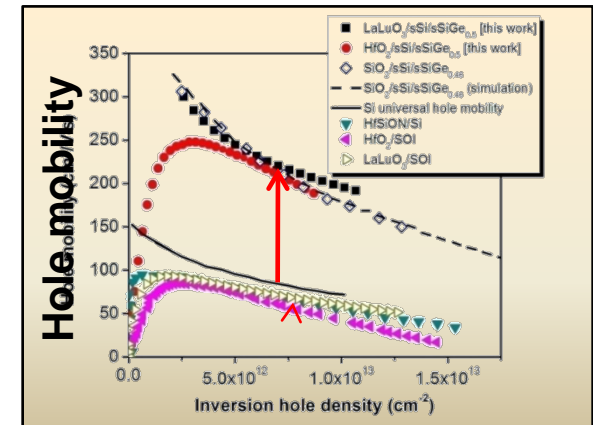
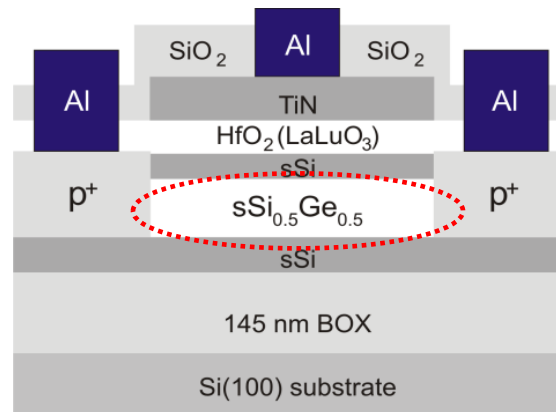
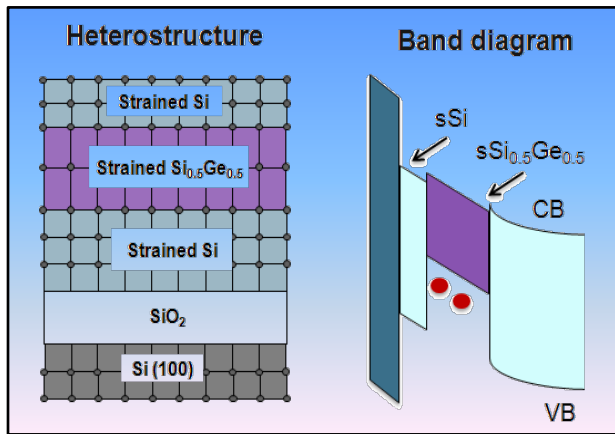
✓ APS special reported



✓ 10Gbps transfer speed

High-K SiGe/SOI quantum well

- ◆ Epitaxial growth of strain silicon substrates was achieved via an Al interlayer mediated epitaxial. The hole mobility is 2.5X larger than Bulk channel.



✓ sSi/sSiGe/sSOI substrate

✓ Carriers are confined in sSiGe

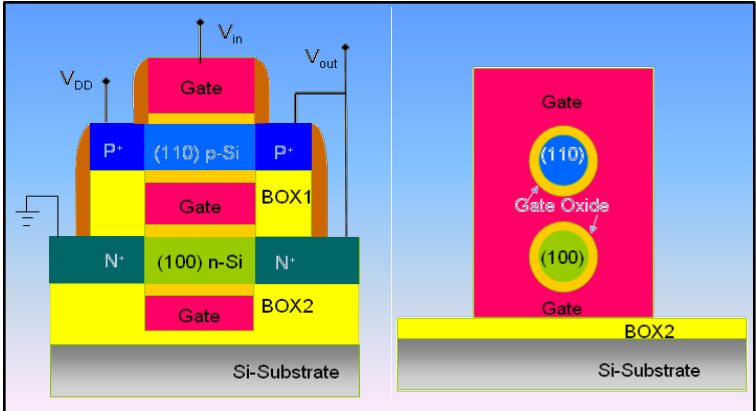
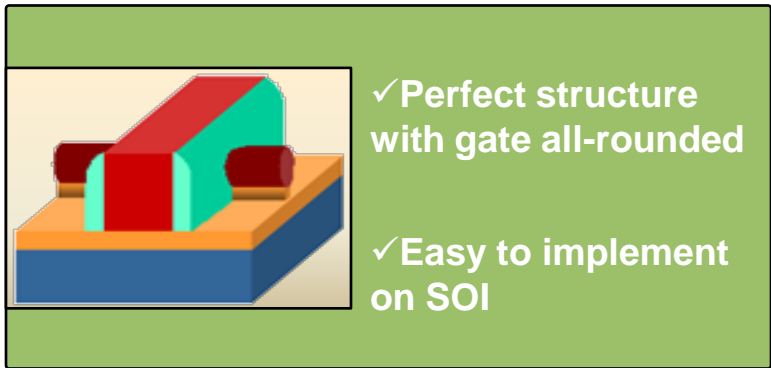
✓ 2.5X larger than Bulk channel

Cooperated with Juelich Research Center, Germany

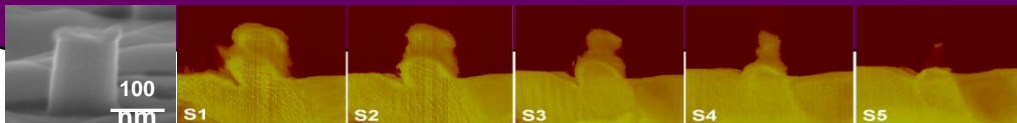
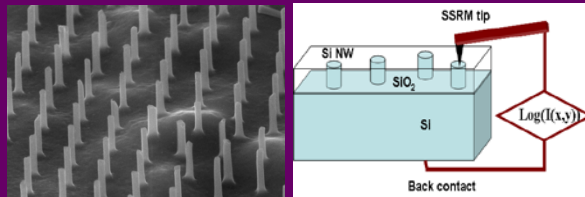
- Bo Zhang et al., *Applied Physics Letters*, 98, 252101 (2011)
- Bo Zhang et al., *Solid-State Electronics*, 62(1), 185, 2011

Nanowire on SOI

- ◆ SSRM has been used to characterize doping in silicon nanowire for the first time. The GAAC FinFET appears to be a good potential candidate for scaling down to sub-10 nm sizes.



SSRM (Scanning Spreading Resistance Microscopy)



Cooperated with Forschungszentrum Dresden-Rossendorf, Germany

✓ Nanowire on Hybrid orientation SOI

• **Xiao Deyuan et al., *Journal of Semiconductors*, 30(1), 2009**

• **Xin Ou et al., *Advanced Materials*, 22(36), 4020, 2010**

• **Xin Ou et al., *Nano Letters*, 10(1), 171, 2010**



- **Introduction of SOI Group**
- **Research results**
 - ✓ **DC Device Model**
 - ✓ **RF Device Model**
 - ✓ **Research of SOI Device**
 - ✓ **Fruits of international cooperation**
- **Summary**

SOI Group

- The leading SOI research teams in China are actively driving new SOI technology development, help to build up SOI ecosystem.

Device Modeling

- We have extracted a complete Model for 0.13 um SOI technology, which was applied to SOI Library and ASIC circuit design.

Research of SOI Device

- We have designed TDBC SOI device, FBGC Cell, LDMOS, Nanowire, Silicon photonics integrated chip, and so on.

International cooperation

- We have fruits of international cooperation with some famous university in USA and Research Centers in Germany.



Thank you!