Aging Gate Delay Model at Logic Circuit under NBTI Effect

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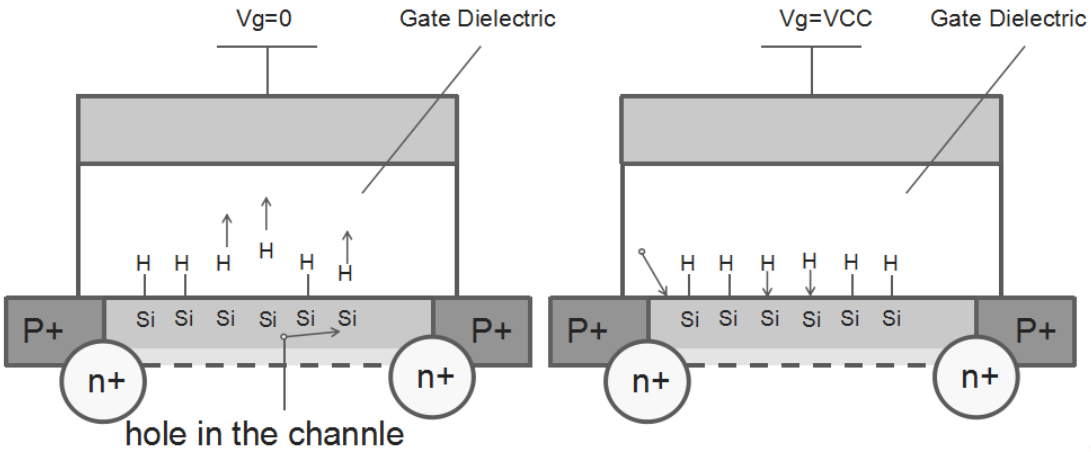
contents

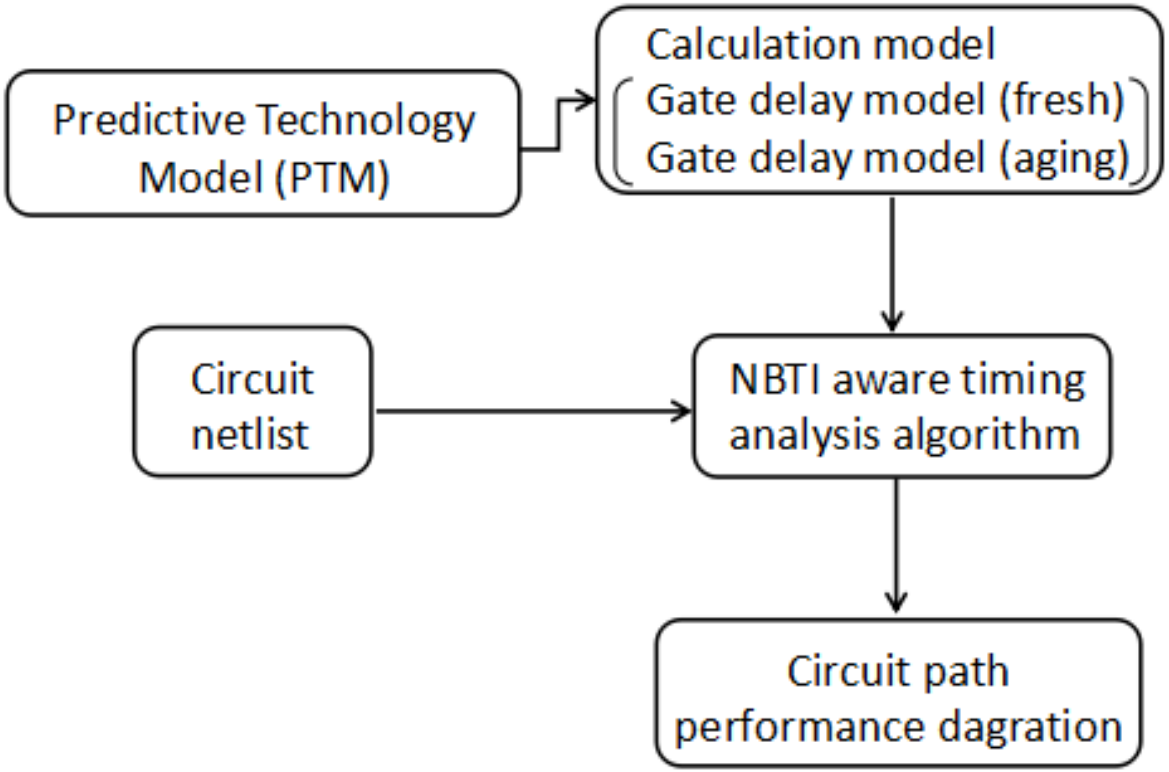
Introduction

The NBTI effect driving the decline in current and transconductance, subthreshold slope increasing and threshold voltage shift, will increase propagation delay of combinational circuits .
Under NBTI effect, the threshold voltage of the PMOS transistor increases and causes the degradation of logic gates and eventually leads to the timing violations.



reaction-diffusion (R-D) theory
Reaction: Si–H or Si–O bonds at the substrate/gate oxide interface are broken
Diffusion: reaction-generated species diffuse away from the interface toward the gate
trapping/detrapping (T/D) theory
Trapping: in electric field, charge in the SiO_2 interface is captured by the defects in the oxide
Detapping: removing electric field, the charge trapping breakaway from oxidation layer.

NBTI timing analysis framework



The long-term prediction model

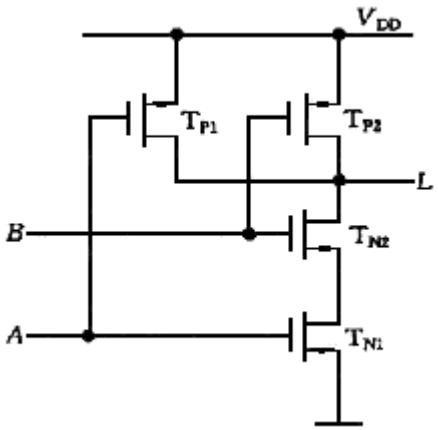
ΔV_{th} for periodical input pattern

ΔVth	$\left(\frac{\sqrt{k_v^2 \alpha T_{clk}}}{1-\beta_e^{1/2n}}\right)^{2n}$		
β_e	$1-\frac{2\varepsilon_1 te+\sqrt{\varepsilon_2 C(1-\alpha)T_{clk}}}{2tox+\sqrt{Ct}}$		
K_v	$\left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)^3 K_1^2 C_{ox}(V_{gs}-V_{th})\sqrt{C}\exp(\frac{2E_{ox}}{E_{o1}})$		
C	$\exp(-E_a/kT)/T_o$		
Ea(eV)	0.49	$K_1(C^{-0.5}nm^{-2.5})$	3×10^4
ε_1	0.9	$T_o(s/nm^2)$	10^{-8}
ε_2	0.5	$E_{o1}(V/nm)$	0.335

n : time exponent (1/6 for H_2 diffusion)
C : temperature dependence factor
Ea : activation energy of hydrogen species
k : Boltzmann constant
Eox : vertical electrical field
T_o ,K_1 , E_o : temperature and process dependent constants
T_{clk} : time period of one stress-recovery cycle
α : duty cycle is the ratio of the time spent in stress to time period
βe : the fraction parameter of the recovery

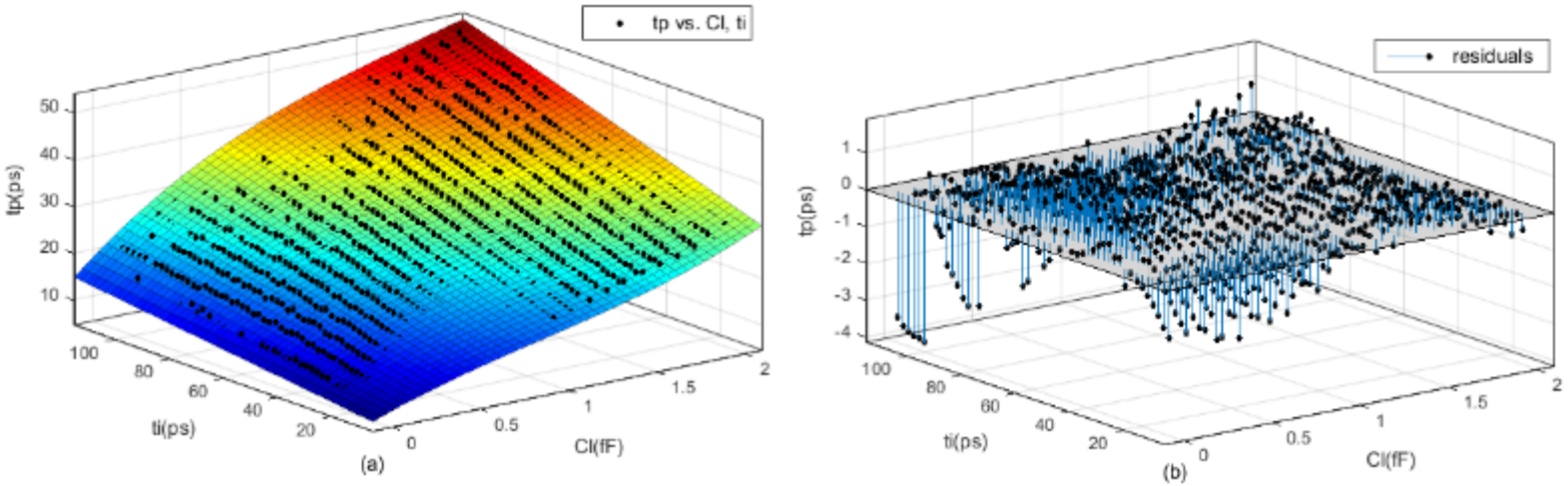
Obtain experimental data

NAND



All transistors use 45-nm PTM model.
pmos:180nm/45nm
nmos:90nm/45nm
VDD:1.1V
T_A:8ns
T_B:4ns
α:0.5

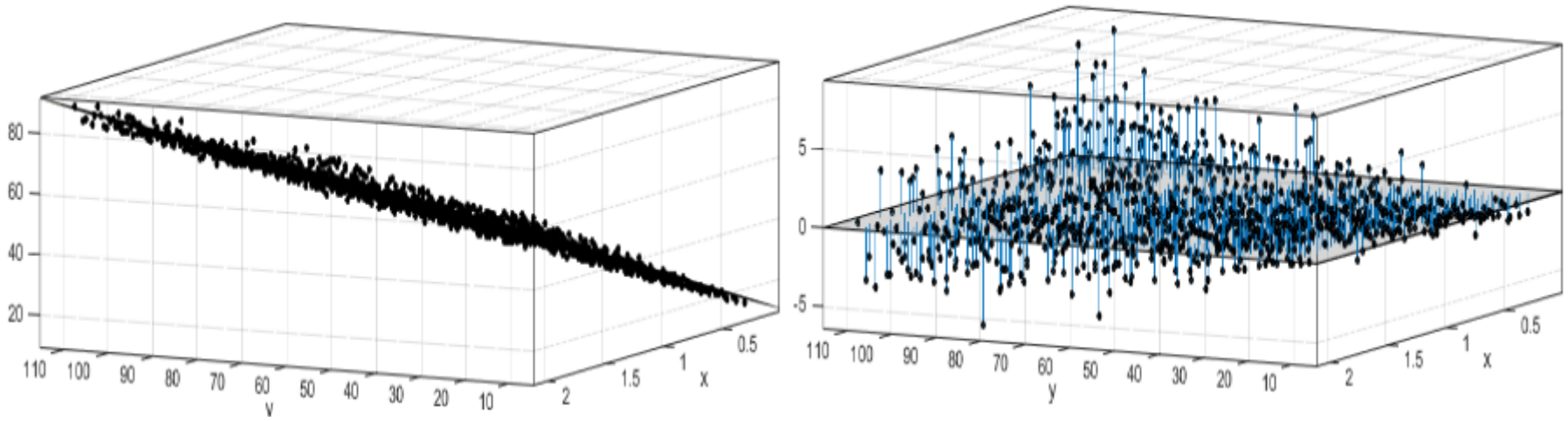
NAND Gate Delay Model without Degradation



(a) The model of tp without degradation and the simulated results
(b) the residuals of tp between model and the simulations

C_L(load capacitor)： 0fF ~ 2fF
t_i(input slew rate)： 10ps ~ 110ps
t_p(gate delay) ： 3ps ~ 53ps

NAND Gate Delay Model without Degradation



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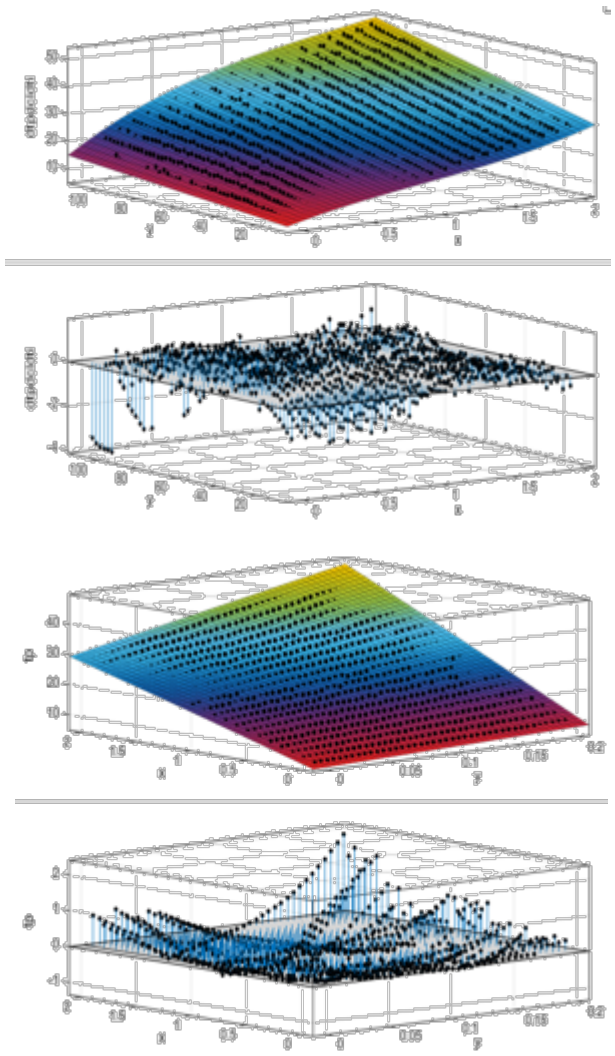
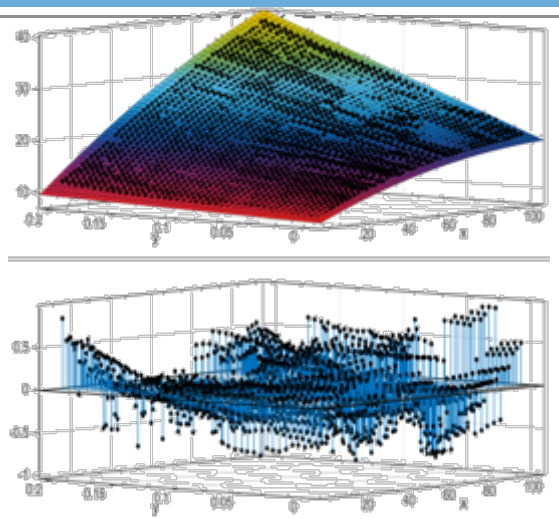
NAND Gate Delay Model without Degradation

$$t_{p,fresh}=a_0+b_1\cdot C_L+b_2\cdot C_L^2+b_3\cdot C_L^3+c_1\cdot ti+e_1\cdot C_L\cdot t_i+e_2\cdot C_L^2\cdot t_i \quad (1)$$

$$t_{o,fresh}=h_0+i_1\cdot C_L+j_1\cdot t_i \quad (2)$$

NAND Gate Delay Model with Degradation





$t_{p,fresh}\ (C_L, t_i)$

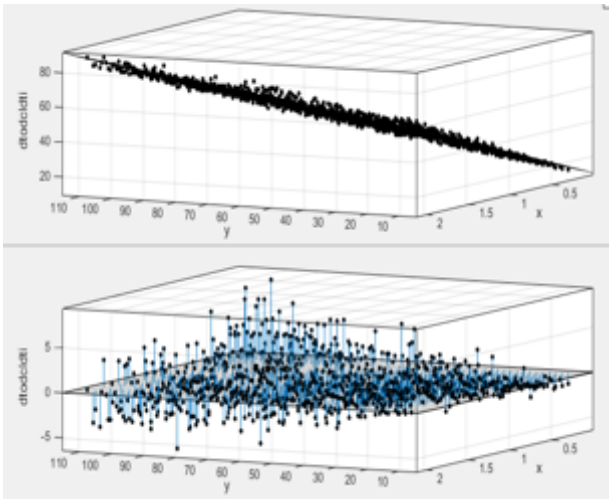
$t_{p,aging}\ (\Delta V_{th}, t_i)$

$t_{p,aging}\ (\Delta V_{th}, C_L)$

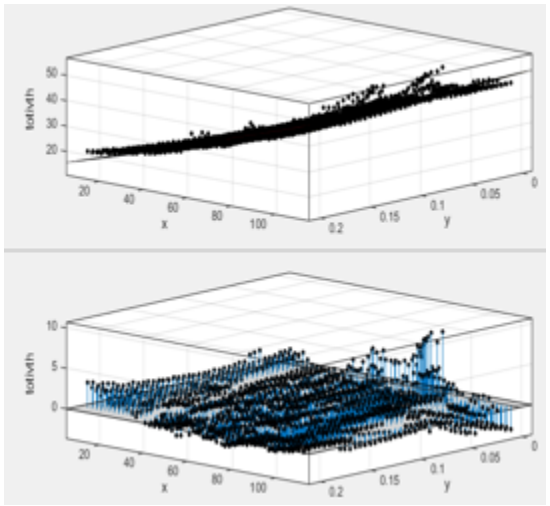
Aging Gate Delay Model

Details of the process

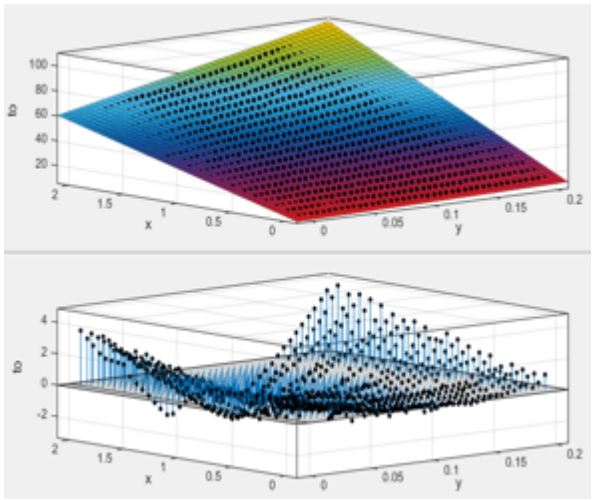
$t_{o,fresh}(C_L, t_i)$



$t_{o,aging}(\Delta V_{th}, t_i)$



$t_{o,aging}(\Delta V_{th}, C_L)$



Aging Gate Delay Model

2,Fitting

NAND Gate Delay Model with Degradation

$t_{p,fresh}(C_L, t_i)$
$t_{p,aging}(\Delta V_{th}, t_i)$
$t_{p,aging}(\Delta V_{th}, C_L)$

→ $t_{p,aging}(C_L, t_i, \Delta V_{th})$

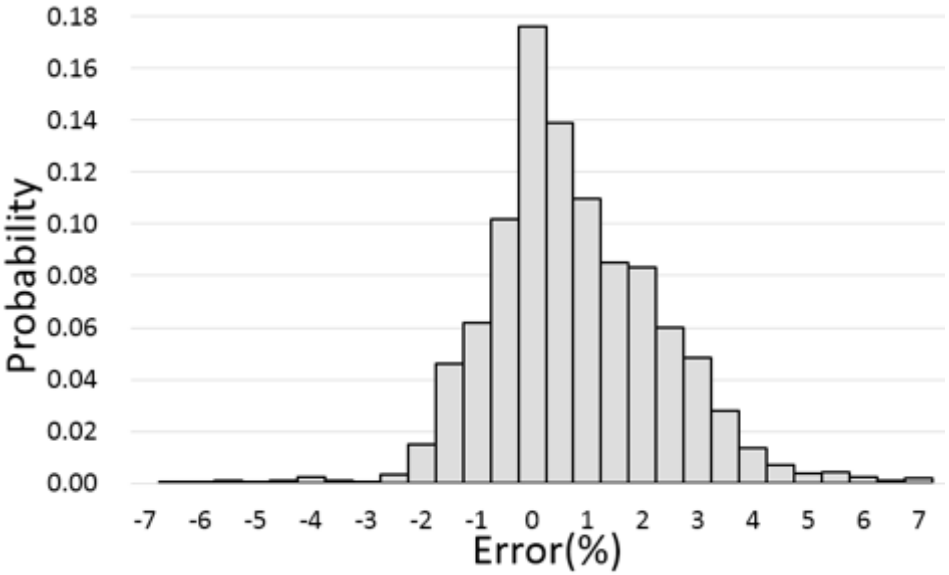
1,keepping common item
2,adding correction item for every factor
3,running genetic algorithm of Random 7000 sets of data to get coefficient

$t_{o,fresh}(C_L, t_i)$
$t_{o,aging}(\Delta V_{th}, t_i)$
$t_{o,aging}(\Delta V_{th}, C_L)$

→ $t_{o,aging}(C_L, t_i, \Delta V_{th})$

Aging Gate Delay Model

The distribution of error between simulation and calculation of $t_{p,aging}$



Fresh propagation delay:

$$t_{p,fresh}=a_0+b_1\cdot C_L+b_2\cdot C_L^2+b_3\cdot C_L^3+c_1\cdot ti+e_1\cdot C_L\cdot t_i+e_2\cdot C_L^2\cdot t_i \quad (1)$$

$$t_{o,fresh}=h_0+i_1\cdot C_L+j_1\cdot t_i \quad (2)$$

Aged propagation delay:

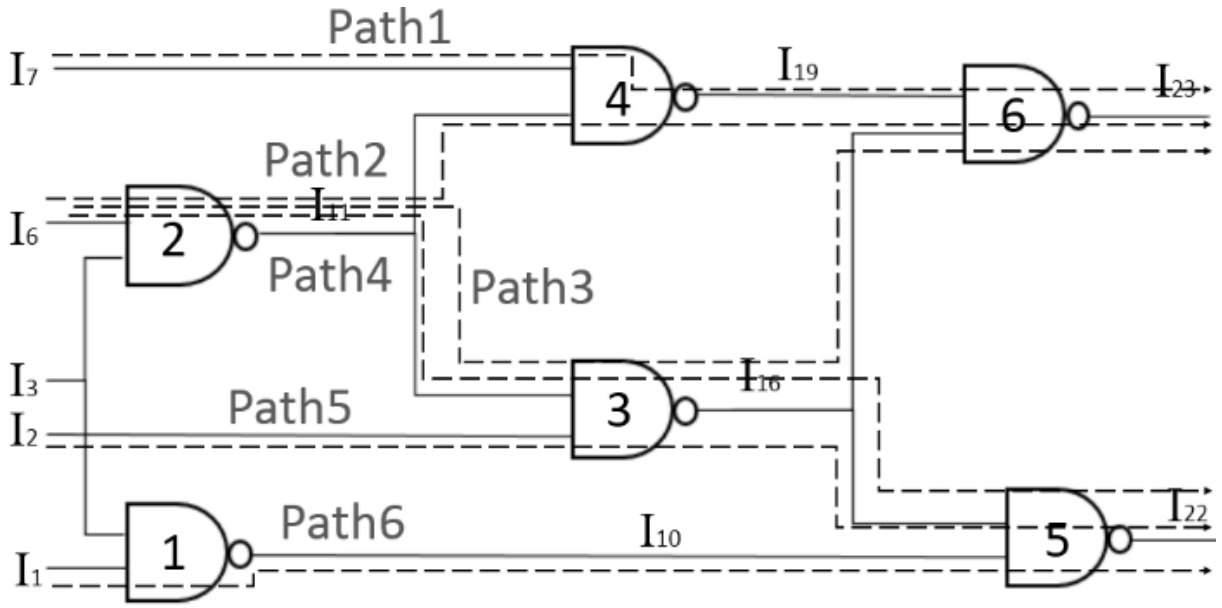
$$t_{p,aging}=a_0+b_1\cdot C_L+b_2\cdot C_L^2+b_3\cdot C_L^3+c_1\cdot t_i+c_2\cdot t_i^2+d_1\cdot \Delta V_{th} +e\cdot C_L\cdot t_i+f\cdot \Delta V_{th}\cdot C_L+g\cdot \Delta V_{th}\cdot t_i \quad (3)$$

$$t_{o,aging}=h_0+i_1\cdot C_L+j_1\cdot t_i+k_1\cdot \Delta V_{th}+l\cdot \Delta V_{th}\cdot t_i+m\cdot C_L\cdot \Delta V_{th} \quad (4)$$

Path delay calculation framework

Validation and Discussion

circuit netlist of C17 in ISCAS85 and the path



The input patterns:

Input slew rate is 20ps .

Input duty-cycle of {I_1 , I_2 , I_3 , I_6 , I_7 } are {0.5,0.5, 0.5, 0.5, 0.33} .

Period of {I_1 , I_2 , I_3 , I_6 , I_7 } are {8ns, 4ns, 4ns, 8ns, 3ns}.

The gate degradation ΔV_{th} is 0.05V

Summary

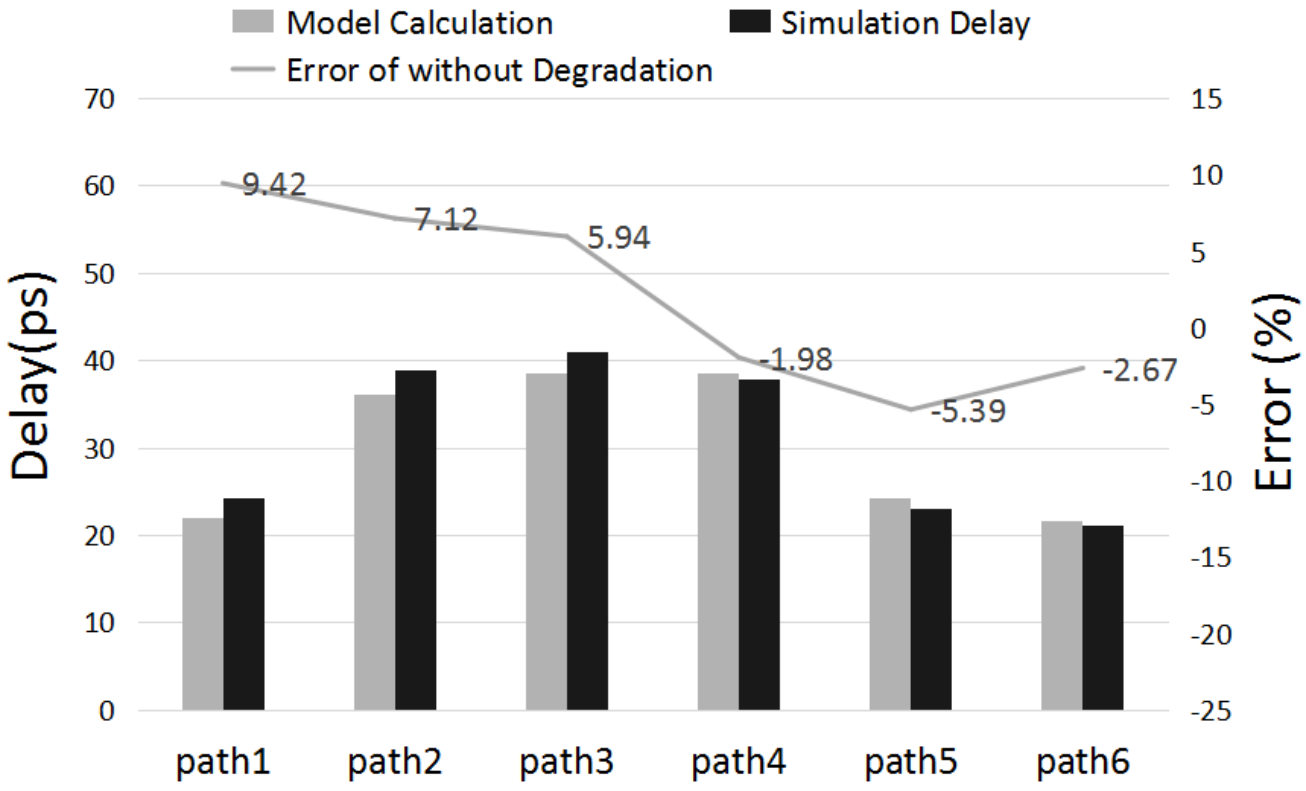
1 Analyzed the time delay under the effect of NBTI in combinational logic circuit.

2 Using the curve fitting toolbox and the genetic algorithm to explore the propagation delay model with the NBTI considered.

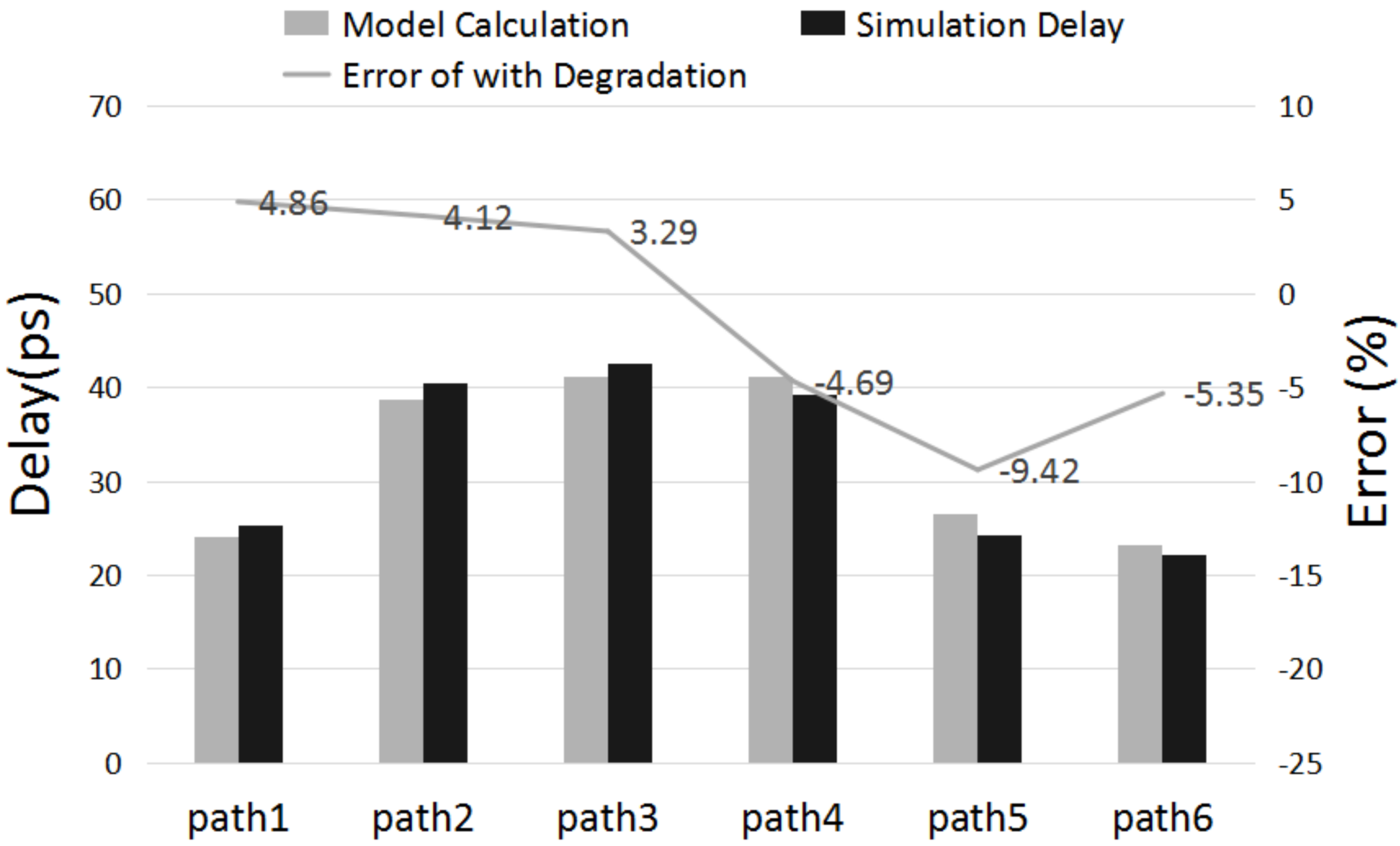
3 This method will also be extended to other logic gates.

Validation and Discussion

The calculations of the delay model without and with degradation for C17 benchmark circuit.



The histogram represents the path delay .
The lines represent the relative errors between the calculation


Model Calculation
Simulation Delay
Error of with Degradation
Delay(ps)
Error (%)
70
60
50
40
30
20
10
0
10
5
0
-5
-10
-15
-20
-25
4.86
4.12
3.29
-4.69
-9.42
-5.35
path1
path2
path3
path4
path5
path6

Question Time

Thanks!

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