# Wafer-Level Calibration & Verification up to 750 GHz

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**2016**

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# Outline

- LRRM vs SOLT
- Calibration Verification
- Over-temperature RF calibration
- 110 GHz 4 port Calibration & Validation
- Sub-THz Wafer Level VNA Calibration


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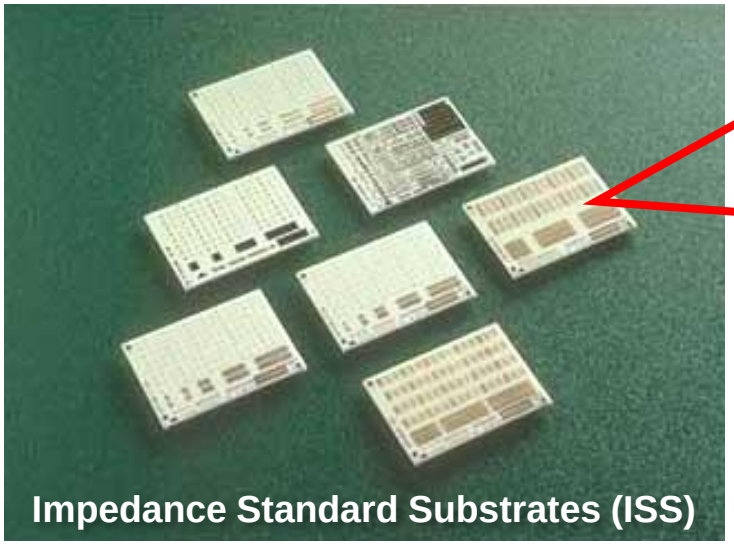
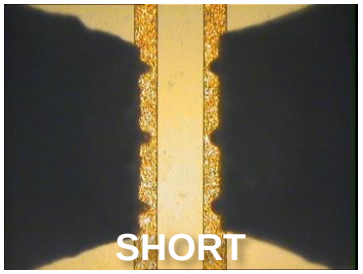
# On-Wafer RF Measurements


Air Coplanar Probes


Probes with Microstrip Design

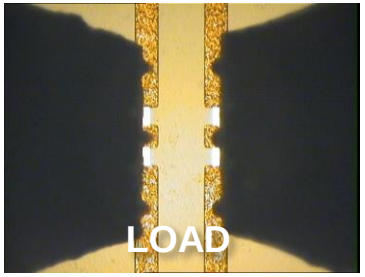


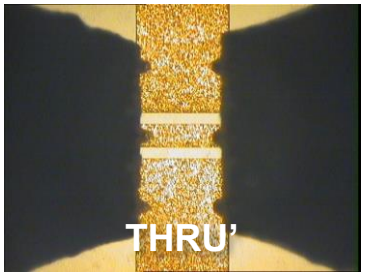
Impedance Standard Substrates (ISS)




Electrical behavior

- standard dimensions
- probe pitch
- probe placement





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# The Need for VNA Calibration


- **Systematic Errors**
  - Imperfections in Network Analyzer and Test setup
  - Define the measurement reference plane in a Test setup

- **Random Errors**
  - Vary with time in Random Fashion (Unpredictable)
  - Main Contributors: Instrument noise, switch and connector repeatability.


- **Drift Errors**
  - Due to System performance changing after a calibration has been done.
  - Primarily cause by Temperature Variation
- **When to Recalibrate?**
  - Perform **System Stability Check**


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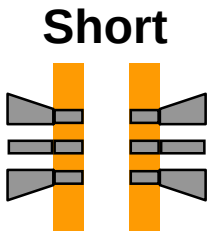
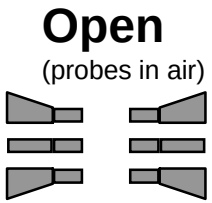
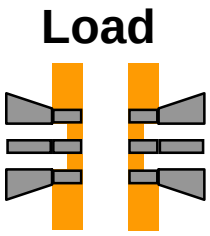
# SOLT Calibration



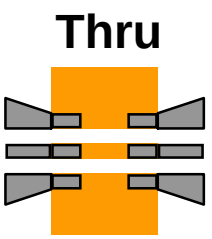

$L_{short}$




$C_{open}$




$L_{term}$




$Delay_{Thru}$

- Oldest calibration technique
- All standards must be perfectly known
  - Available every vector network analyzer (CalKit required)
  - Open has capacitance/Inductances
  - Short and load have inductances
- Cal coefficients are defined for a particular probe placement
- Sensitive to probe placement
- Looks best after calibration
- Forces VNA to correct itself based on Cal Coefficients
- How about over-temperature?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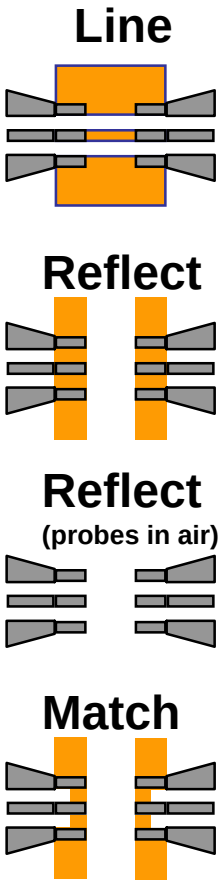
# LRRM Calibration




- Same Standards as SOLT
- Industry Standard verified by NIST
- Line-Reflect-Reflect-Match Calibration
  - Only need to know Thru (line) delay & Match resistance
  - Measurements referenced to trimmed resistor
  - Dynamic Load Inductance Extraction
    - Minimize probe placement sensitivity, providing accurate load inductance extraction
    - Improves the accuracy of reference impedance
- Robust and Accurate
  - Less sensitive to probe placement errors
  - Requires less information about standards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# SOLT vs LRRM Calibration

- Experiment:
  - Infinity probes GSG pitch 100μm Probes
  - ISS 101-190

| Calibration Technique | SOLT | LRRM |
|---|---|---|
| OPEN Capacitance (fF) | -6.5 | Not Required |
| SHORT Inductance (pH) | 3.3 | Not Required |
| Load (Ohm) | 50 | 50 |
| Load Inductance (pH) | -0.4 | Automatically Determined |
| Thru' Delay | 1ps | 1ps |


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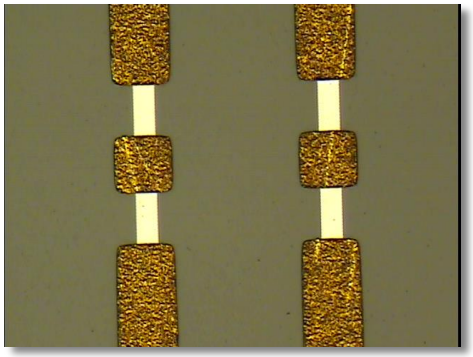
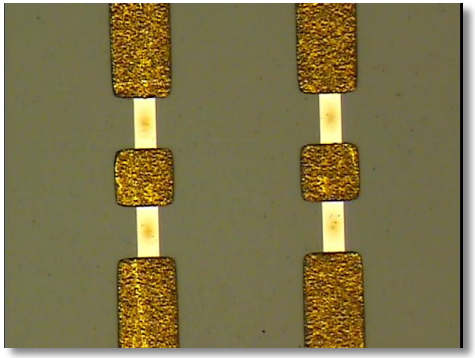
# 50 Ohm and Thru' Standards

- 50 Ohm Standard
  - Use only precision trimmed loads marked on the ISS maps.
  - ±0.3% accuracy.

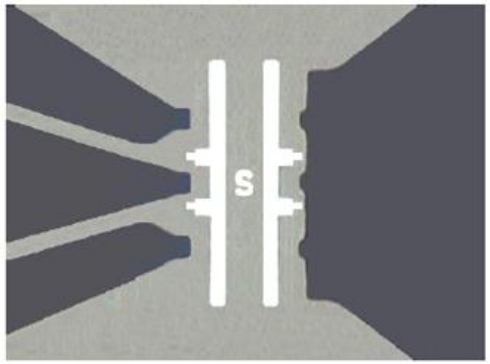


Untrimmed Loads

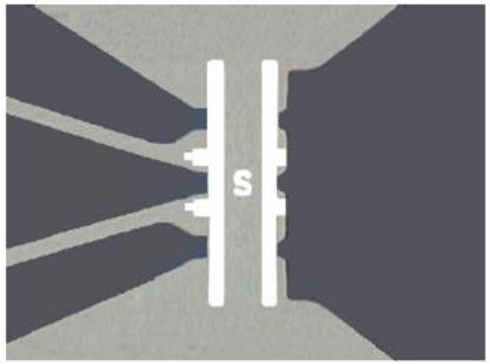


Trimmed Loads

- 1ps Thru' Standard
  - Use alignment marks to maintain correct probe separation distance.




Initial Contact




Final Contact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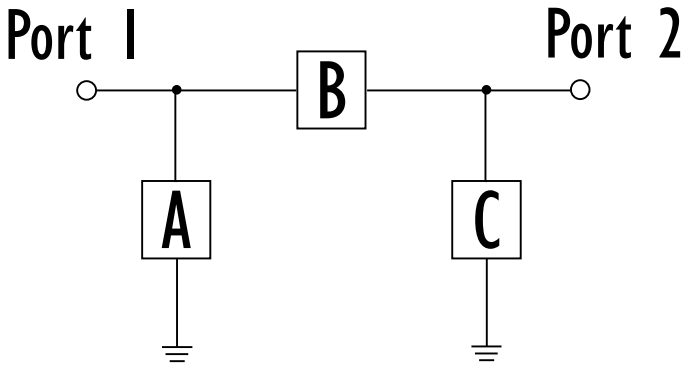
# Measure OPEN & SHORT after LRRM Calibration

- Probes are calibrated using LRRM and then, 2 measurements are made:
  - Probes lifted in the air (OPEN)
  - Separate SHORT standard
- Using $\pi$ network & Admittance (S to Y) parameters to extract OPEN cap and SHORT Inductance




$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} A+B & -B \\ -B & C+B \end{bmatrix}$$

$$A = Y_{11} + Y_{12}$$
$$C = Y_{22} + Y_{21}$$
$$B = -Y_{12} \text{ or } -Y_{21}$$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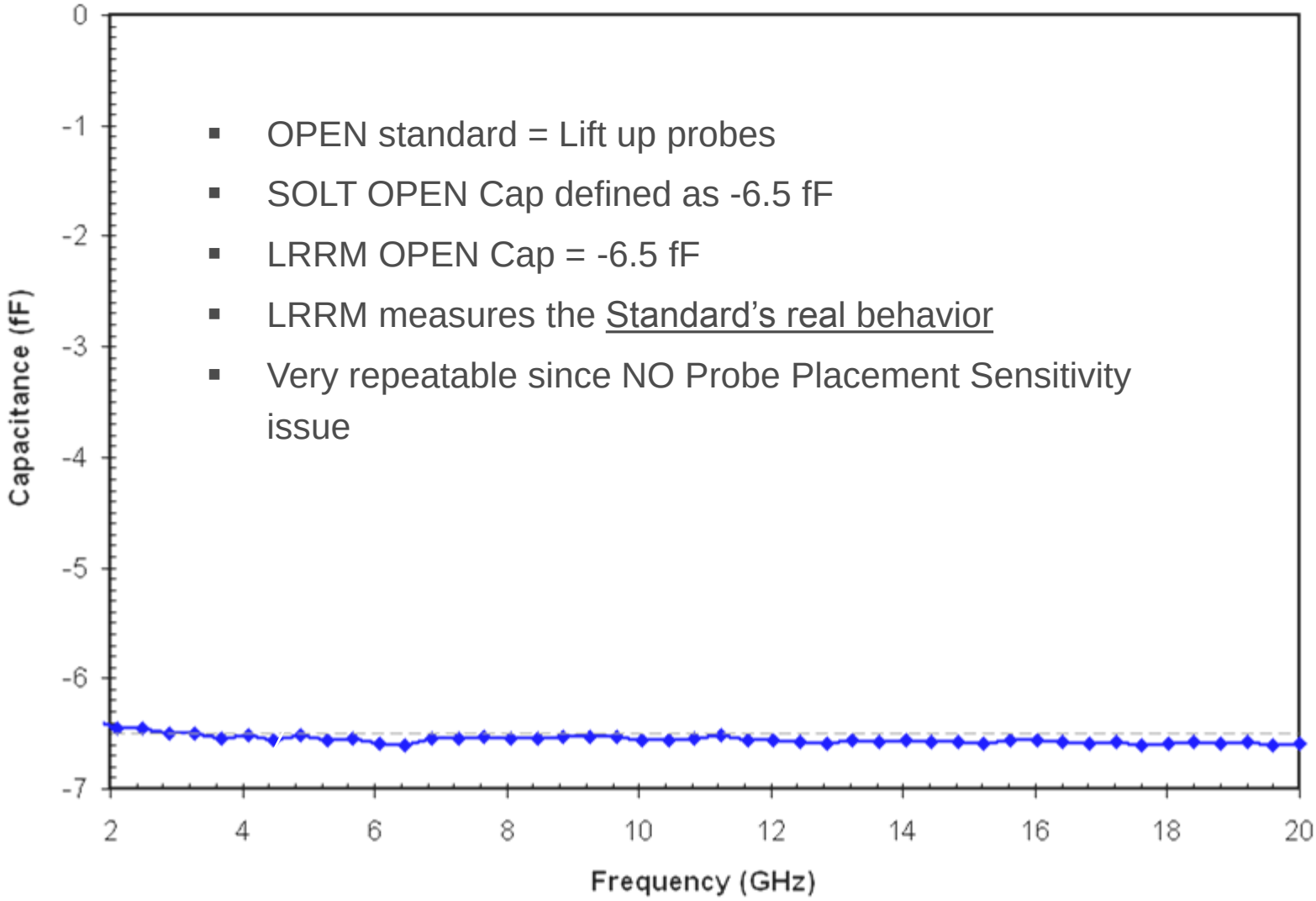
# OPEN Standard measured with LRRM




- OPEN standard = Lift up probes
- SOLT OPEN Cap defined as -6.5 fF
- LRRM OPEN Cap = -6.5 fF
- LRRM measures the Standard's real behavior
- Very repeatable since NO Probe Placement Sensitivity issue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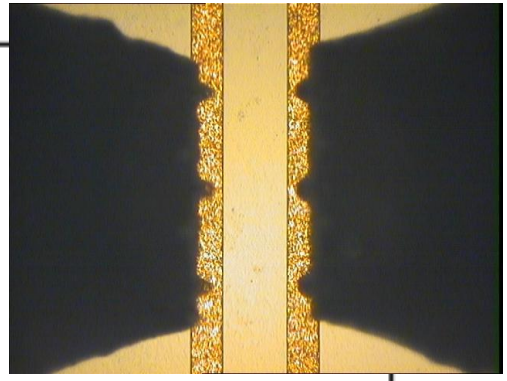
# SHORT Standard measured with LRRM






- SOLT – requires probe on SHORT = 3.3 pH
- LRRM gives actual value
- Slight deviation could be due to
  - Probe Placement Error
  - Worn-out Standard
- Is this critical?
  - Small L – Gate Inductance RFCMOS (pH)
  - Large L – 2nH Inductor, Error ≈ 0.01%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# Calibration Verification


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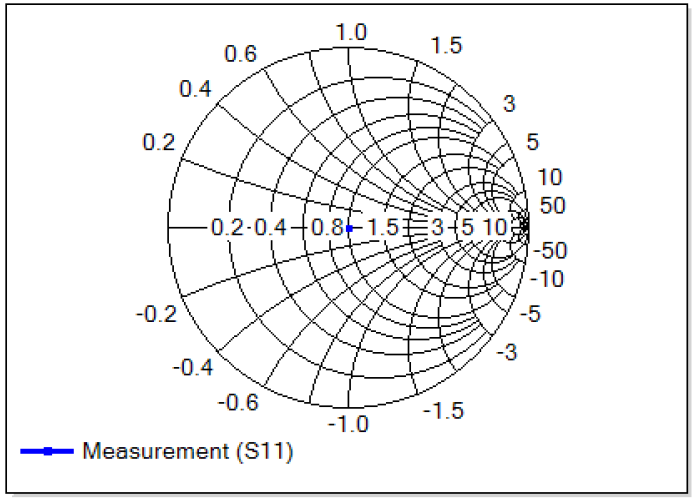
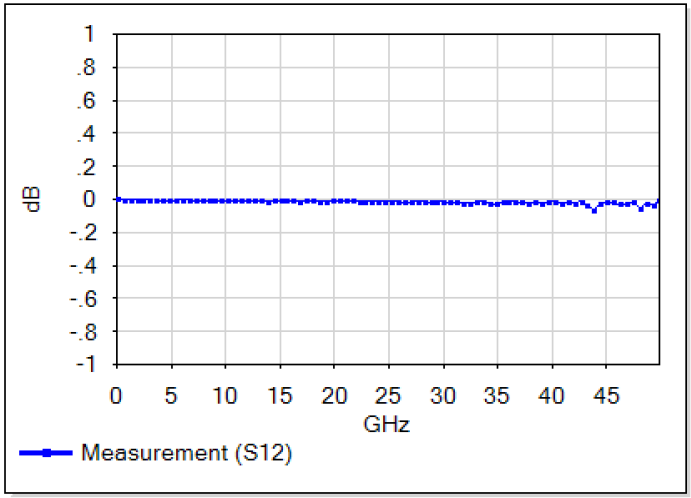
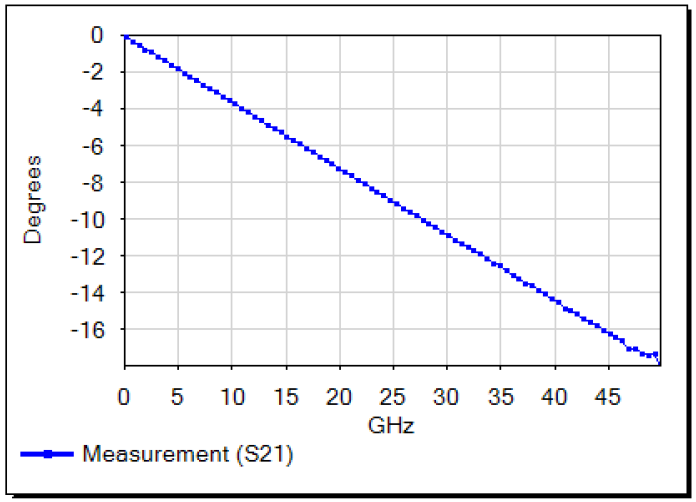
# 1ps Verification Line




3

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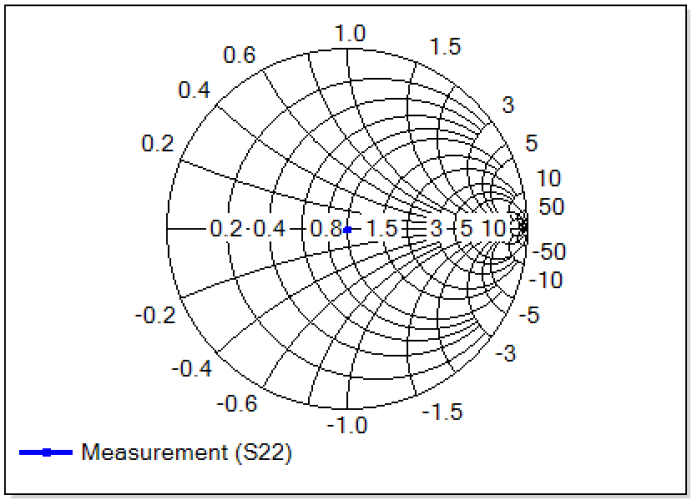



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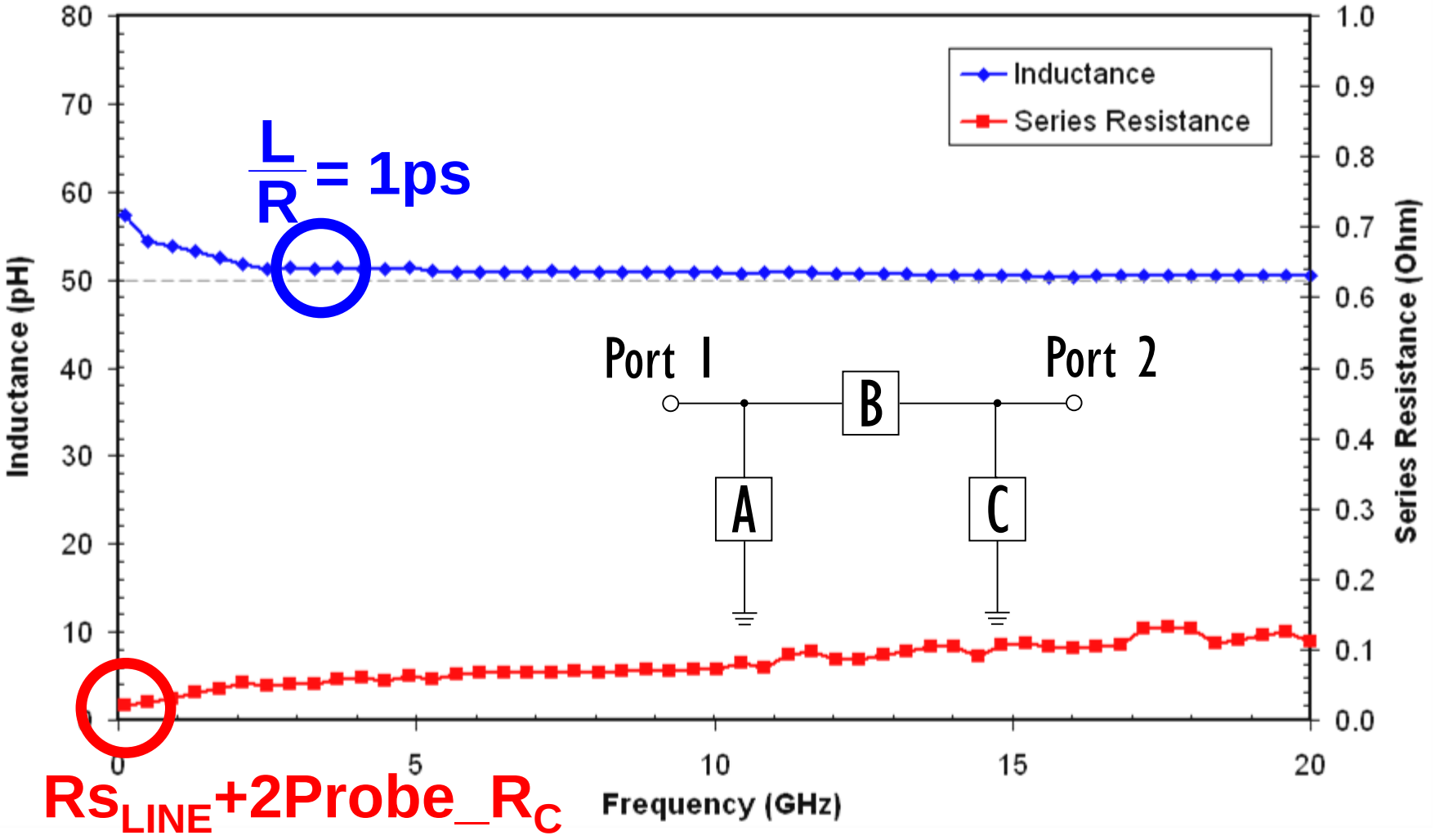



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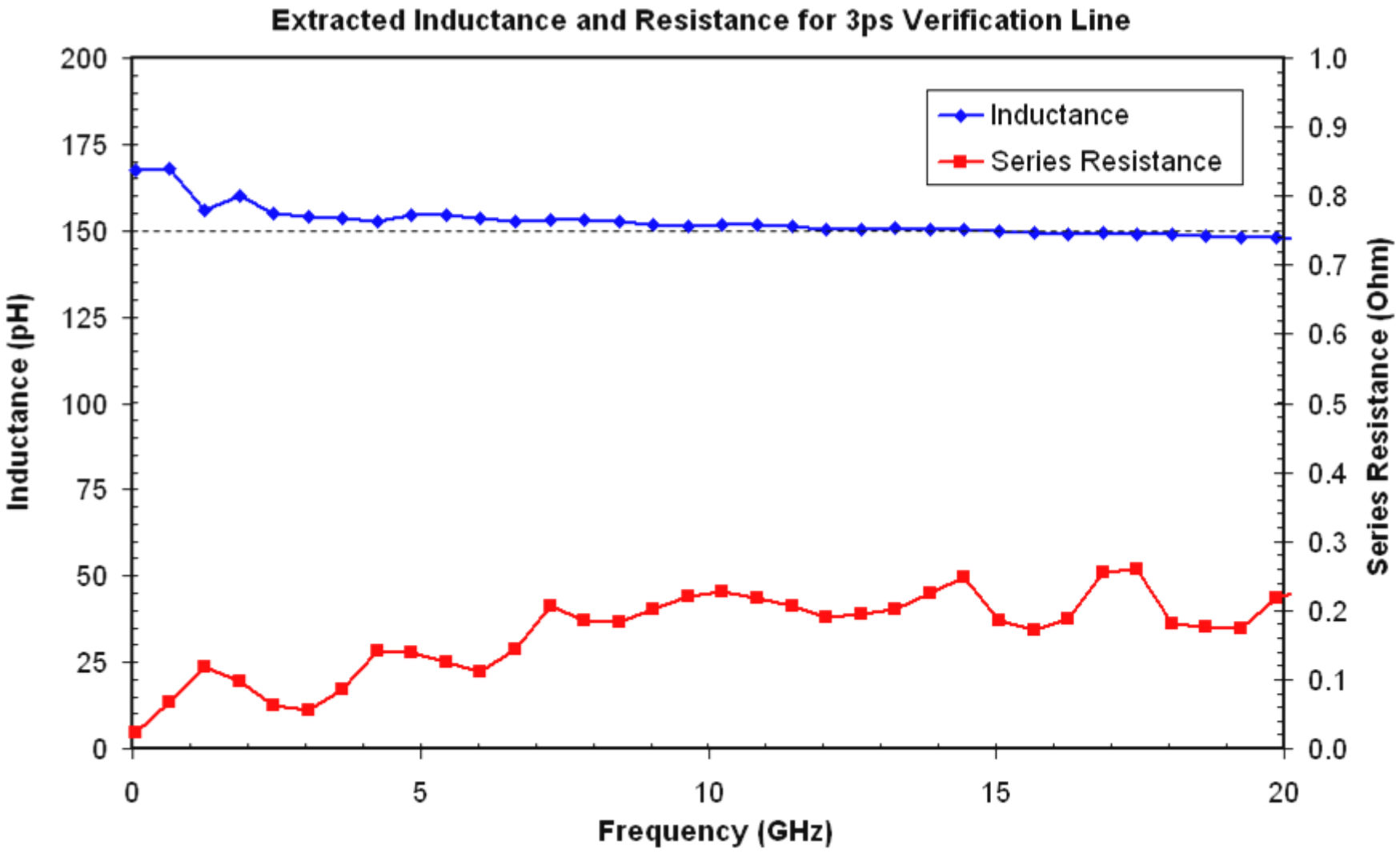
# 3ps Verification Line





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# RF Over-Temperature Calibration


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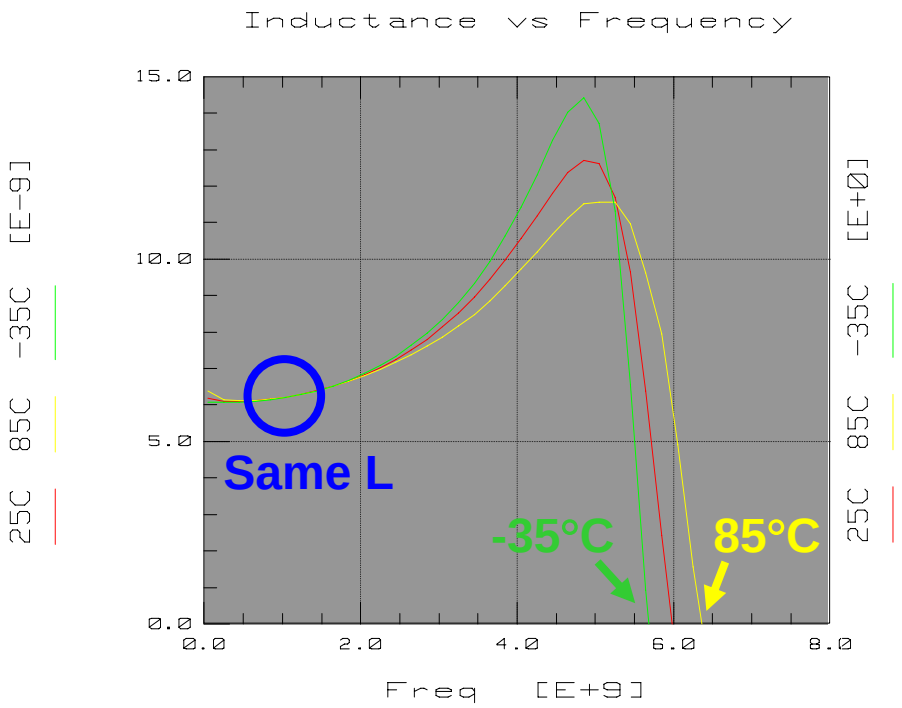
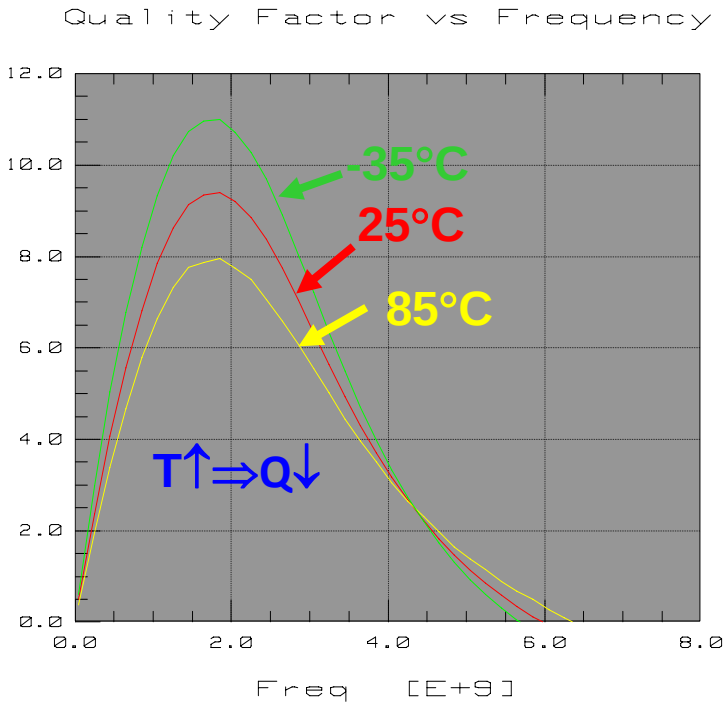
# Example of RF Over-Temperature Device Measurement – Inductor (N5W10D120)




**Inductance**




**Quality Factor**

- MUST characterize devices at operating temperatures
- Device models must predict temperature effects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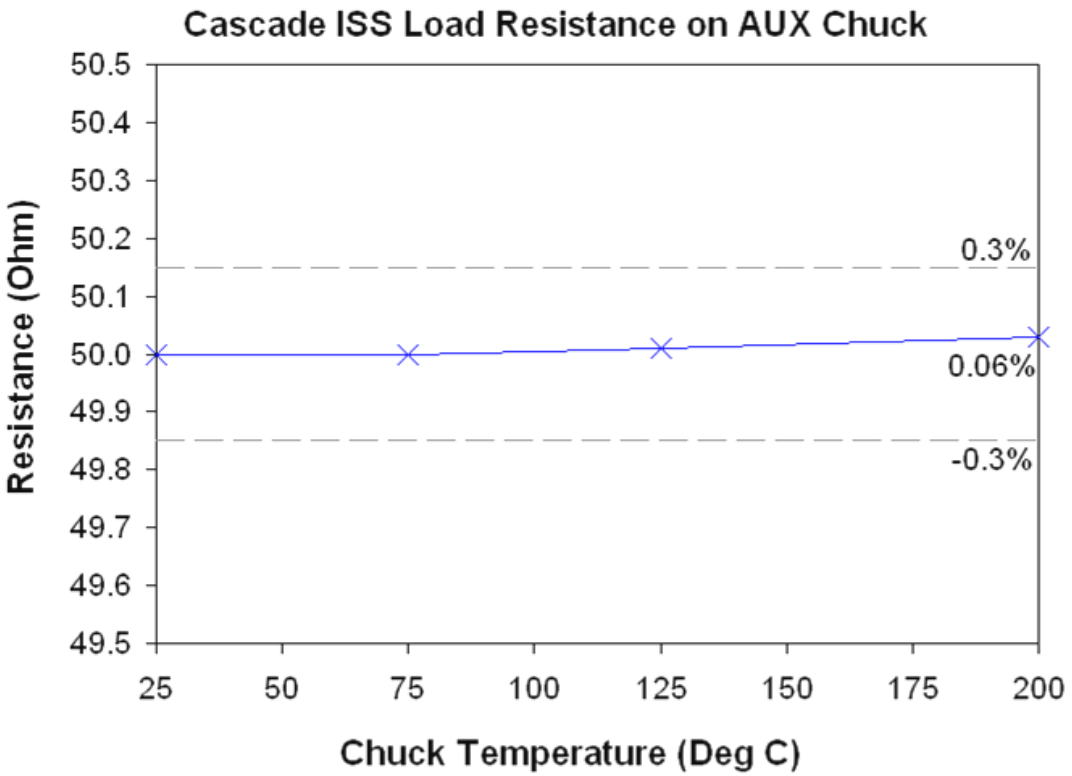
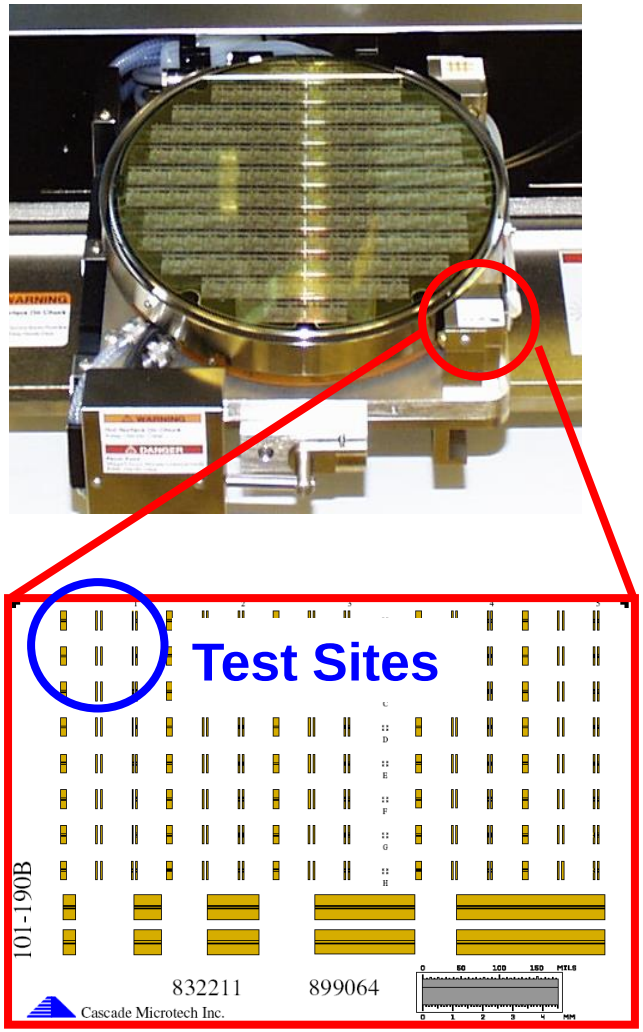
# Over-temperature RF Probe Calibration

1. Load std = 50 Ohms at all temperatures (Standards must be thermally Isolated)
2. RF probes in thermal equilibrium as devices during cal & measurement.





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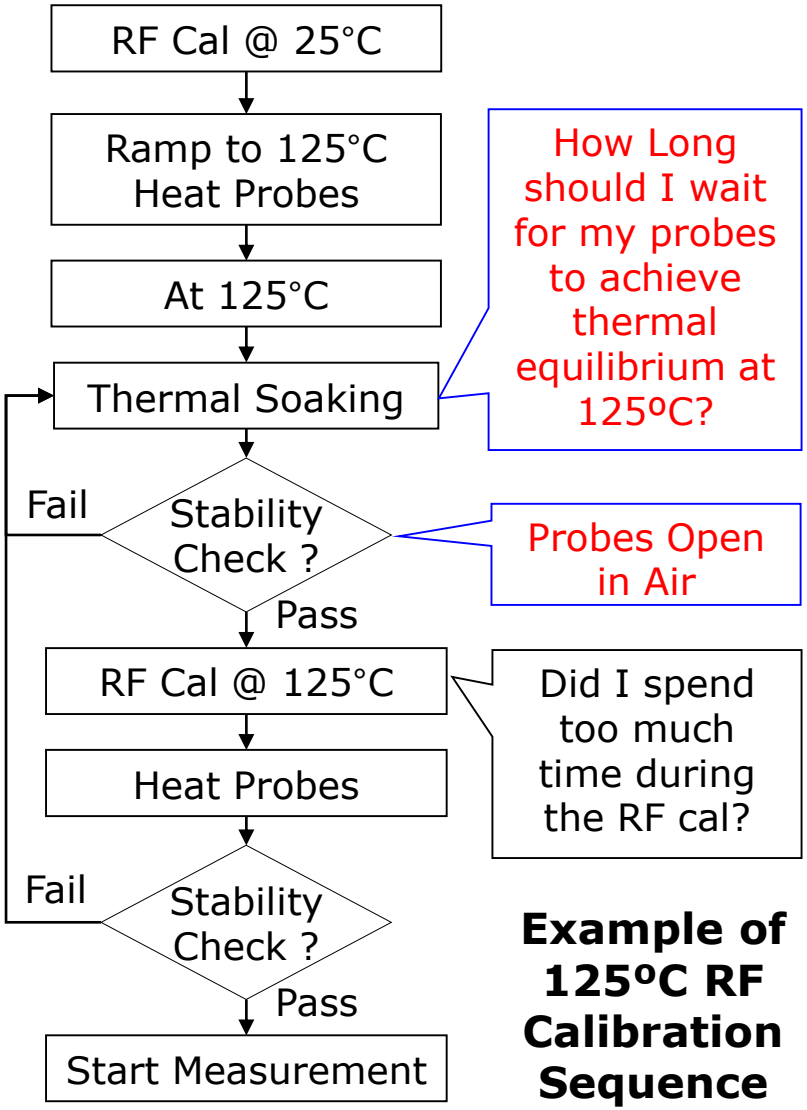
# Recommended Flow for Over-temperature Cal

- How to check if probe in thermal equilibrium with DUT?
- Perform Stability Check
  - Lift Probes up in Air (OPEN)
  - Measure and Monitor S11 & S22
  - OPEN allow probe thermal stability checks anywhere.




**Example of 125ºC RF Calibration Sequence**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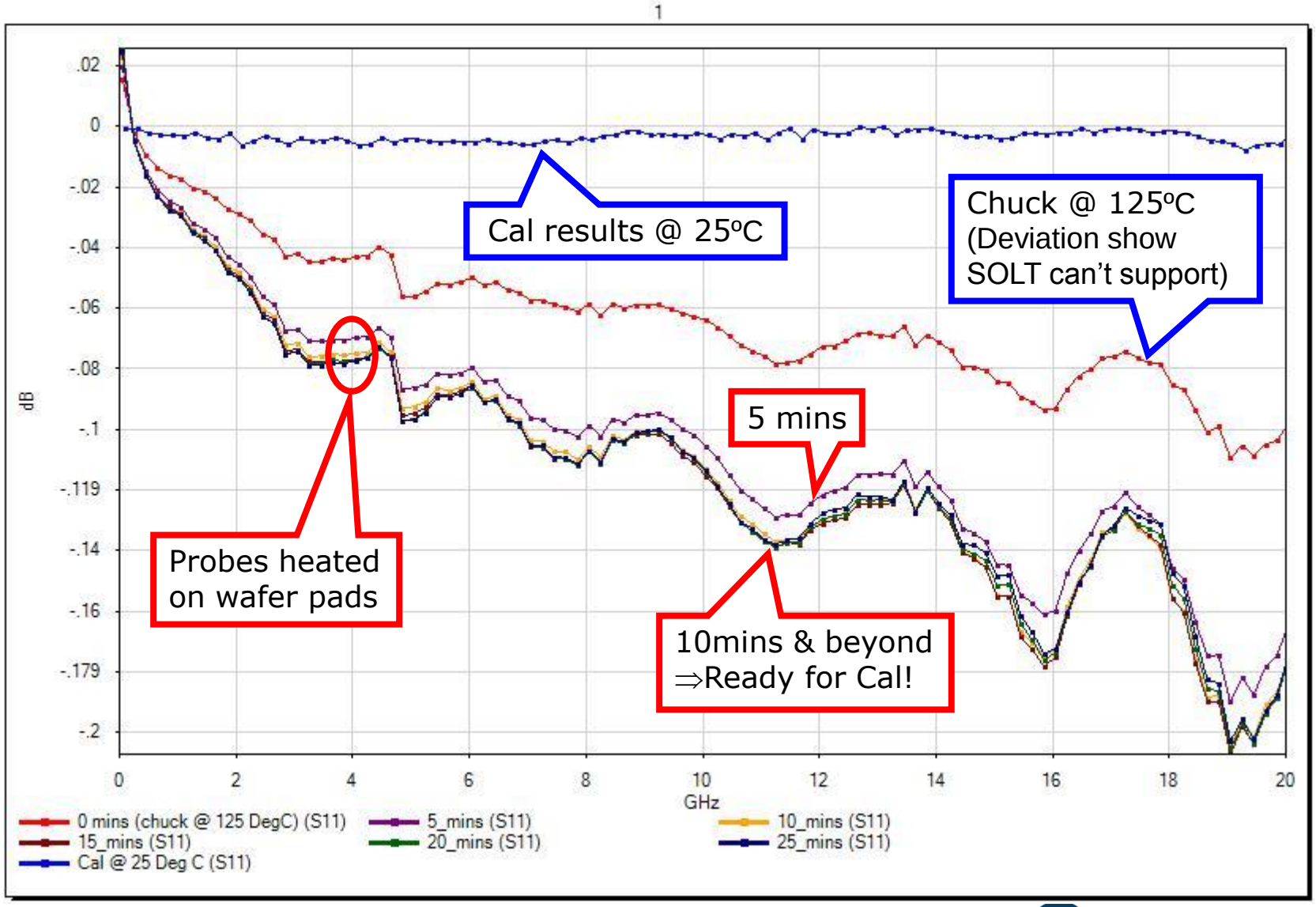
# Deviation in Probe S11 OPEN (in Air)





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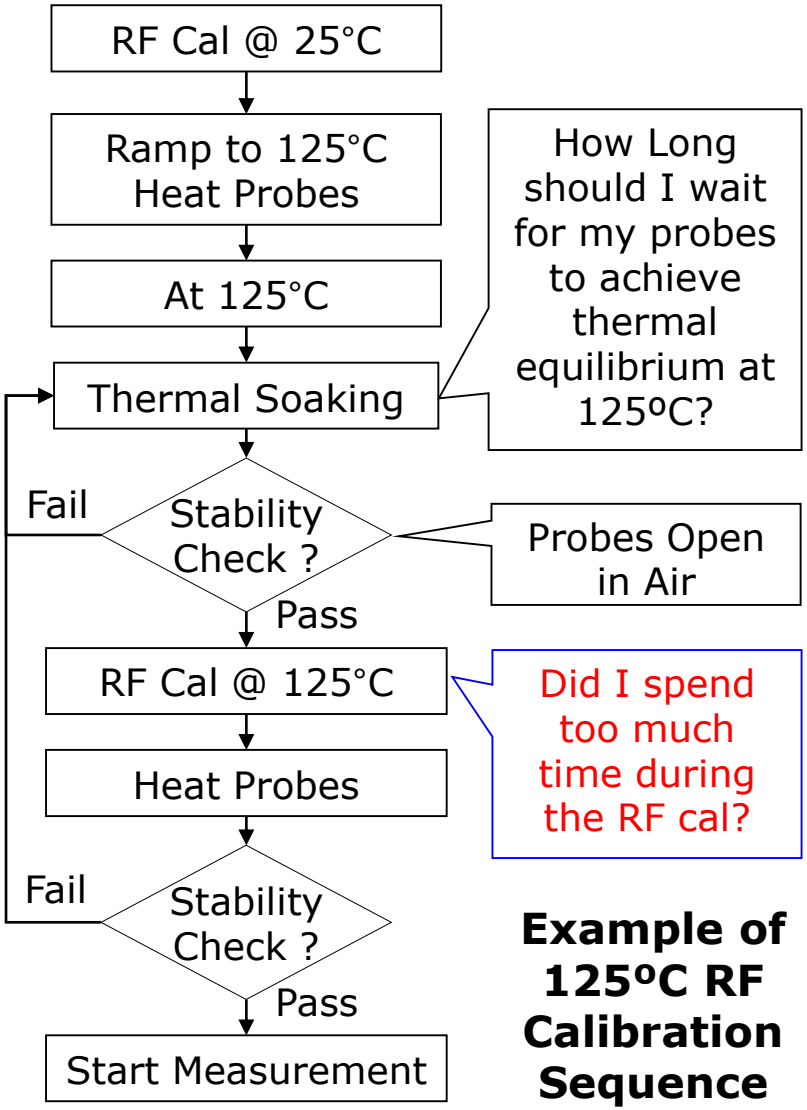


**Example of 125ºC RF Calibration Sequence**


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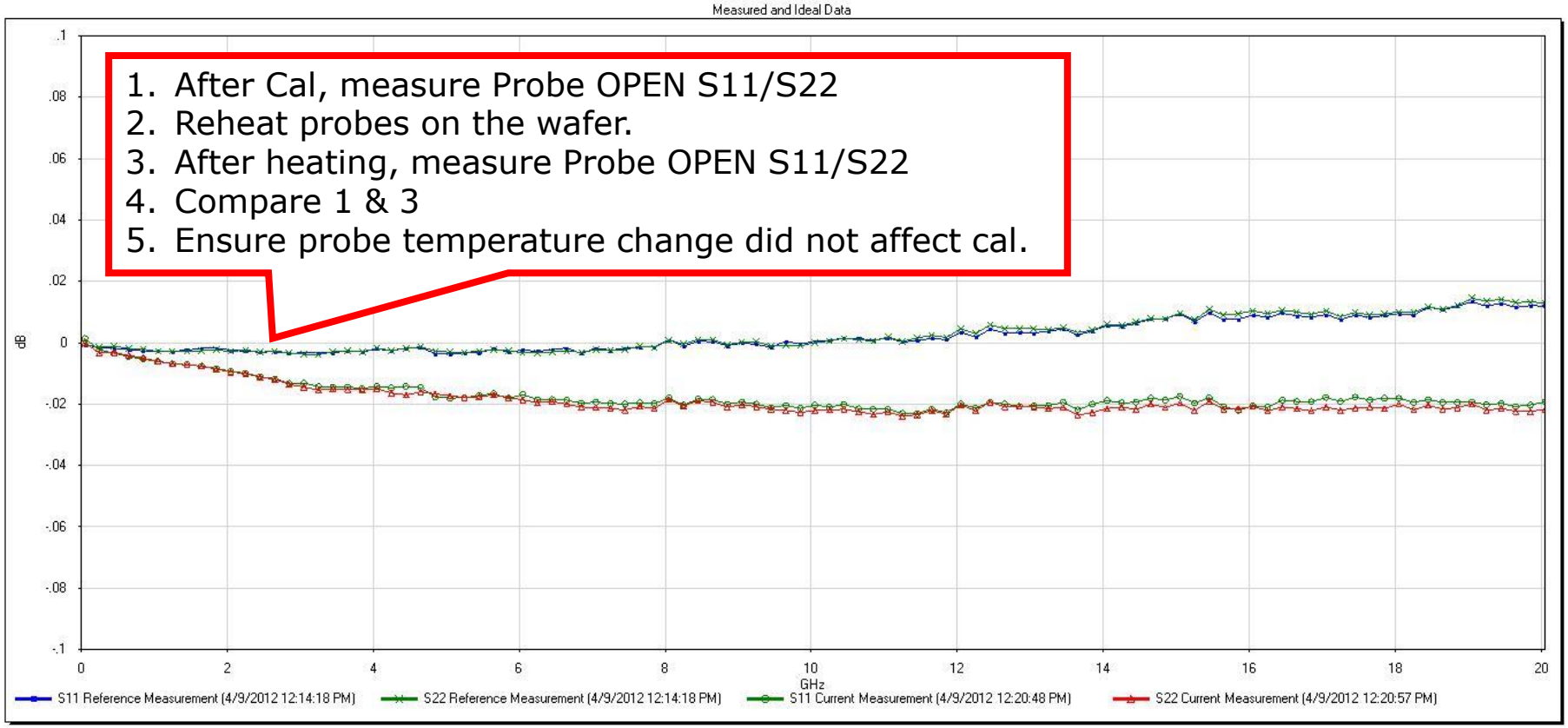
# Checking Probe Thermal Stability after Cal





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# 110 GHz 4 port Calibration using GSGSG probes


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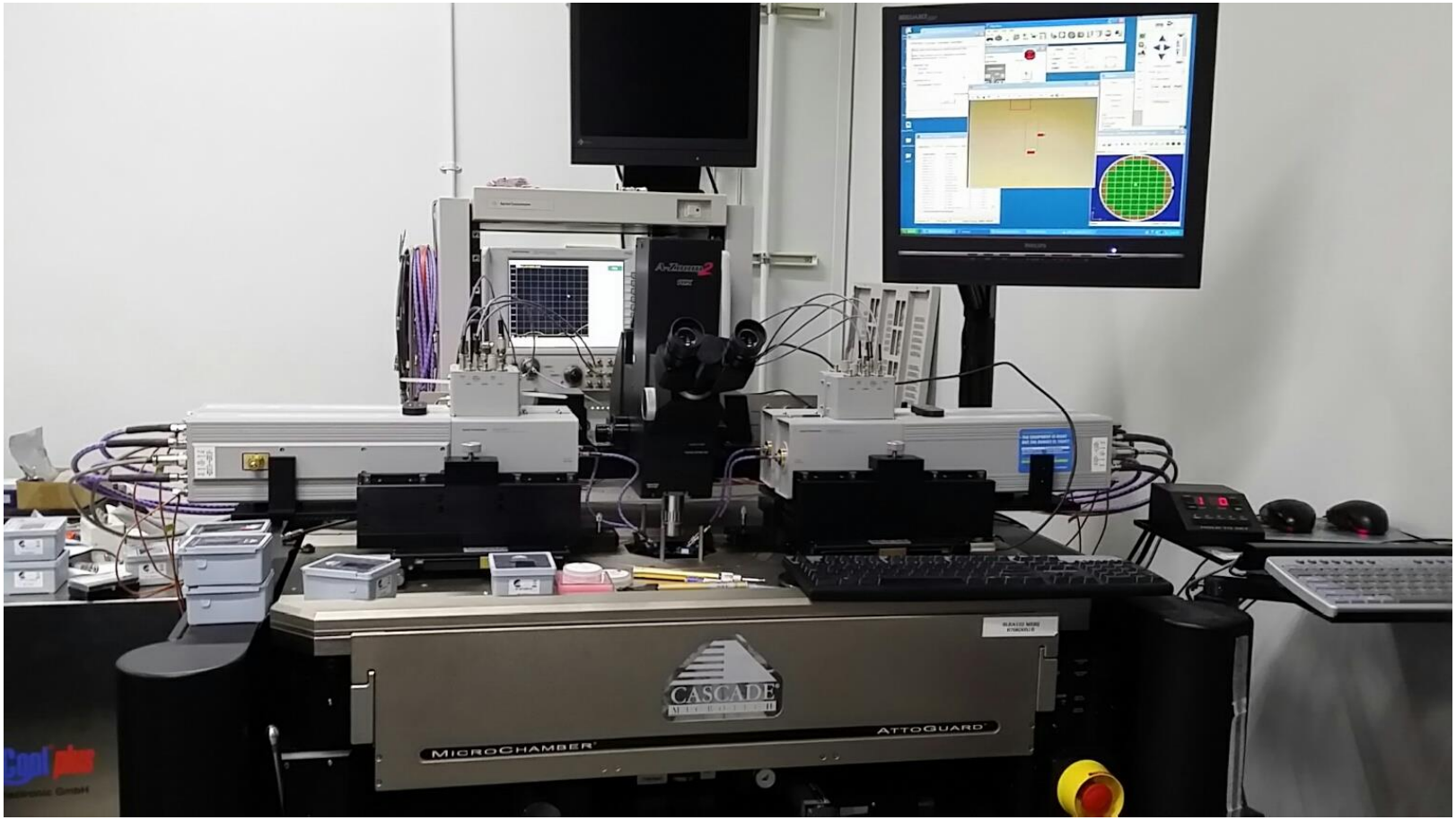
# Cascade & Keysight 4 port 110 GHz Setup





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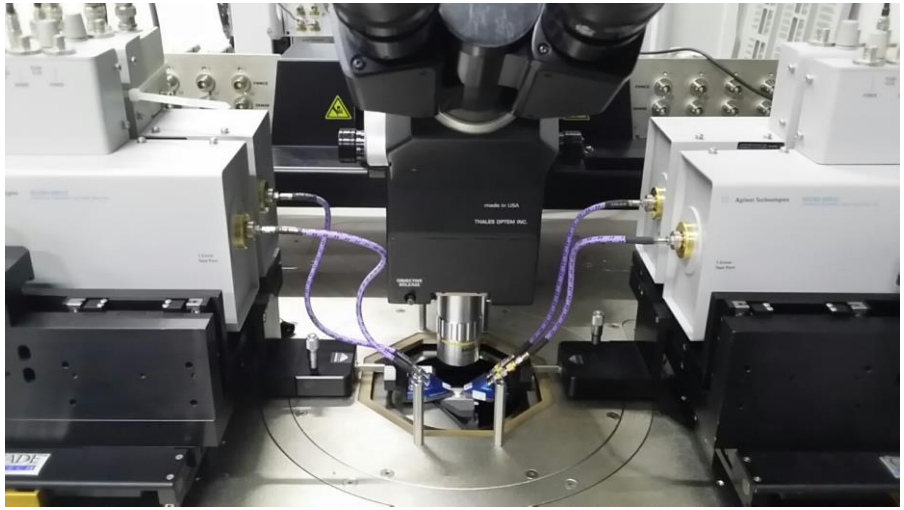
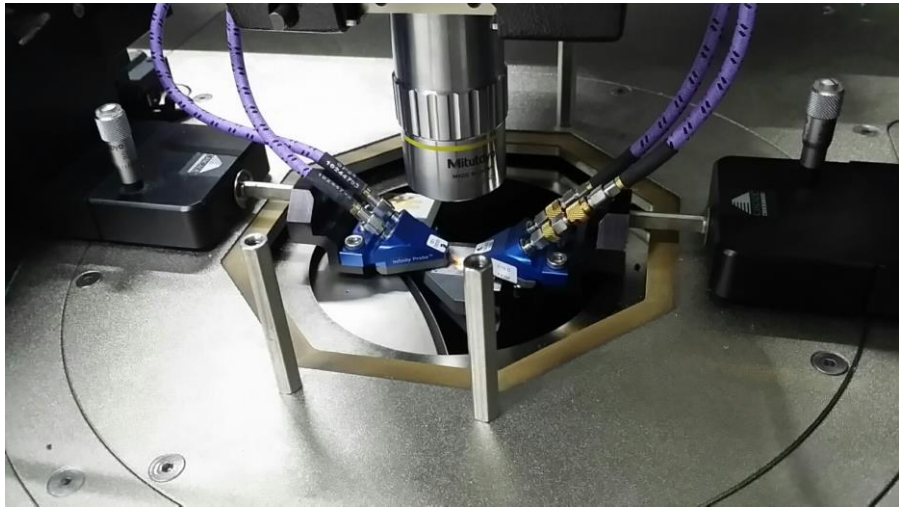
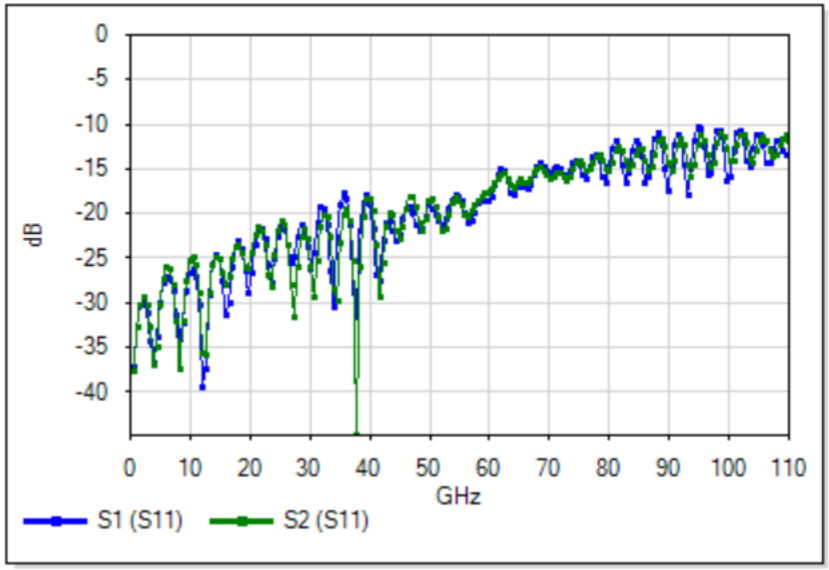
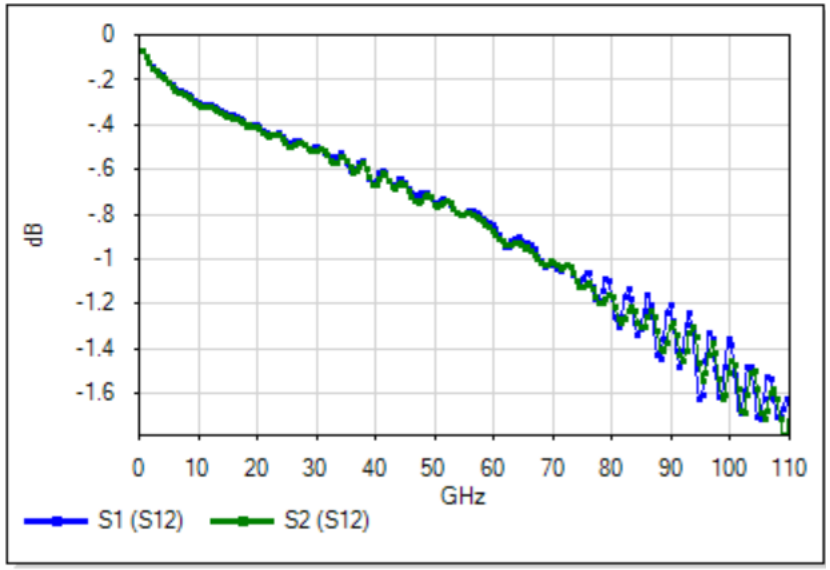
# Cascade & Keysight 4 port 110 GHz Setup









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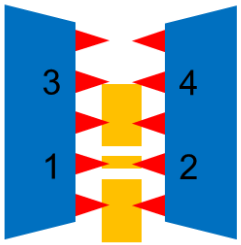
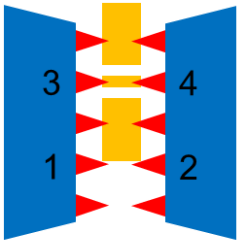
# Unknown Thru' Calibration

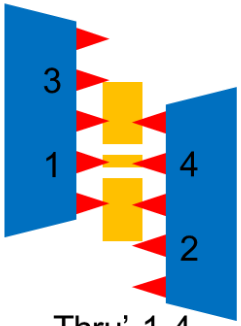
- Adopt unknown thru' calibration or SOLR calibration.
- SHORT-OPEN-LOAD for each ports on ISS (104-783).
- For the Thru' standard, adjust the probes to complete 4 thru' standards.



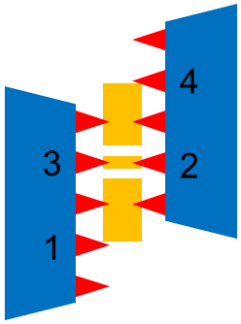

Thru' 1-2



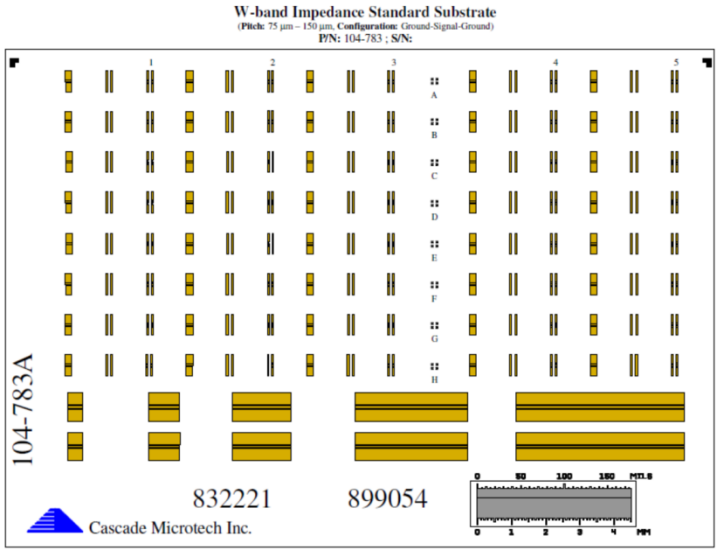

Thru' 3-4

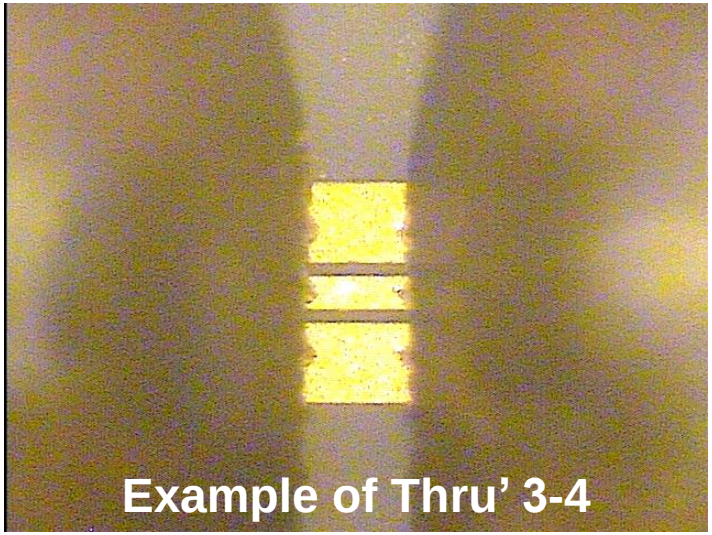



Thru' 1-4




Thru' 3-2





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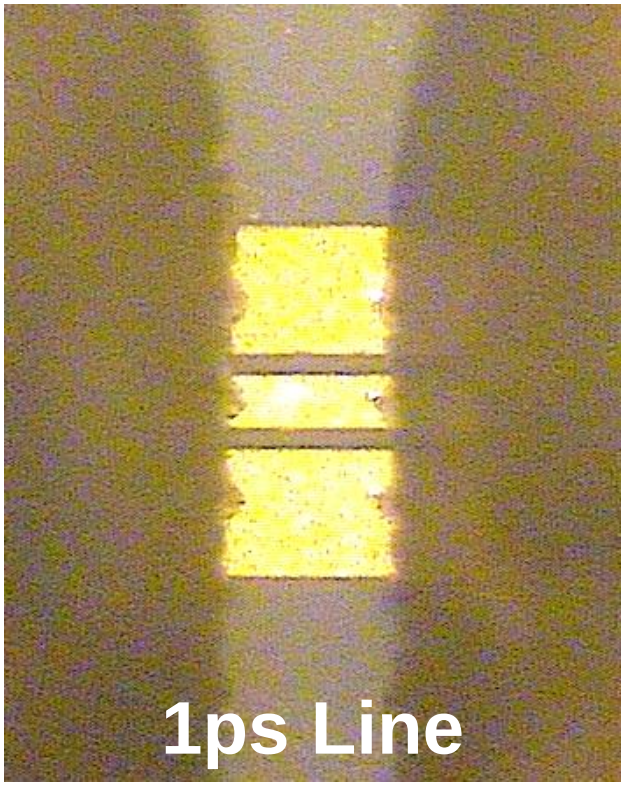
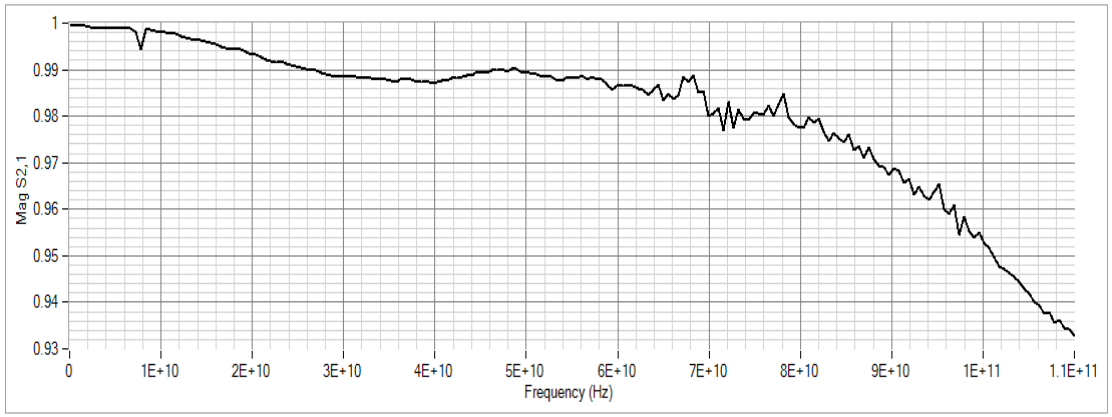
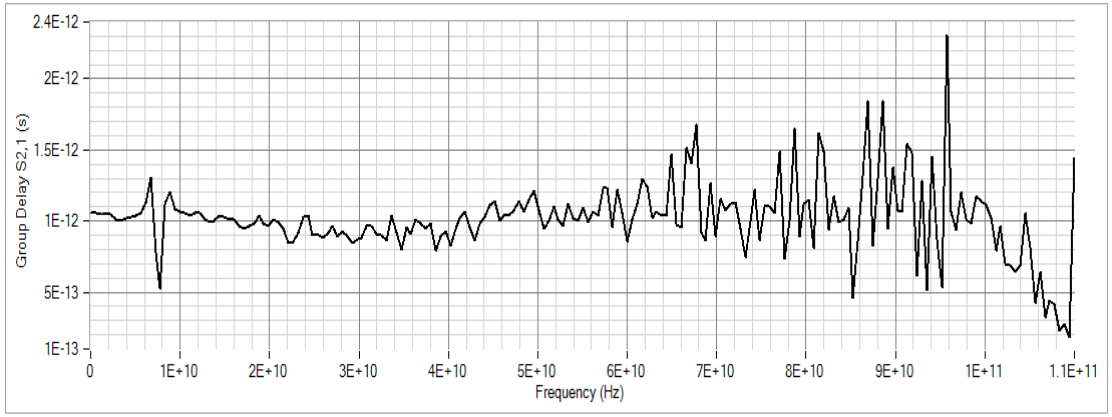
# Port 3-4 Calibration Verification




**Delay valid up to 100GHz**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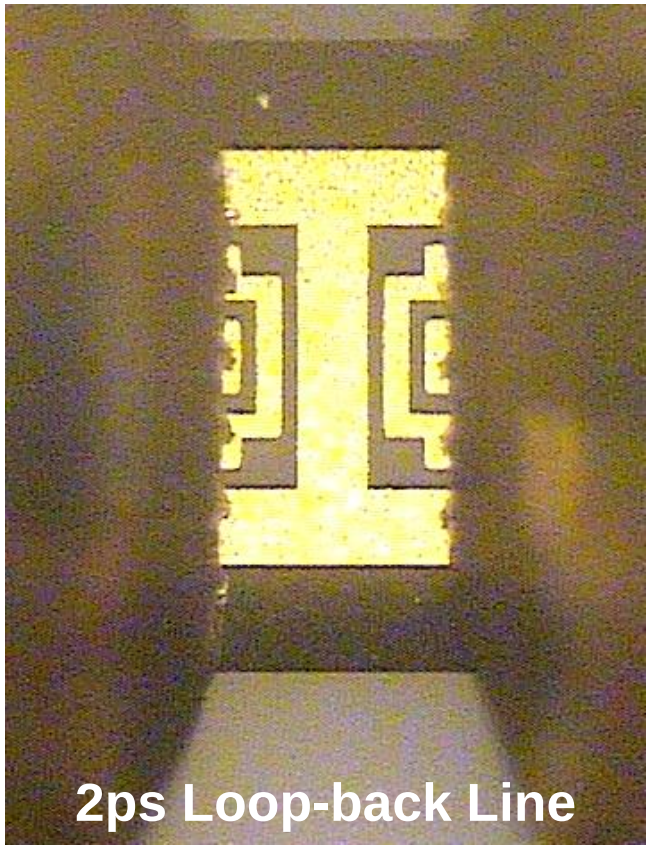
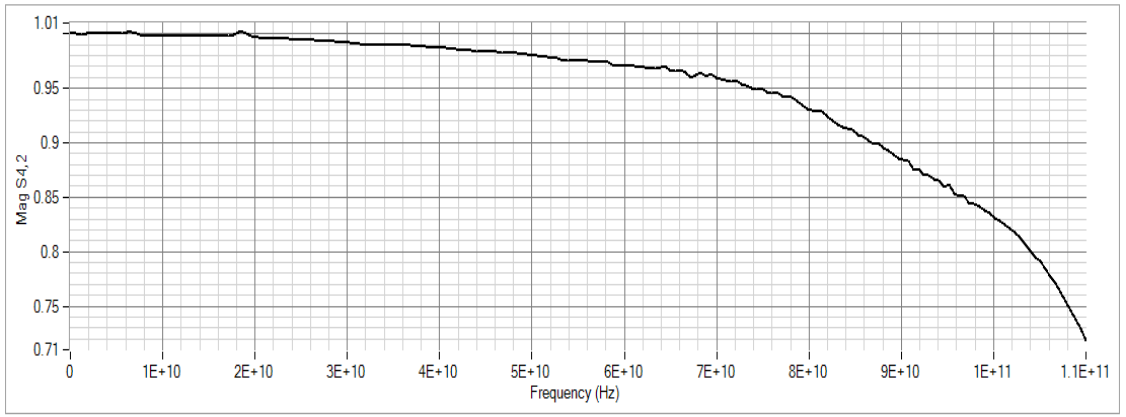
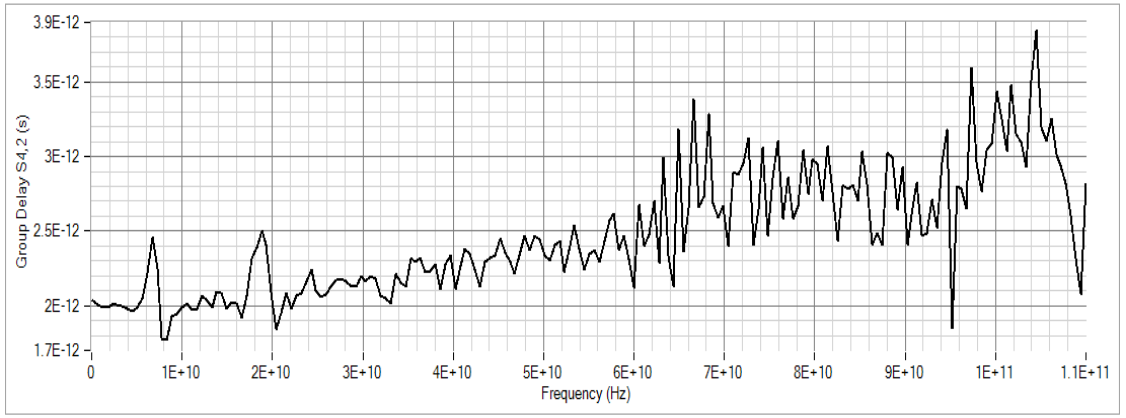
# Port 1-3 Calibration Verification




**Increase in Delay due to increase in inductance**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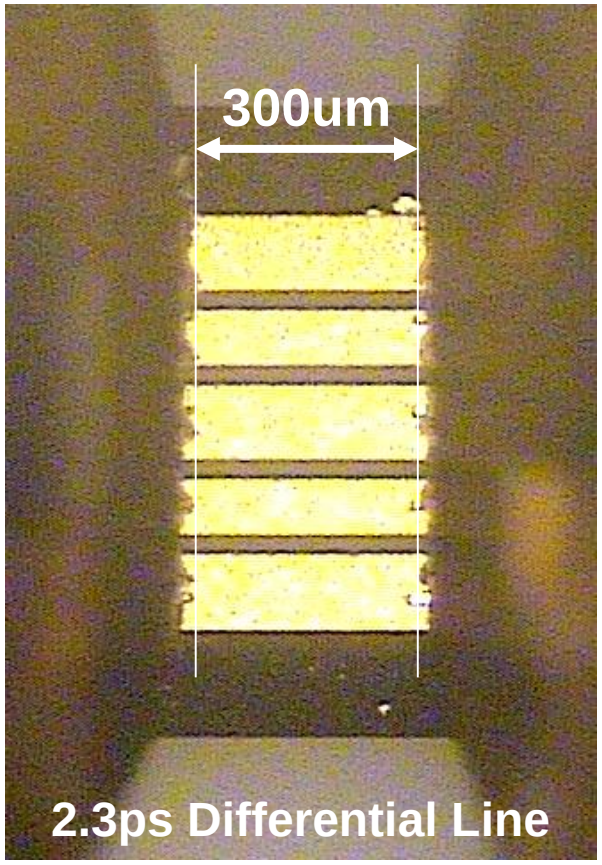
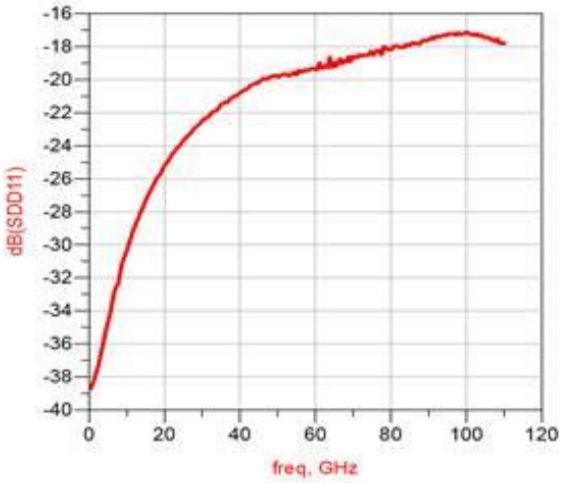
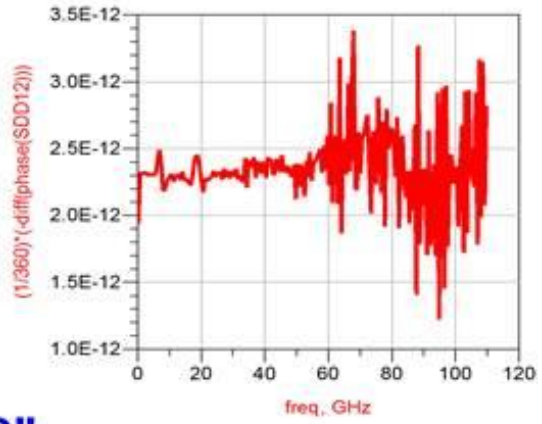
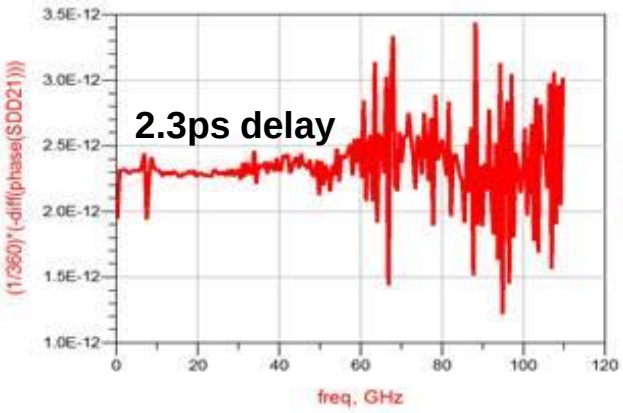
# Differential Line

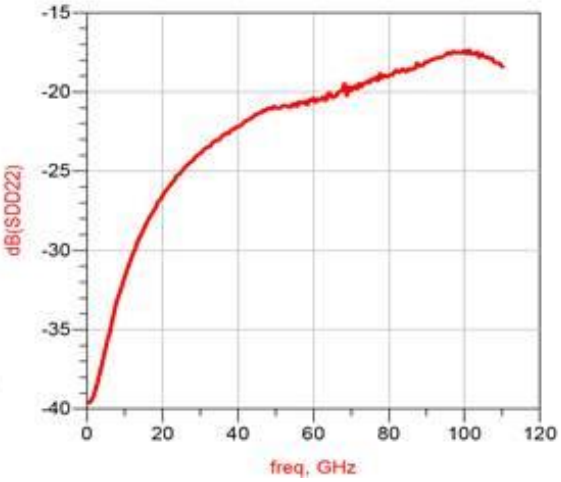



"DD"





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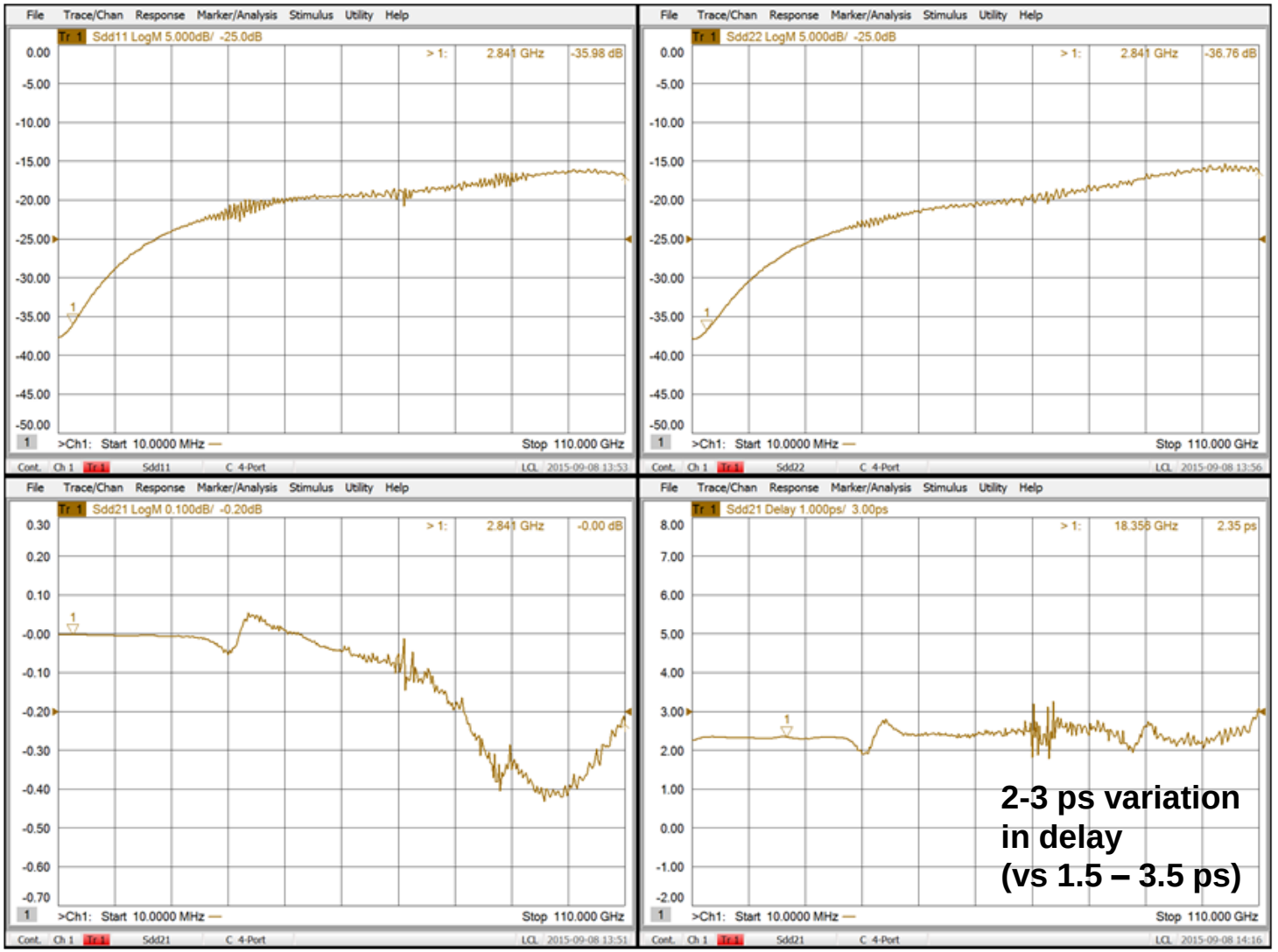
# Differential Line (WincalXE, 4 Port SOLR cal)





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# Sub-THz Wafer Level VNA Calibration


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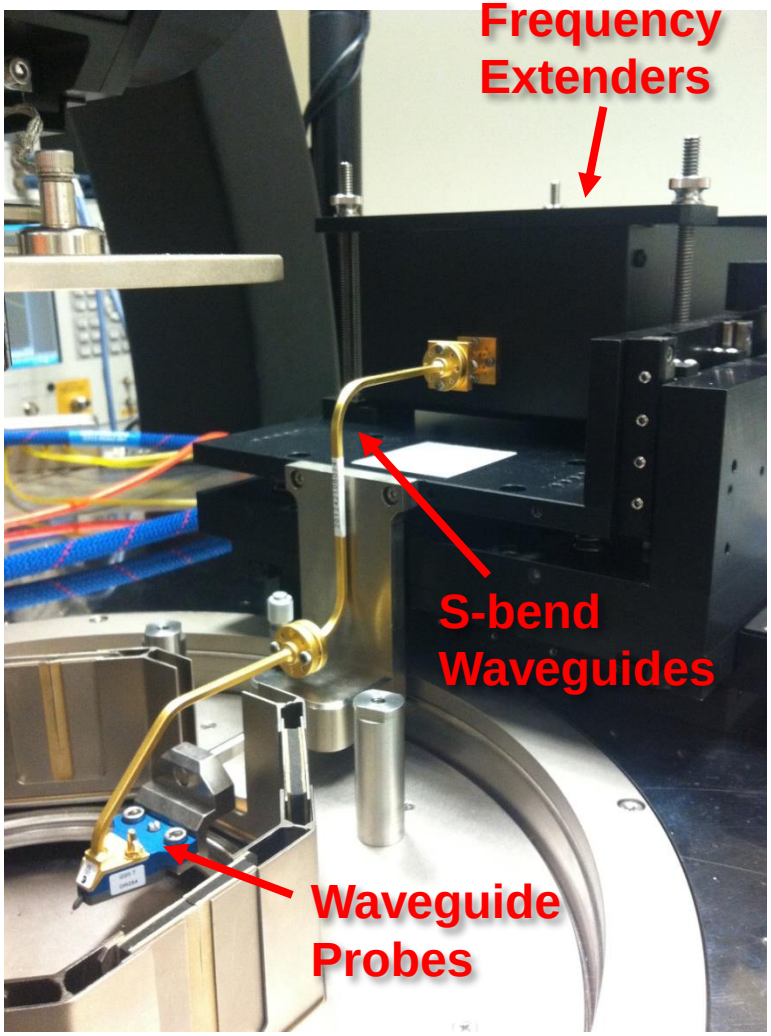
# Challenges for Sub-THz Banded measurements

- Banded Calibration :- 50-75GHz, 90-140GHz, 110-170GHz, 140-220GHz, 220-325GHz and 325-500GHz.
- mmW tests on same device
  - Design TRL standards.
  - Setup Freq extenders, S-bends and waveguide probes for every frequency bands.
  - Perform calibration & measure device for every band - Tedious and time consuming.
- How to ensure calibration continuity and device measurement integrity for all frequency bands?





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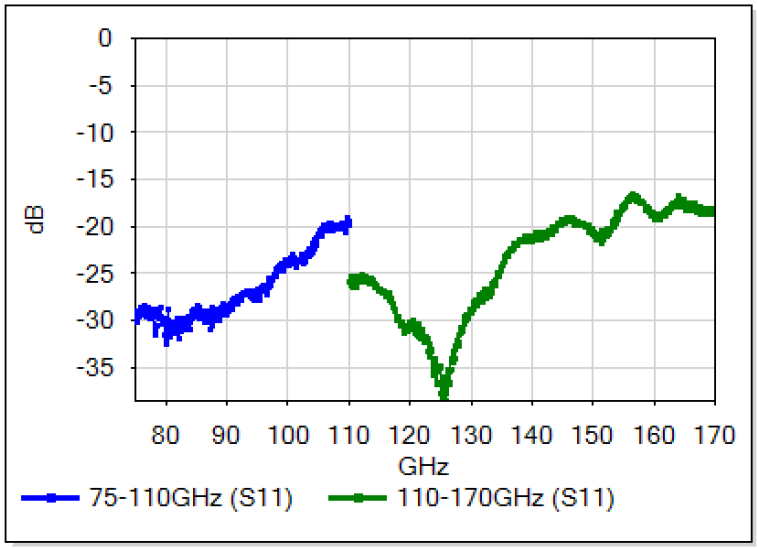
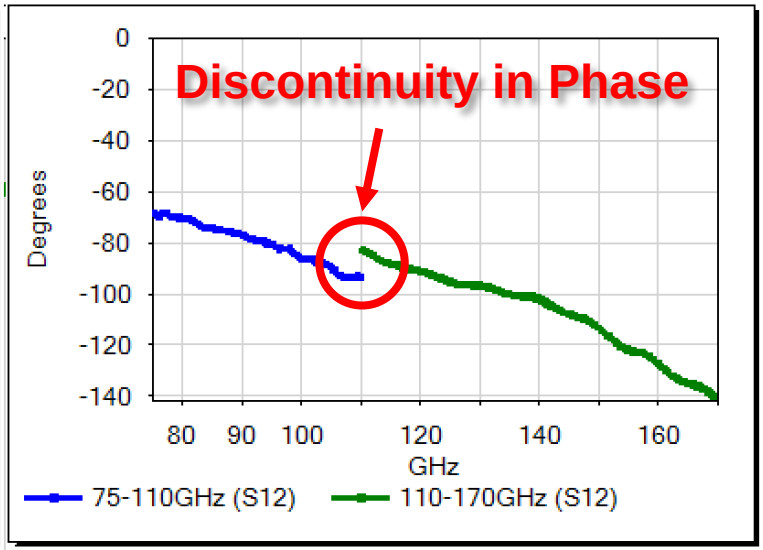
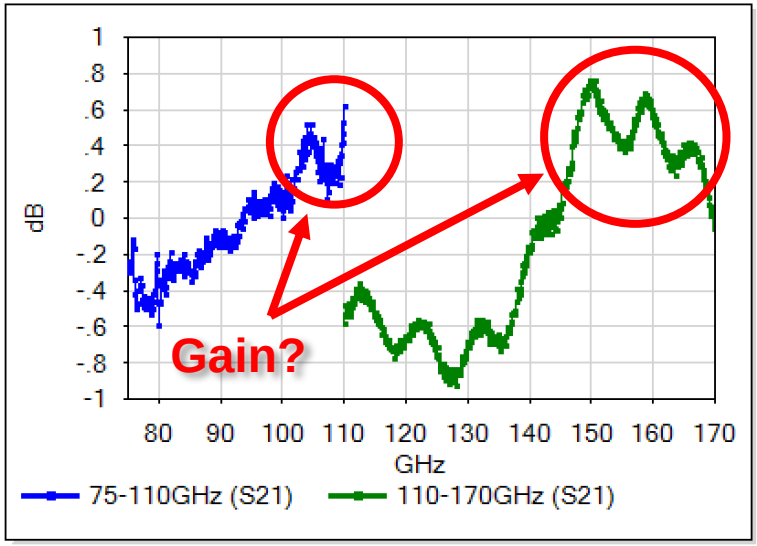
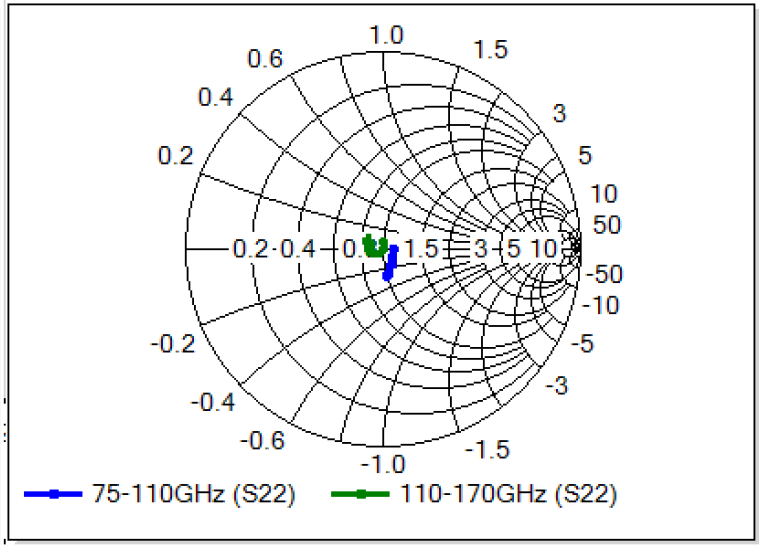
# Example of Data Discontinuity (160um Line)





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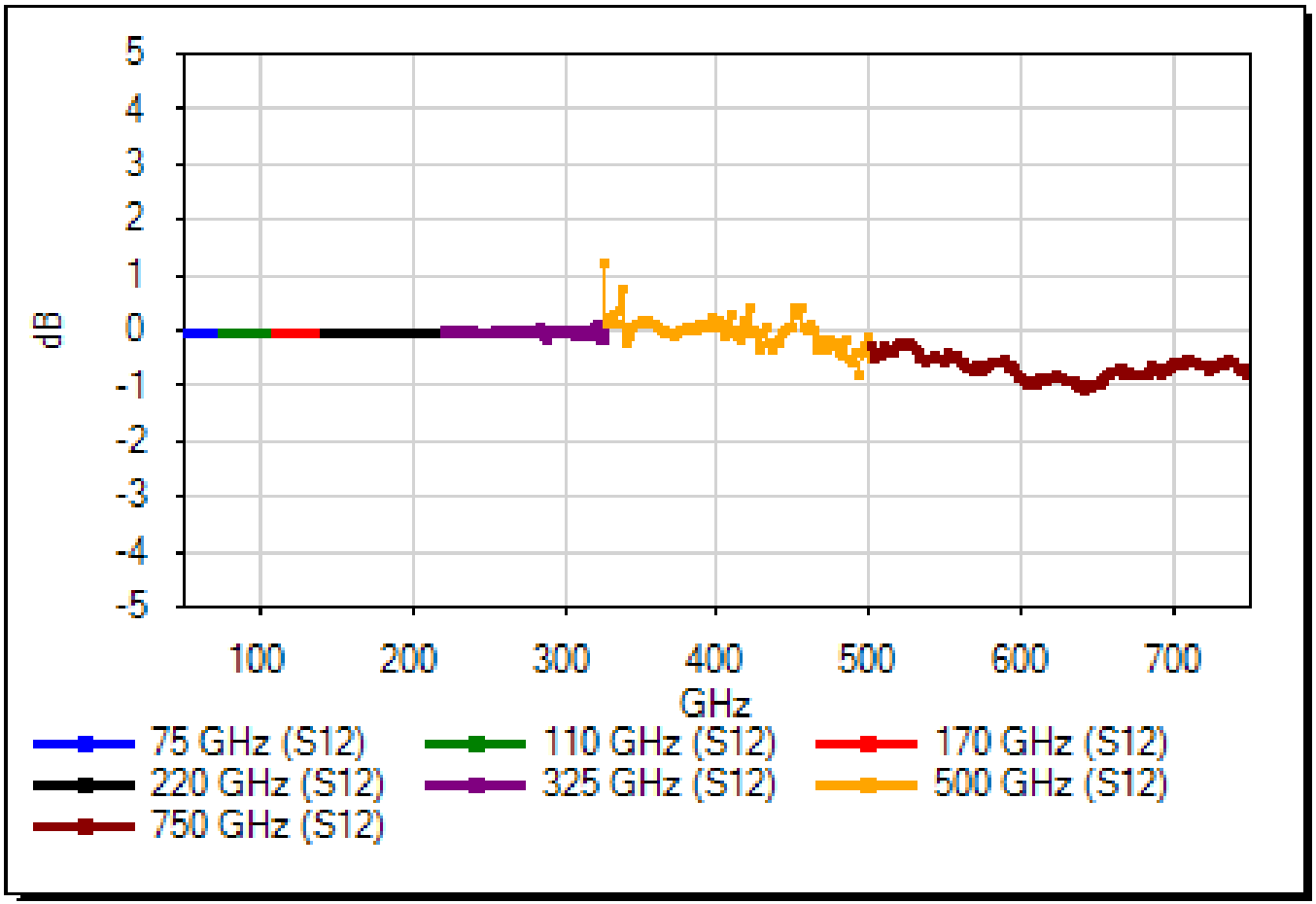
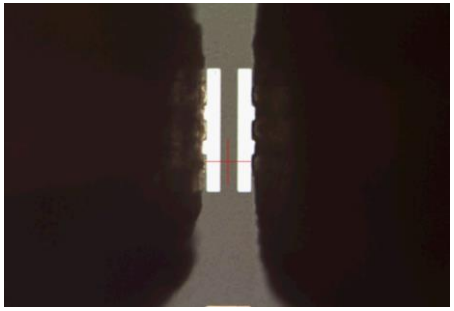
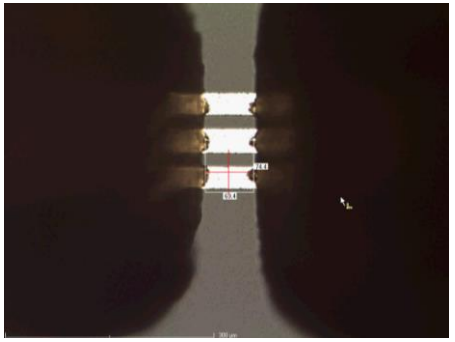
# How to Verify Calibration Continuity?




**Magnitude S21 on 0.5ps Line**



**Aligning Probes**



**0.5ps Line**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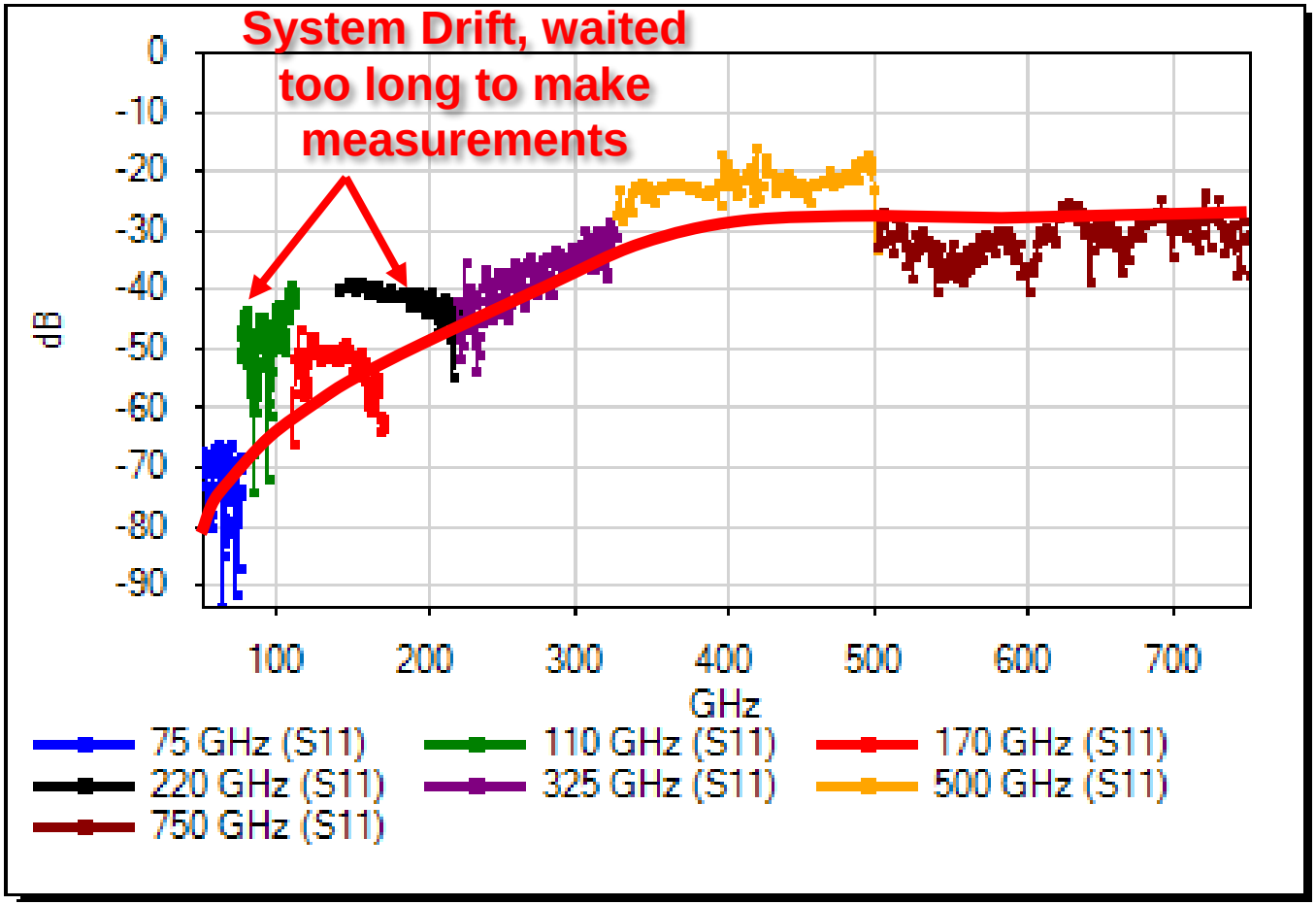
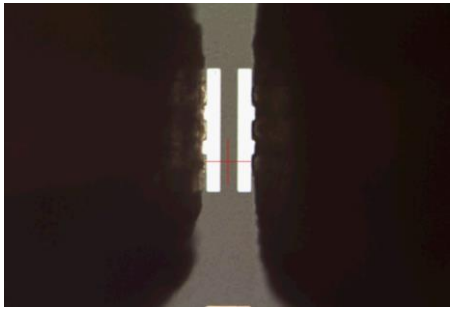
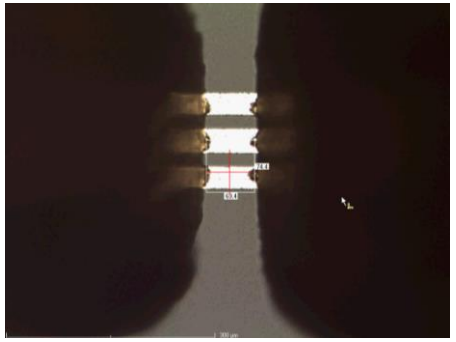
# How to Verify Calibration Continuity?




Return Loss on 0.5ps Line



Aligning Probes



0.5ps Line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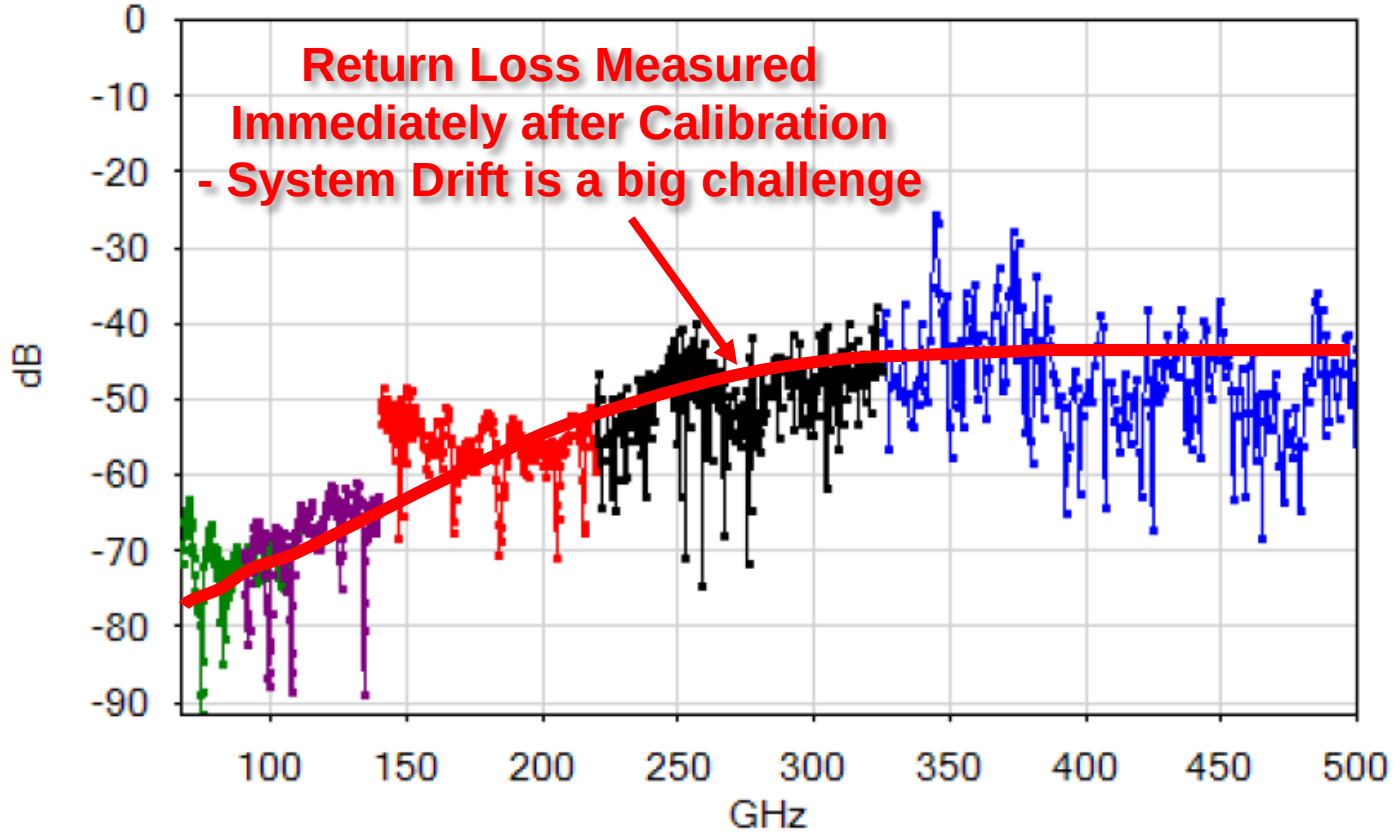
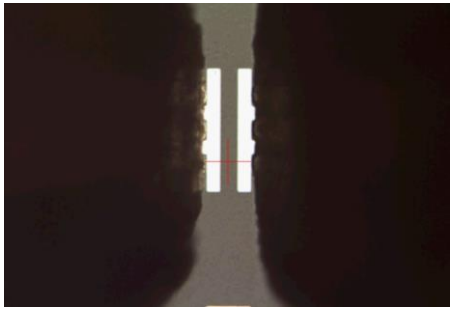
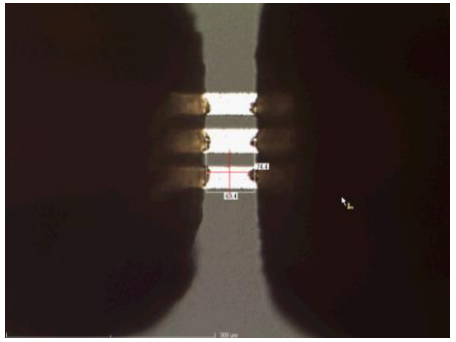
# How to Verify Calibration Continuity?



Aligning Probes



0.5ps Line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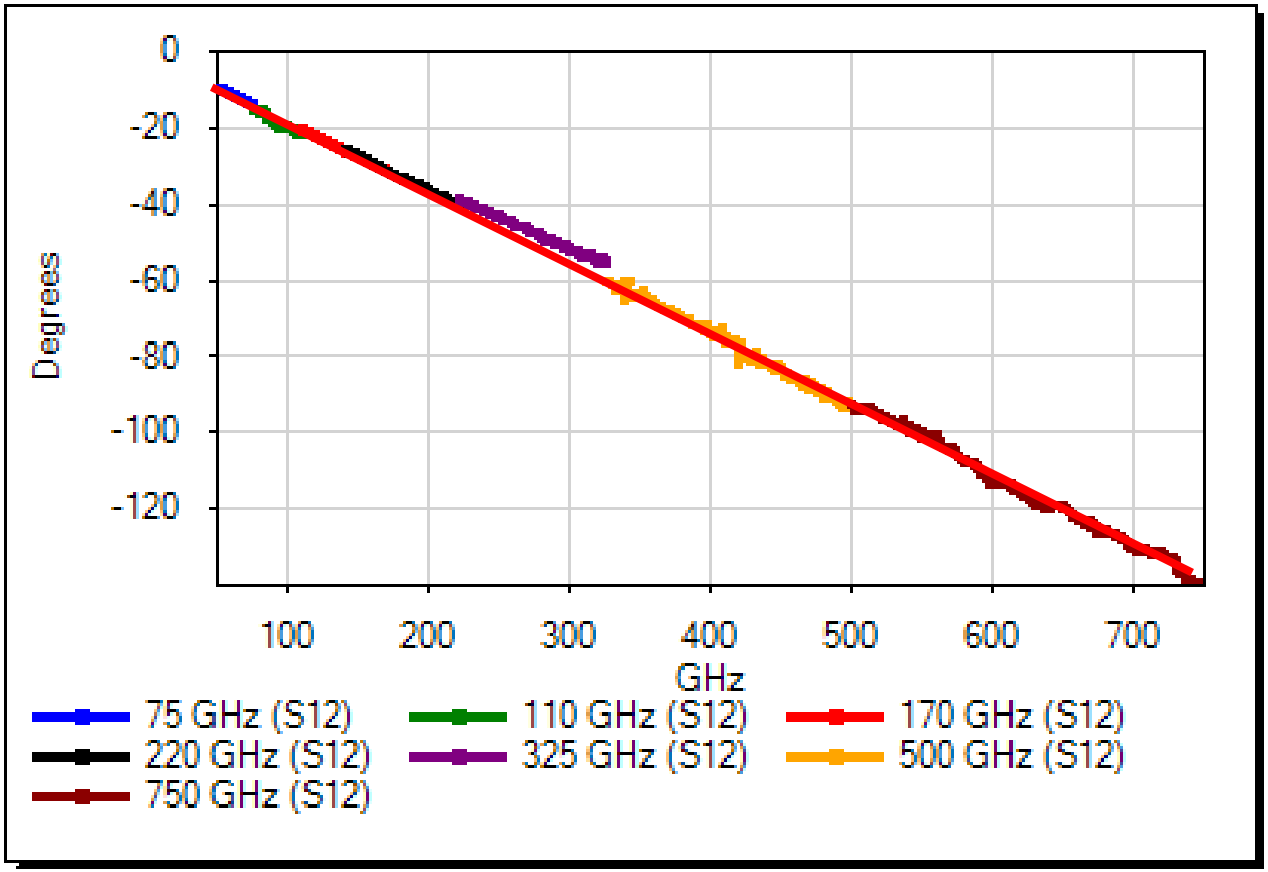
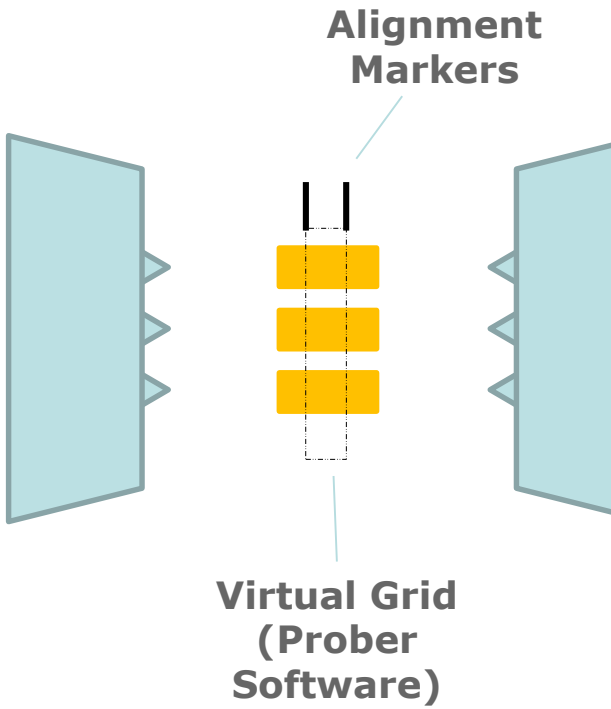
# Verifying Calibration Continuity

- Design verification line with alignment markers on wafer.
- Characterize same line for all bands after TRL cal (or LRRM cal).
- Plot all bands, Phase S12 or S21 (group delay can be used too)
- Use plot as reference – ensure Measurement Continuity & Integrity.

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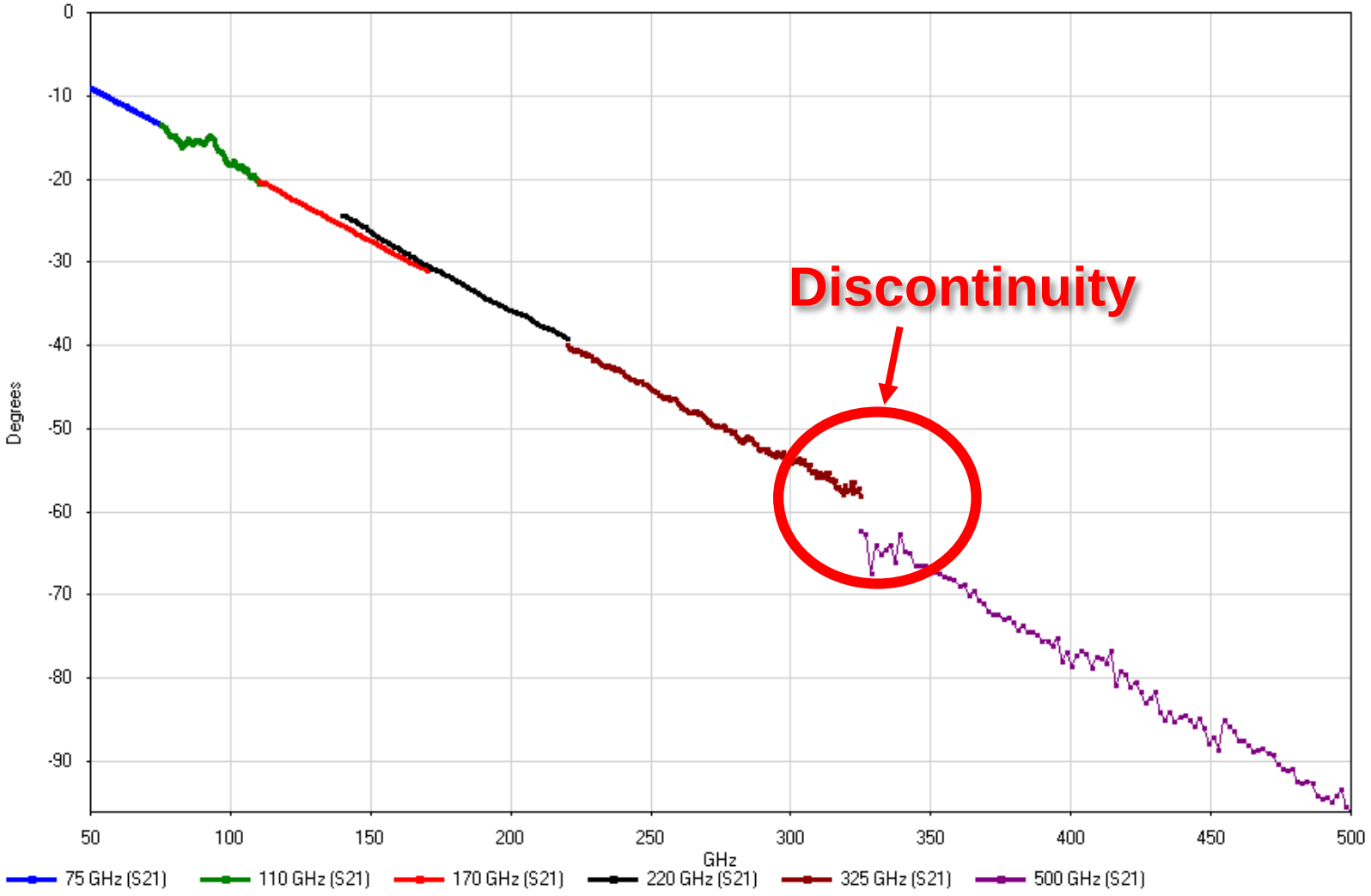
# Example of 325 GHz cal – Discontinuity in Test Data





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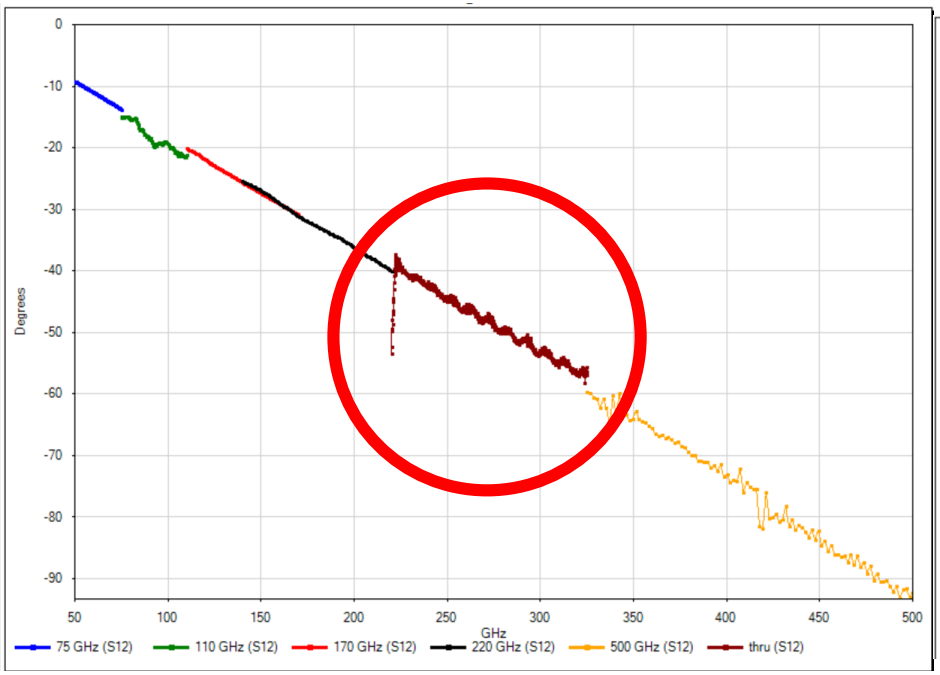
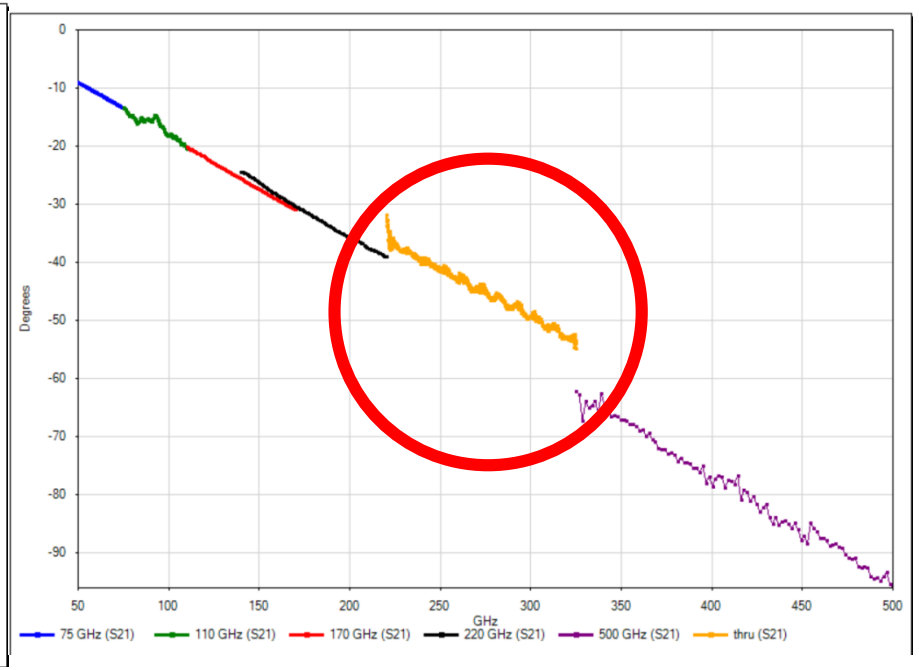
# Example of 325 GHz cal – Discontinuity in Test Data





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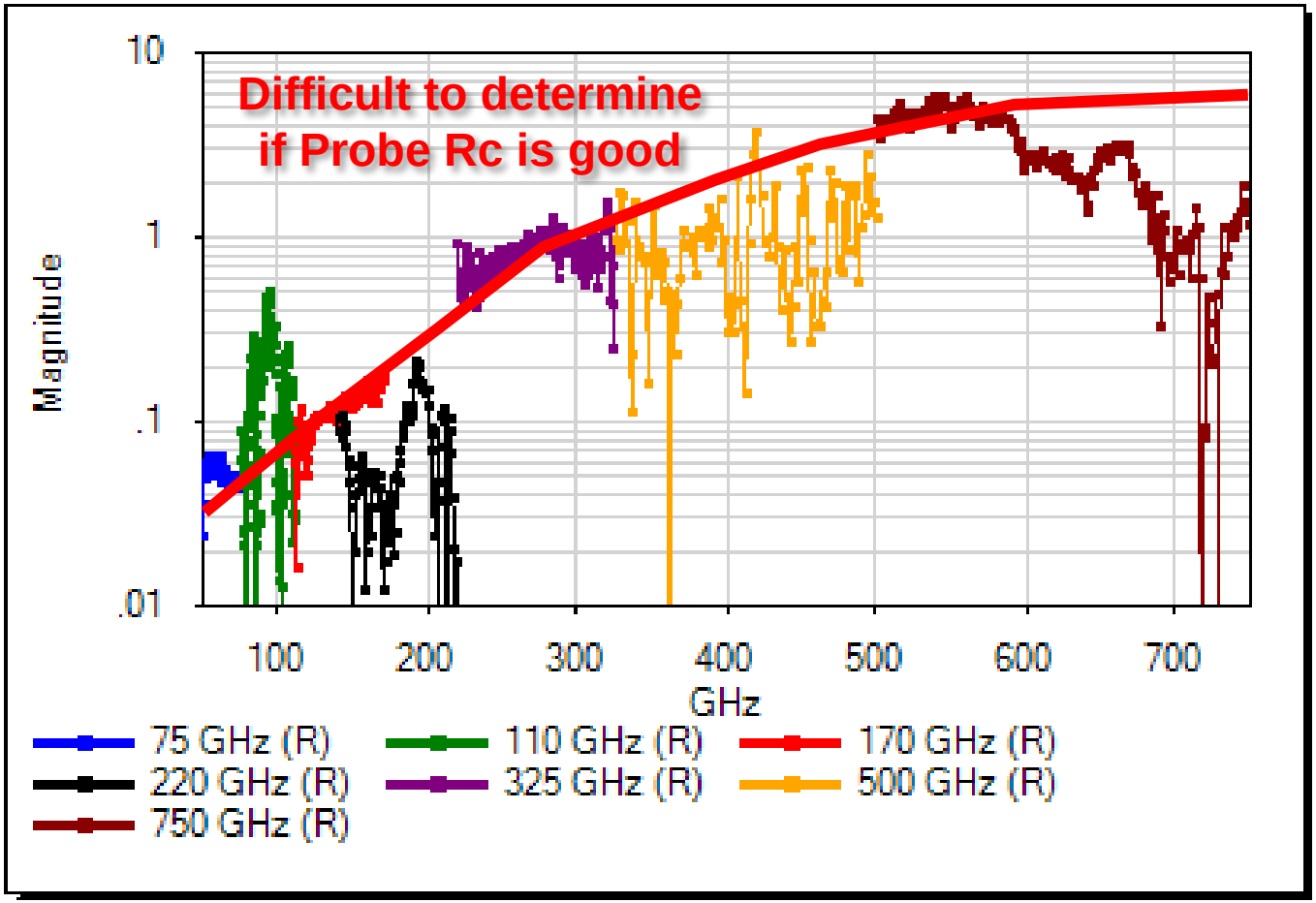
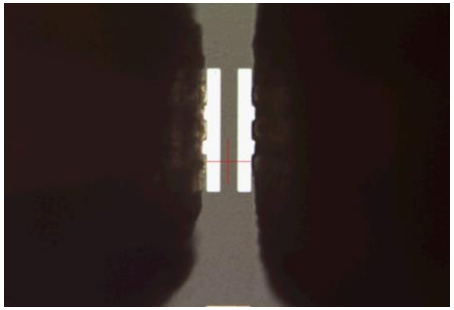
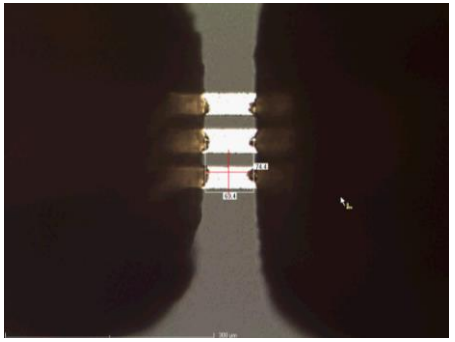
# Ensure Continuity in Contact Resistance?




Extracted 2*Probe Rc + Line Resistance



Aligning Probes



0.5ps Line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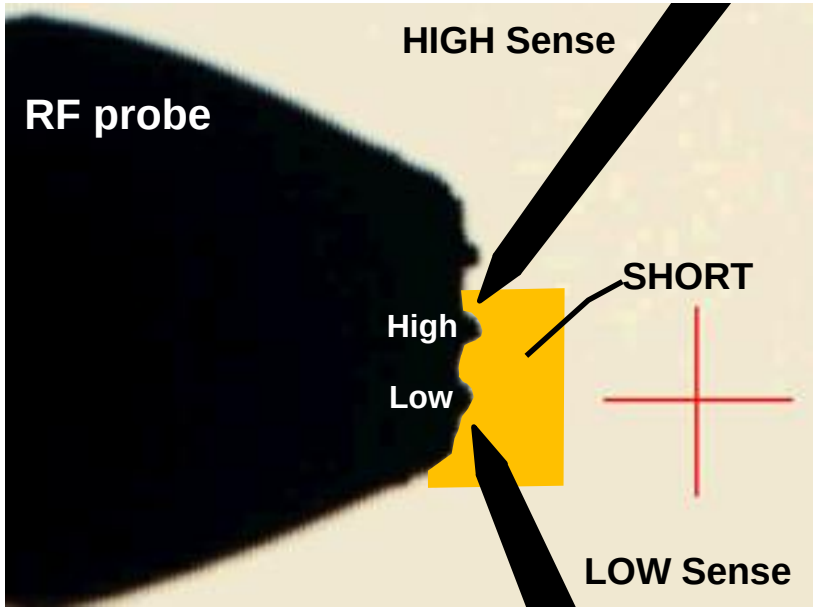
# Ensure Continuity in Contact Resistance?

- Check DC contact resistance for each set of waveguide probes (20-50 milliohm range)
  - Contacting probes Short Structure Design on Wafer
  - Additional DC probes (for True Kelvin measurement) to measure Rc of the waveguide probes.





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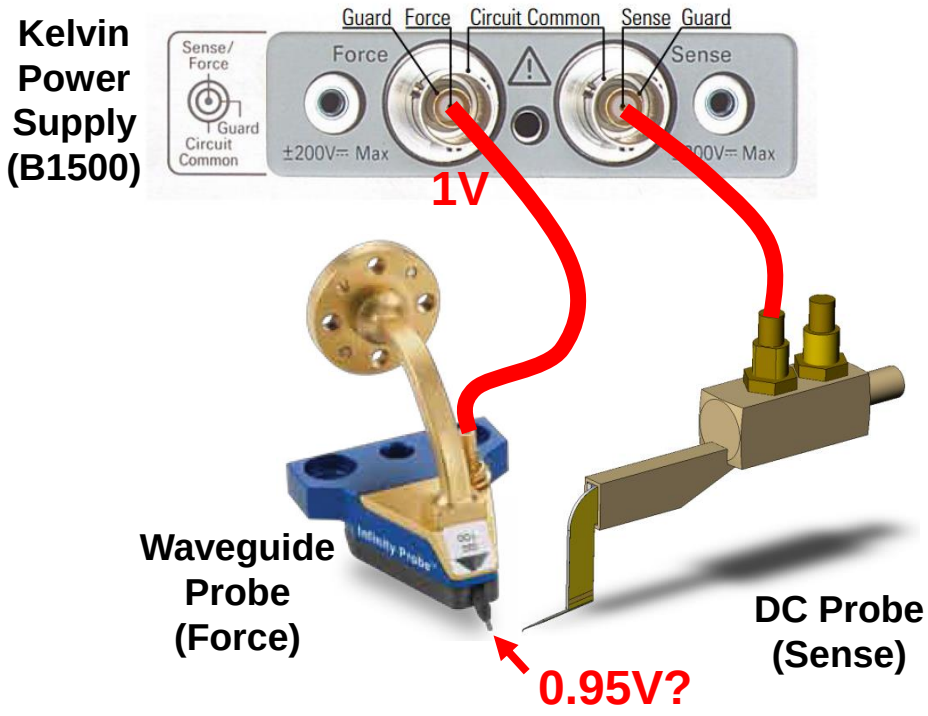
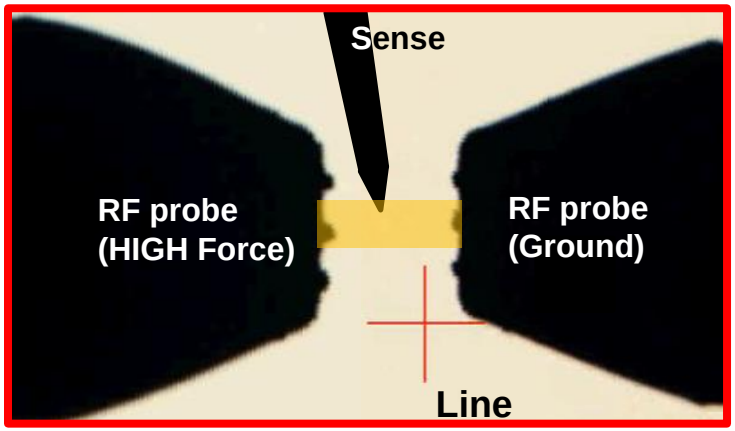
# Ensure Continuity in Biasing Voltage

- Ensure same Voltage is applied to Device terminals.
  - Correct Series Resistance from Cabling, Probe Bias Tee Network, Probe tips contact for every frequency band setup.
  - Use Voltmeter if power supply has no sense capability



# Summary

- Choose the calibration method which,
  - Requires minimal info of the calibration standards
  - Insensitive to Probe Placement
- Always verify with known devices after calibration.
- Over-temperature Calibration
  - Ensure standards are thermally isolated
  - Ensure probes are in thermal equilibrium as Device/Wafer
- Unknown Thru' or SOLR calibration to support 110 GHz 4 port calibration.
- For Banded Calibration,
  - Check Probe $R_{DC}$, Design & use alignment markers to ensure consistent probe placement
  - Ensure data integrity and continuity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# Thank You

Questions – Email to Choonbeng.sia@cmicro.com