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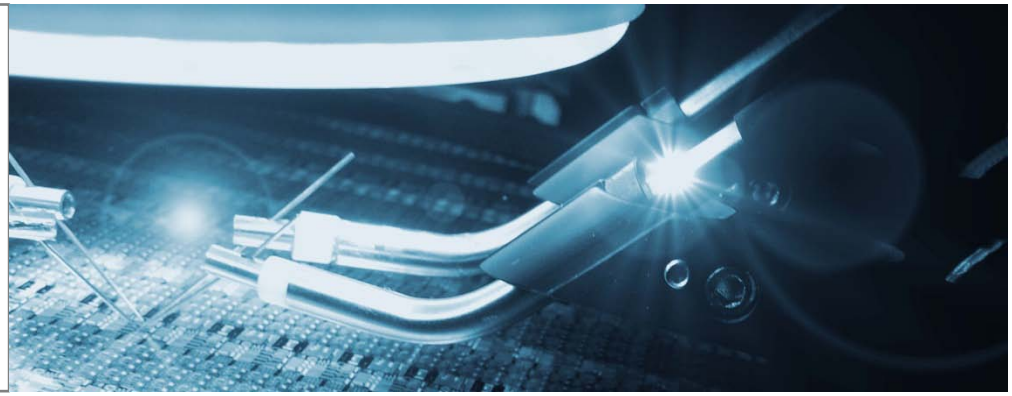
# Understanding RF CMOS Compact Modeling to Allow Accurate RF & mm wave Circuit Design



# FOREWORDS

- This talk will be aimed at practical aspects impacting RF characterization and modeling
- No complex theory, but pragmatic hints and tricks acquired by experience and usually not discussed in scientific papers
- Present common mistakes and their direct impact on the model (by switching ON/OFF the related effect in a model card) in order to quantify their impact
- When possible present existing solutions to the problem, but keep in mind that in this domain there's not ONE FITS ALL solution, always looking for better solutions and creative thinking is the key

# OUTLINE

- Introduction
- De-embedding basics
- DUT reference plane
- RF Test Structures
- Parasitic series resistances
- Self-heating
- Parasitic substrate network
- Conclusion

# INTRODUCTION

- Evaluating the accuracy of a compact model is a difficult task
- Attempts have been made to rationalize the accuracy evaluation by introducing “quantitative” fit function (or accuracy criterion)
- Examples of accuracy criterion typically used by foundries

| | |
|---|---|
| Vt_lin(mV) | abs(ΔVt_lin)<=10mV |
| Vt_sat(mV) | abs(ΔVt_sat)<=10mV |
| Idlin(%) | abs(ΔIdlin)<=6% |
| Idsat(%) | abs(ΔIdsat)<=6% |
| Idoff(%) | abs(ΔIdoff)<=50% |

RMS & Max error <10%

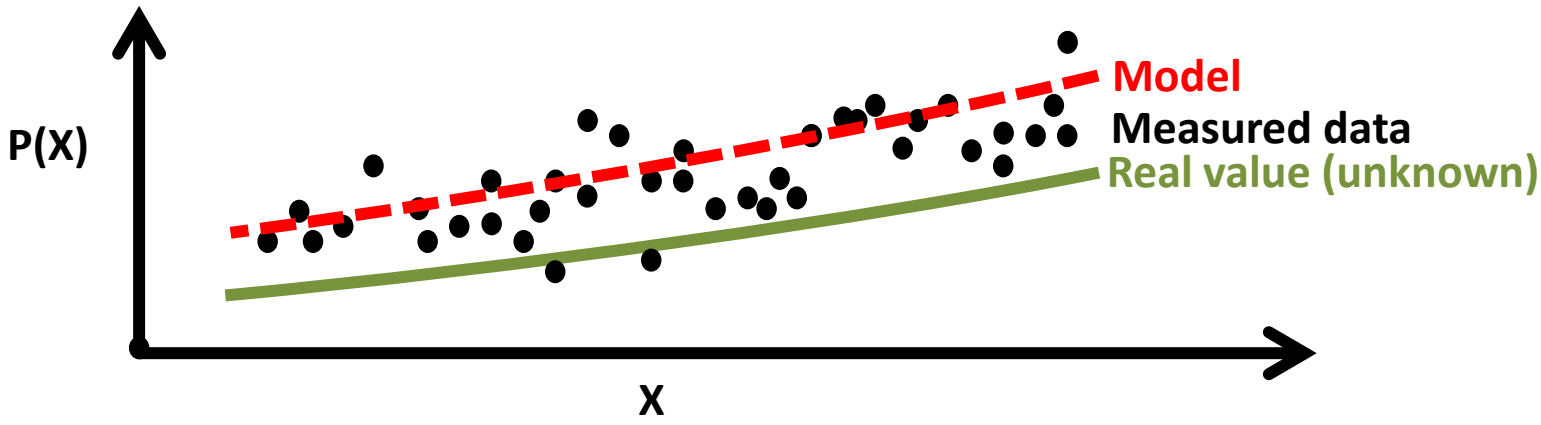
$$\text{Maximum error} = \max(abs((sim_i - mea_i)/\max(mea_i)))$$

$$\text{RMS error} = \text{sqrt}(\sum_{i=0}^{n}\left(\frac{sim_i - mea_i}{\max(mea_i)}\right)^2)/\text{n}$$

This often leads to a misconception of **accuracy**

# INTRODUCTION

Let us consider a measured quantity P(x)



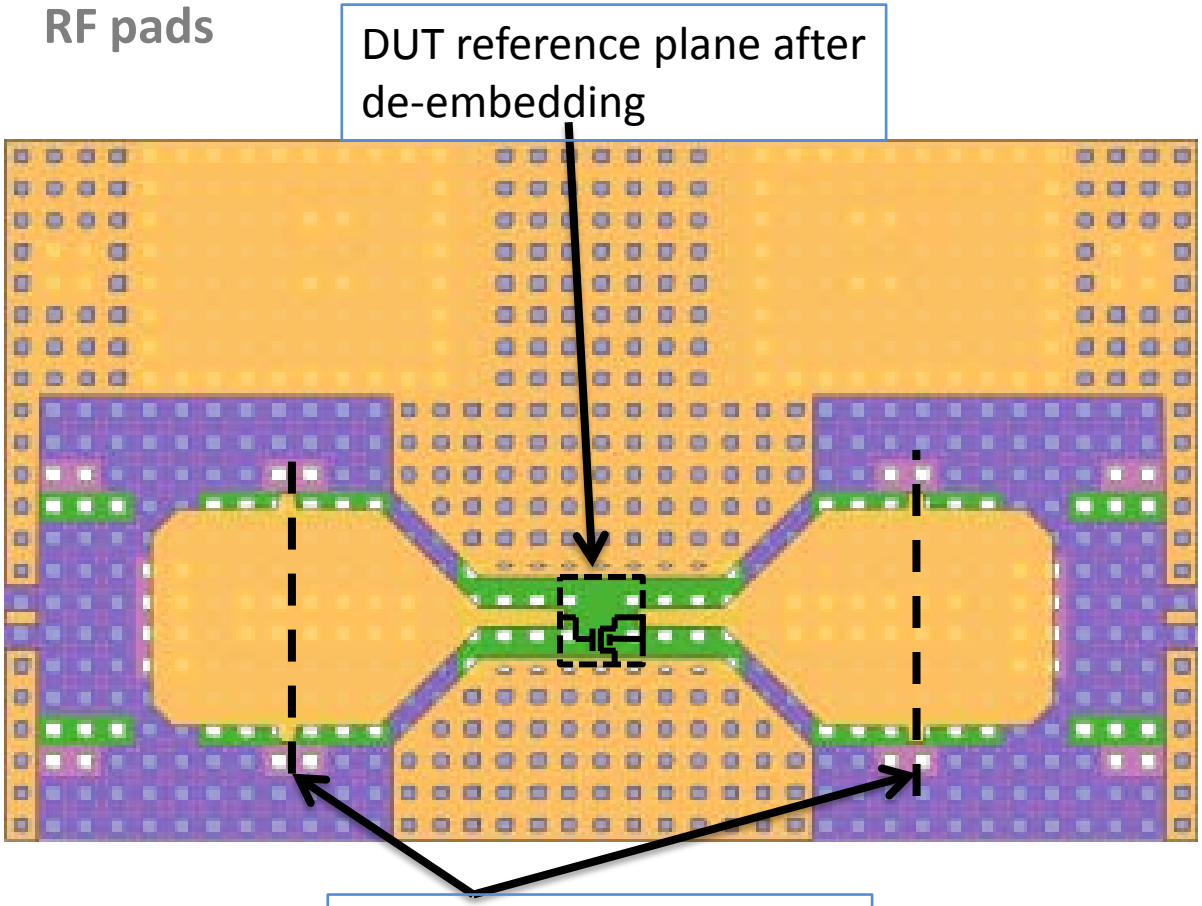

Accuracy criterion only considers the error between measured data and model

All aspects of data deviation from the real value are ignored !

This aspect is fundamental in RF domain and we will show later some examples

# DE-EMBEDDING

**After calibration, the reference plane is located in the center of the RF pads**



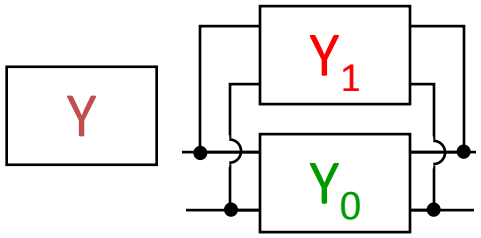

All parasitics associated with the pads and access lines are still included in measurements

The operation consisting in removing these parasitics is called **de-embedding**

# DE-EMBEDDING

## Useful matrix operations for de-embedding

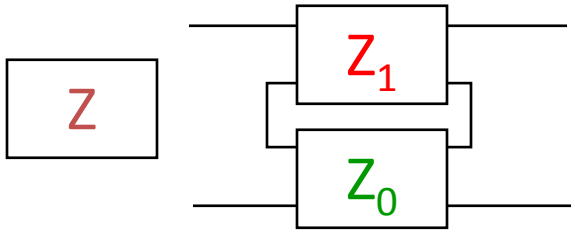
Y Matrix




$$[Y] = [Y_0] + [Y_1]$$

$$[Y_0] = [Y] - [Y_1]$$

Z Matrix

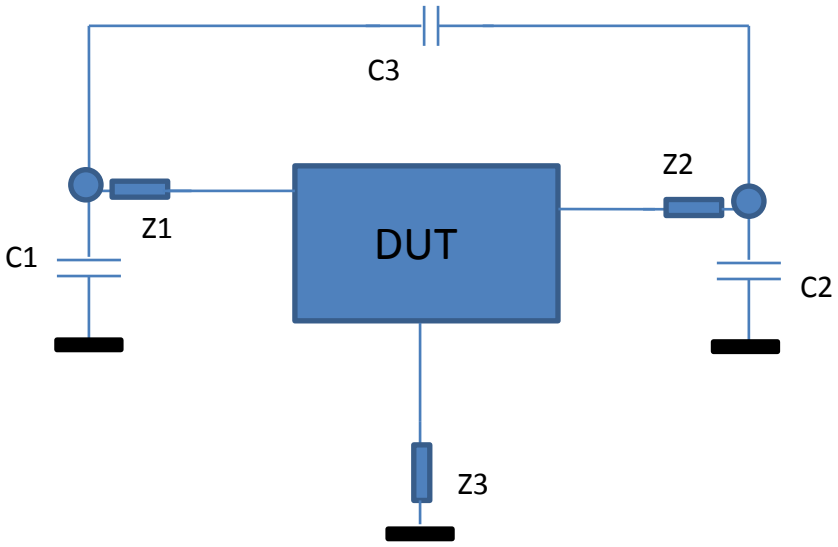



$$[Z] = [Z_0] + [Z_1]$$

$$[Z_0] = [Z] - [Z_1]$$

# DE-EMBEDDING

The industry standard : OPEN-SHORT de-embedding



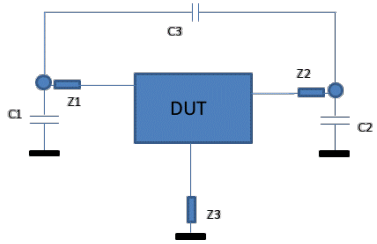

Assumption: Pad parasitics are modeled by parallel conductances and series impedances

**IF THIS IS NOT THE CASE, OPEN/SHORT DE-EMBEDDING CAN'T BE APPLIED**

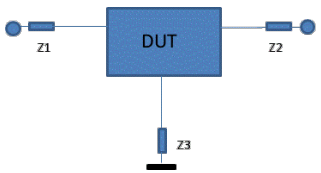
# DE-EMBEDDING

## OPEN-SHORT de-embedding

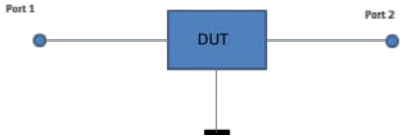
$(Y_{TOTAL})$



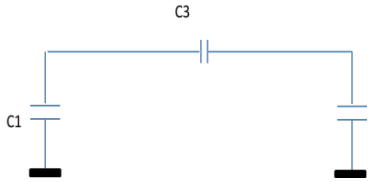

$(Z_{O\_DUT})$



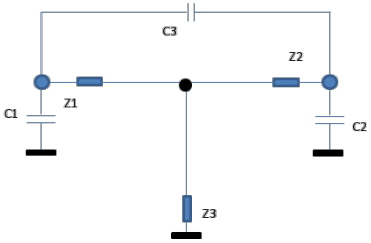

$(Z_{DUT})$



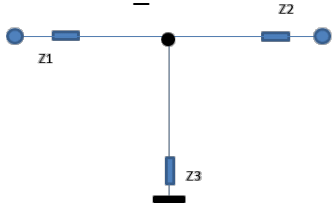

$(Y_{OPEN})$




$(Y_{SHORT})$




$(Z_{O\_SHORT})$



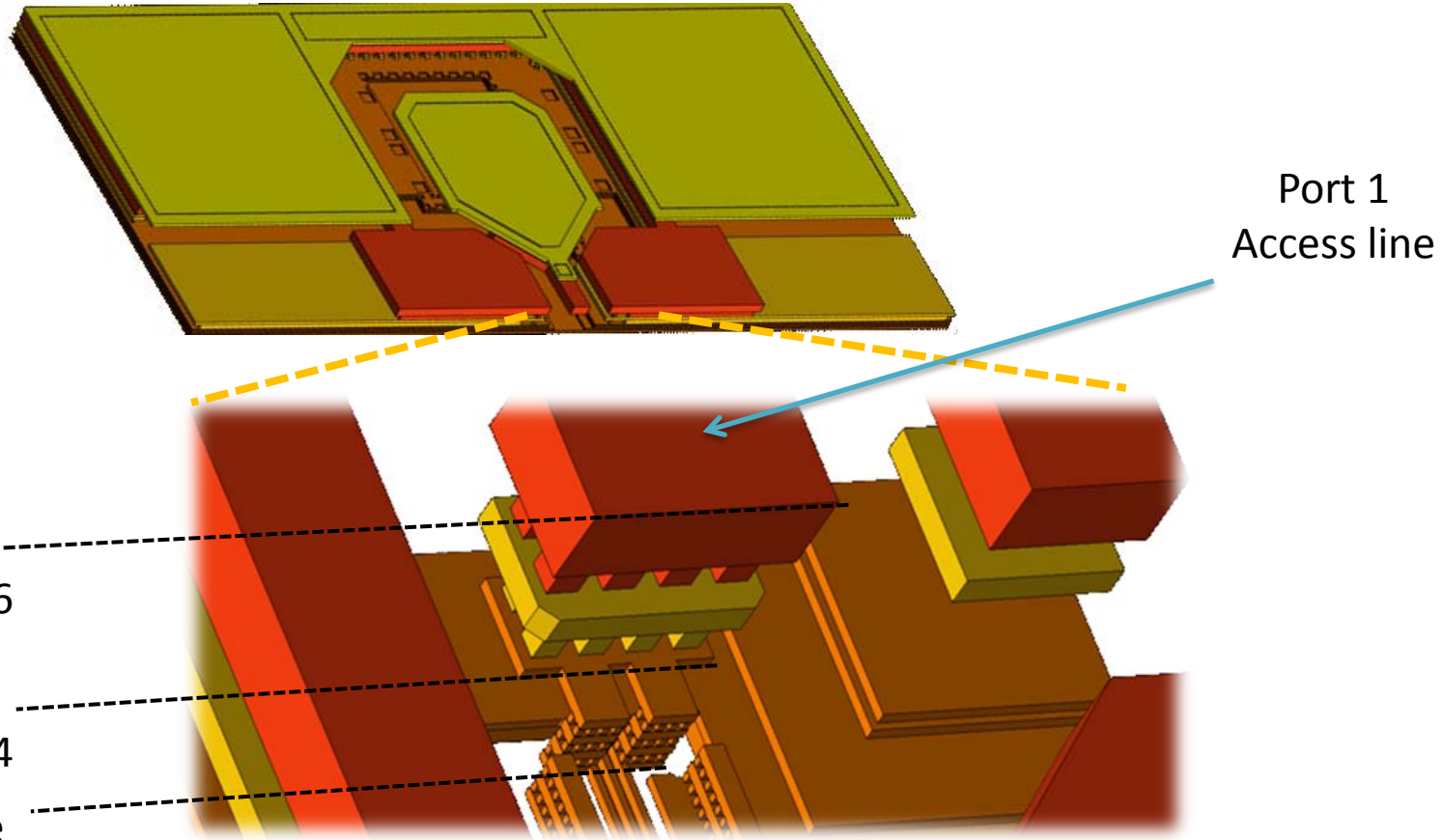

$(Y_{TOTAL}) - (Y_{OPEN}) = (Y_{O\_DUT}) \Rightarrow (Z_{O\_DUT})$

$(Y_{SHORT}) - (Y_{OPEN}) = (Y_{O\_SHORT}) \Rightarrow (Z_{O\_SHORT})$

$(Z_{O\_DUT}) - (Z_{O\_SHORT}) = (Z_{DUT})$

# DUT REFERENCE PLANE

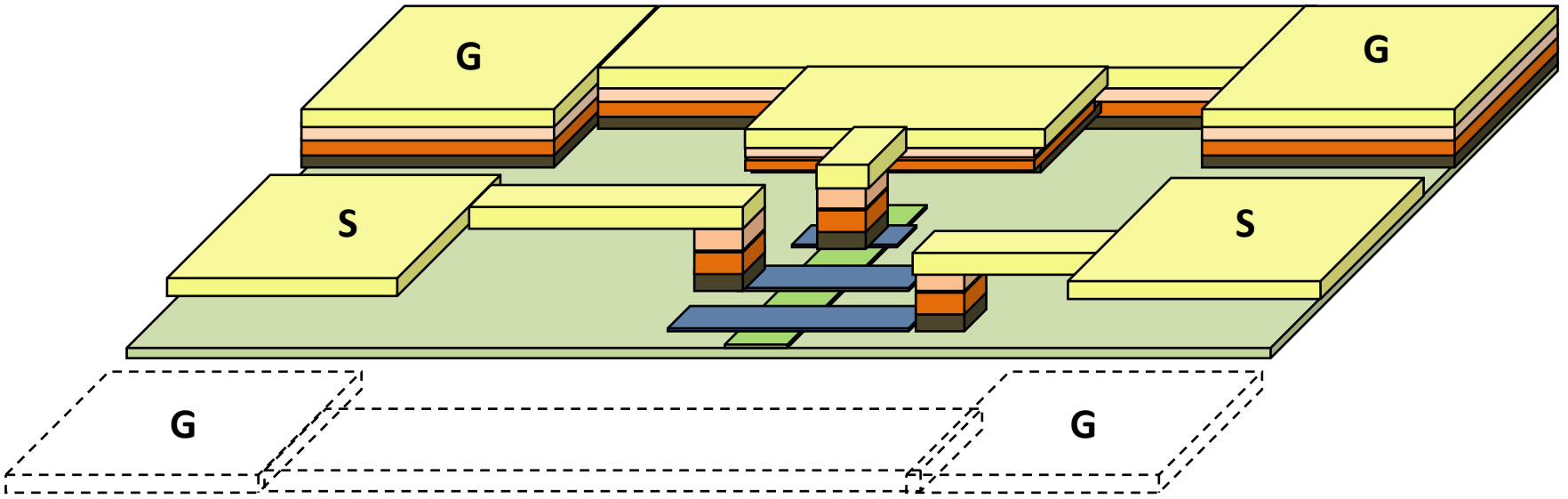
**Key point is where to stop de-embedding : which parasitics are part of the model ? What is upper frequency limit ?**



# DUT REFERENCE PLANE

RF-GSG test structure sketch (half): used to present the different options of reference plane definition

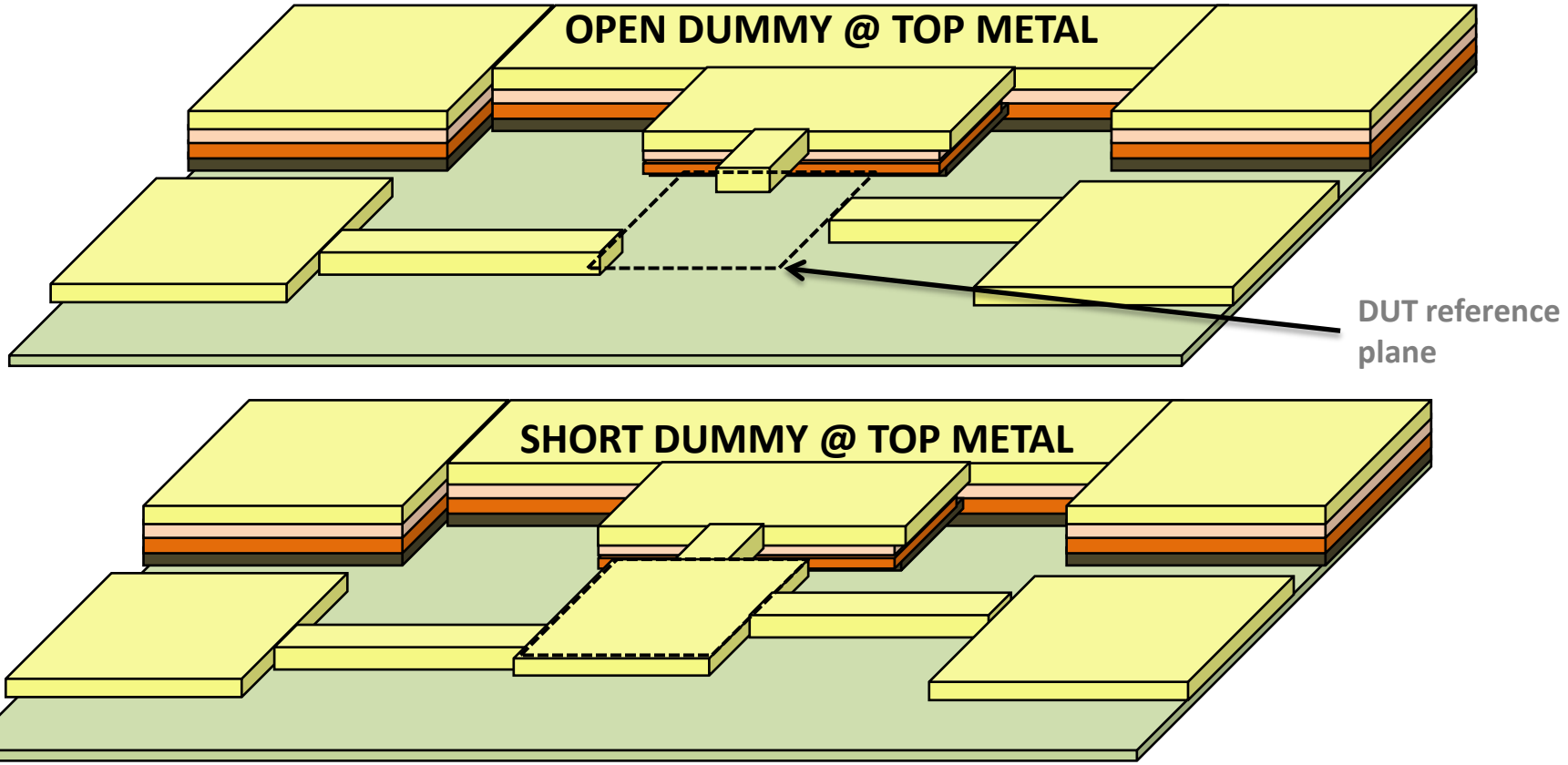
**Ground shield not shown for simplicity**



# DUT REFERENCE PLANE

Reference plane at TOP METAL :

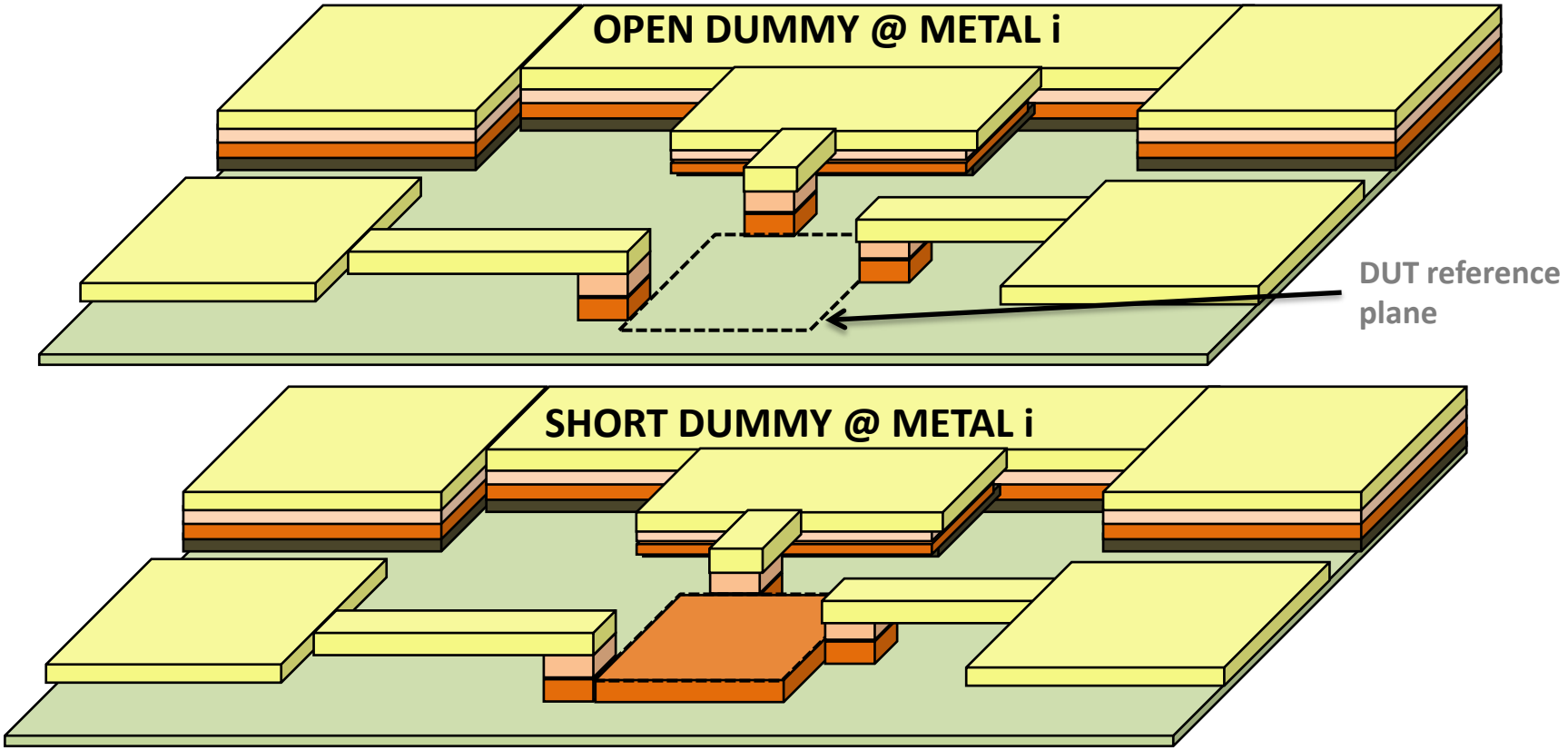
- Most parasitics are part of the model, model is a Black box/ layout fixed
- More “ideal” structures (better at high frequency)



# DUT REFERENCE PLANE

Reference plane at Intermediate METAL : trade off

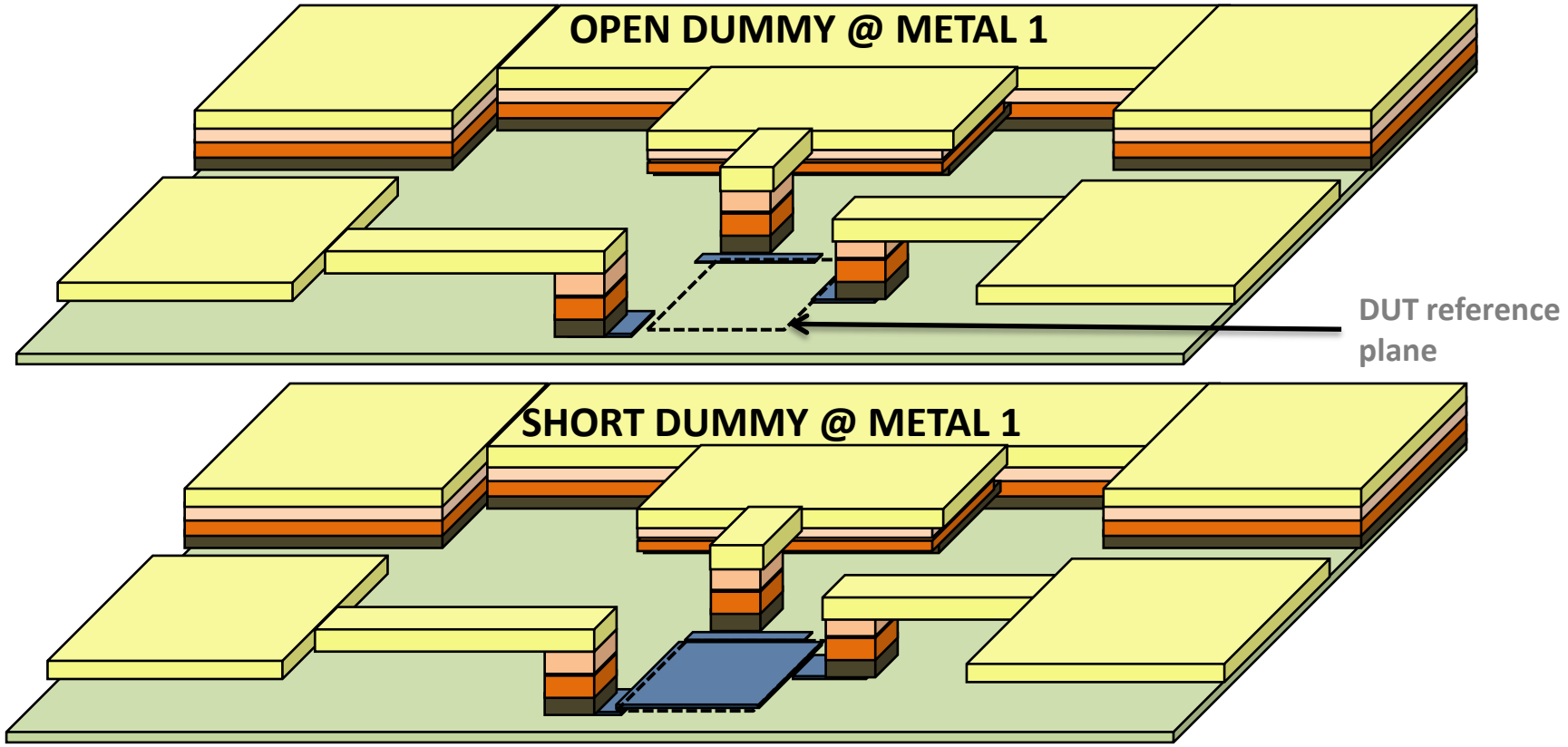
Useful when Pcell has M2 or M3 pins for instance



# DUT REFERENCE PLANE

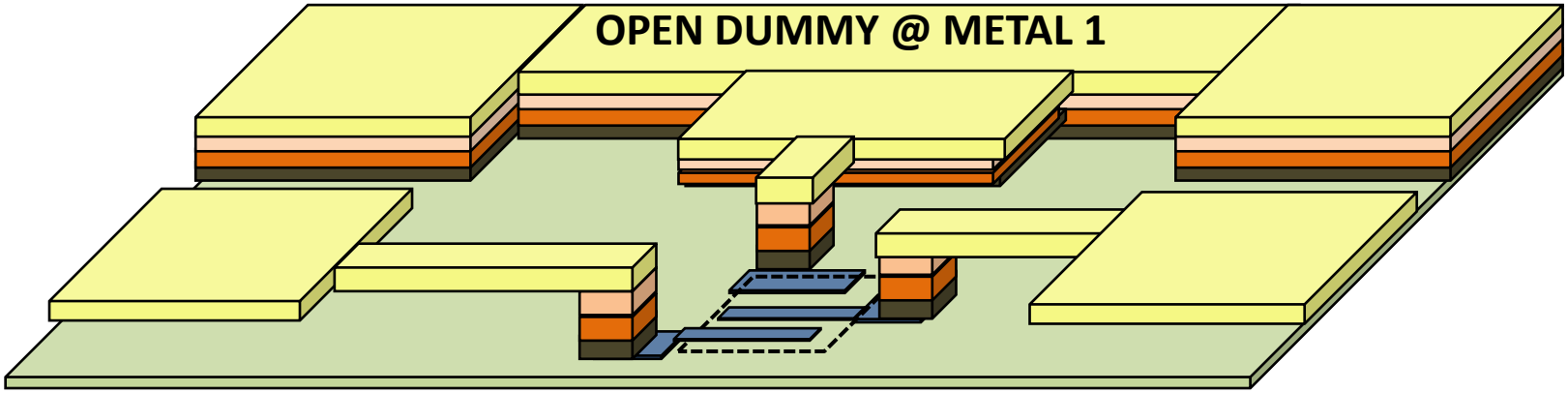
Reference plane at METAL 1: remove almost all parasitic, but HF behavior deviates from ideal assumptions

**Design is challenging**



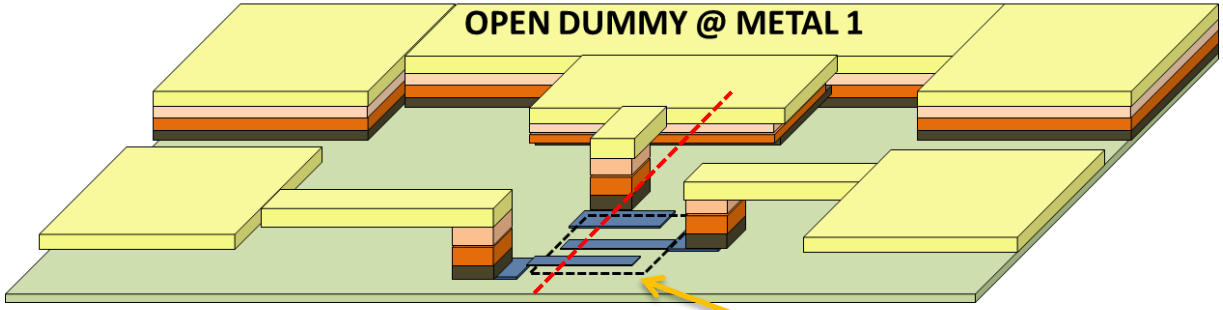
# DUT REFERENCE PLANE

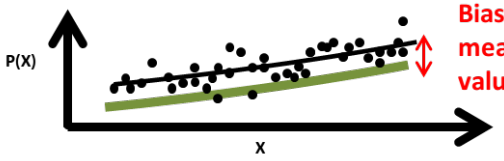
Common Mistake: leave some metal lines within the DUT reference plane

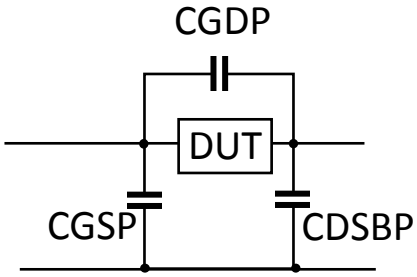


# DUT REFERENCE PLANE

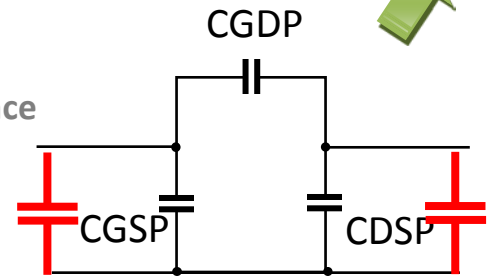
## Pay attention to fake parasitics to ground



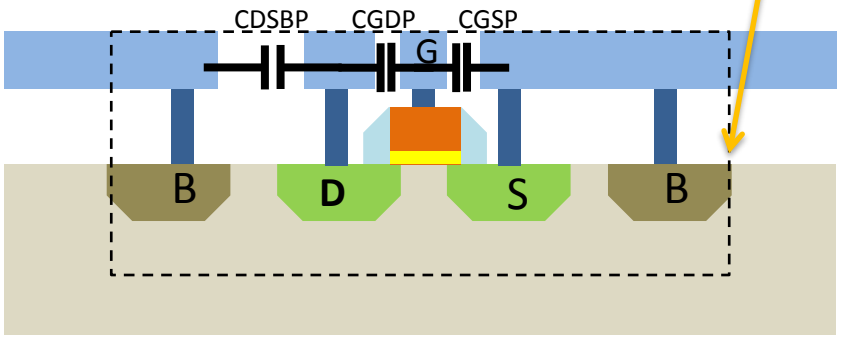



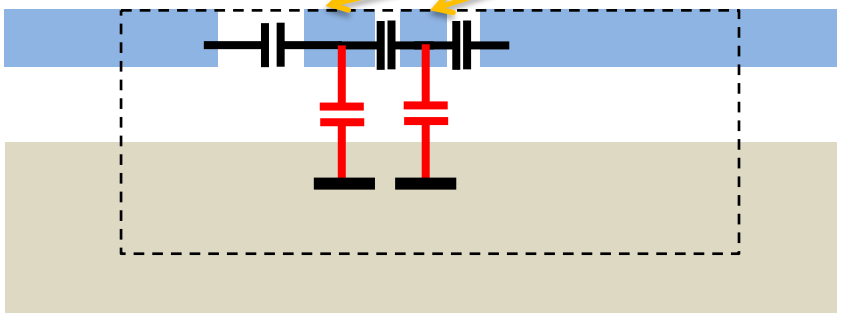




DUT reference plane




Remaining metal inside reference plane



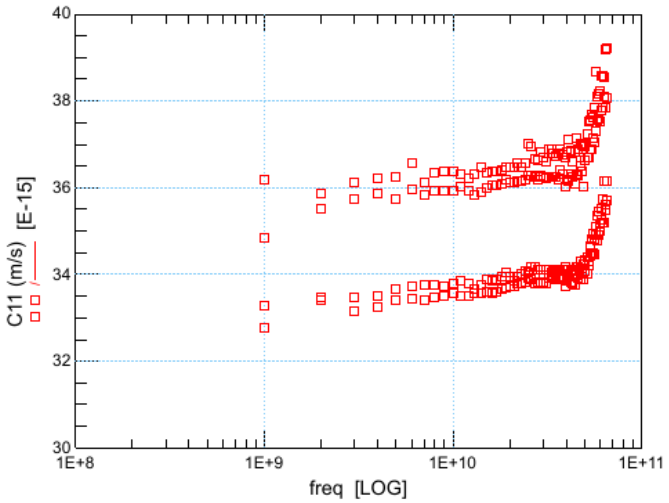



# DUT REFERENCE PLANE

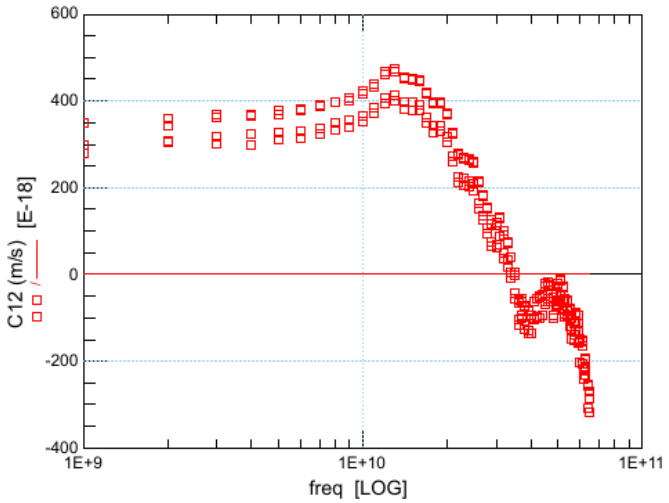
Example of complete OPEN DUMMY measurement (down to M 1):

- At high frequency the capacitance starts to deviate from ideal behavior
- At high frequency, the de-embedding is inaccurate

**Capacitance @ Port 1**




**Capacitance between Port 1 and port 2**




**Several geometries of OPEN DUMMY @ METAL 1**

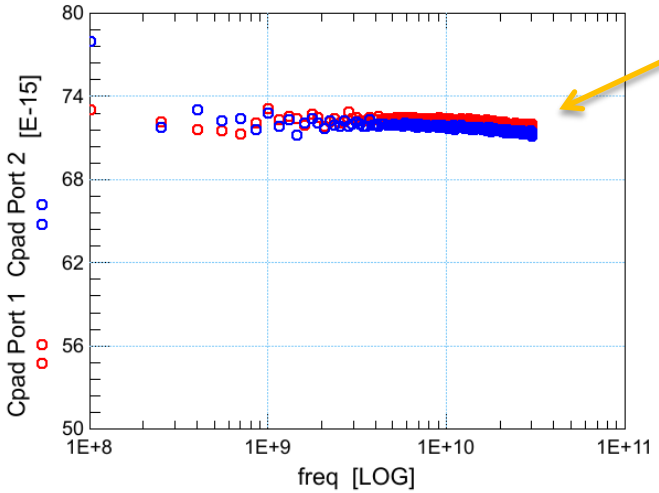
# RF TEST STRUCTURES

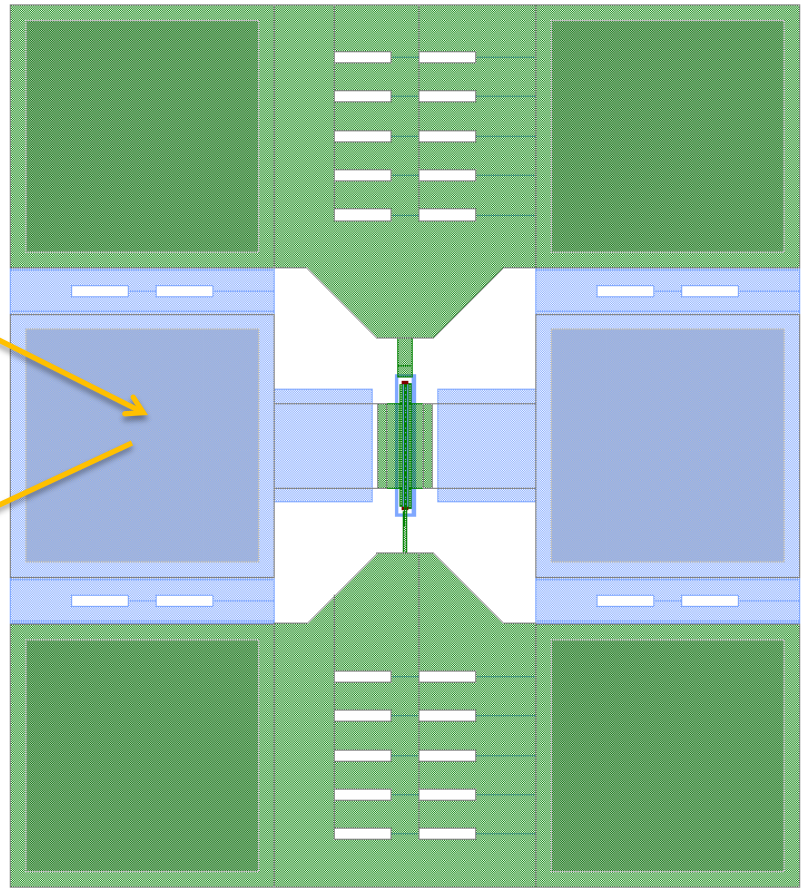
Common mistakes

Pad area is large Cpad ~ 72 fF
Optimized pads down to 20 fF

5% of error on this pad is 3.6fF
5% of error on optimized pad is only 1 fF

Hint: Cgs of the smallest devices ~ 1-2 fF



**This effect is confirmed by measurements:**
**CGD extracted from S parameters is always more accurate than CGS**

# RF TEST STRUCTURES

Common mistakes

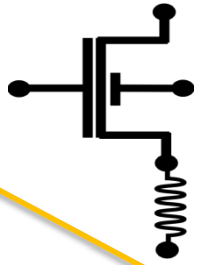
Note: The shorting layer in the SHORT is also inductive when NF<<1 !

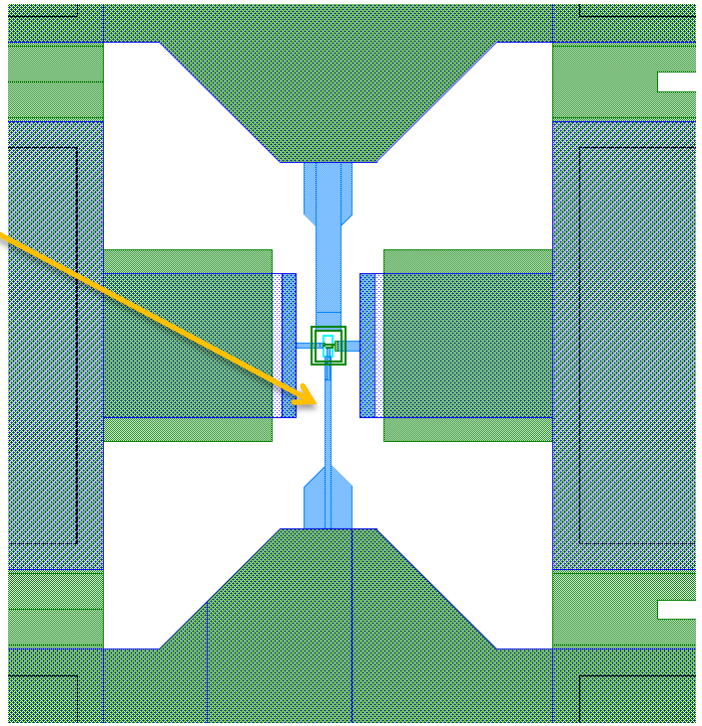
Source connection to ground is inductive

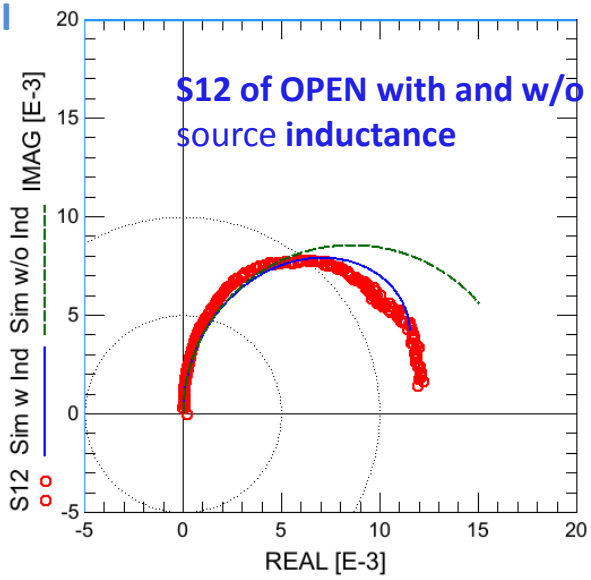
This inductance is part of the OPEN dummy

The OPEN is not a PI network of parallel conductances anymore

OPEN-SHORT De-embedding assumptions Fail





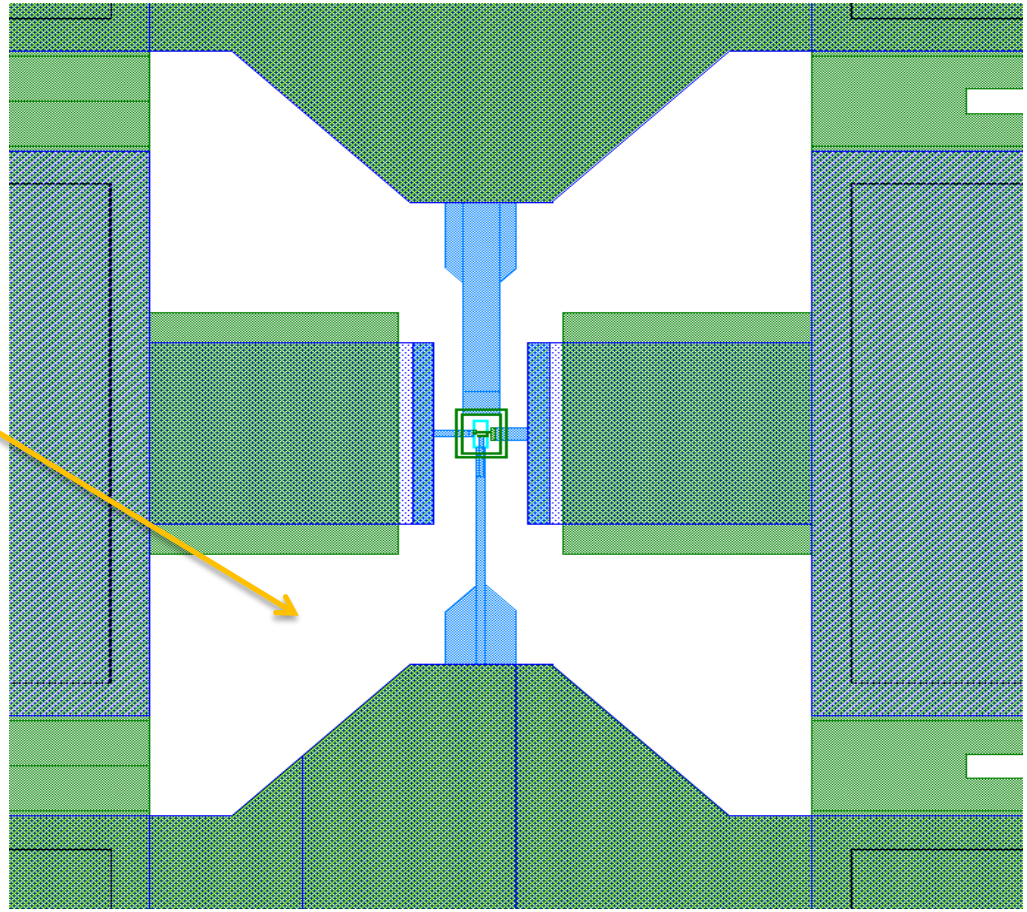


# RF TEST STRUCTURES

## Common mistakes

No ground plane:

- Ground return path is too long
- Substrate coupling can occur between P1 and P2



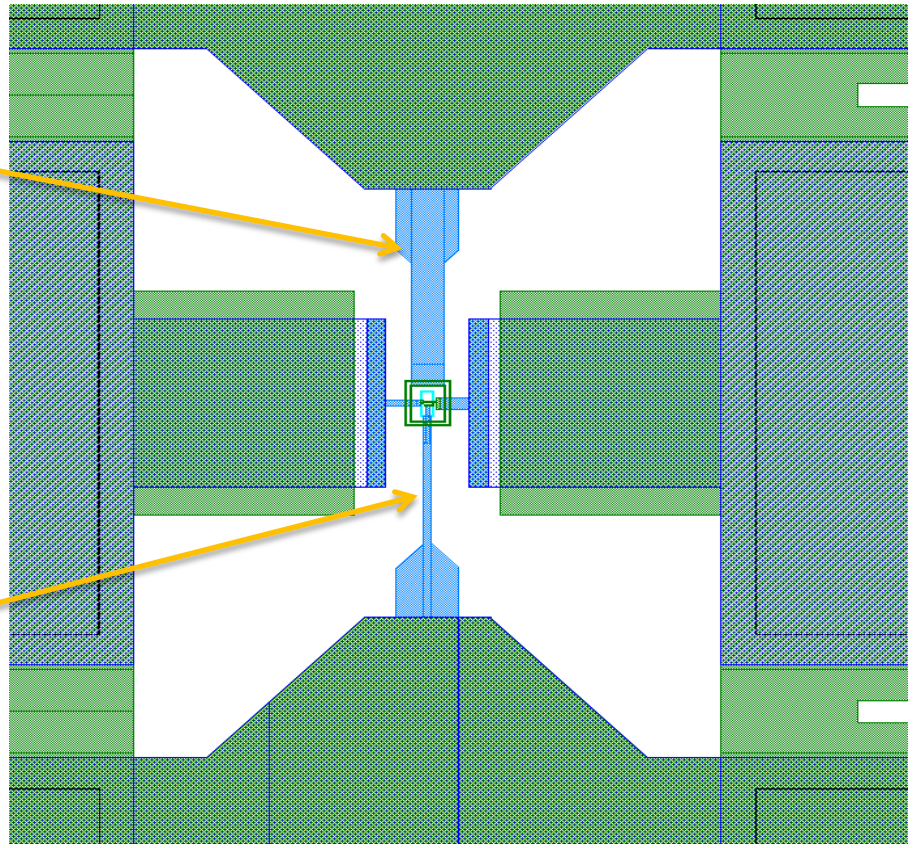
# RF TEST STRUCTURES

## Common mistakes

Substrate / body has a separate connection to ground:

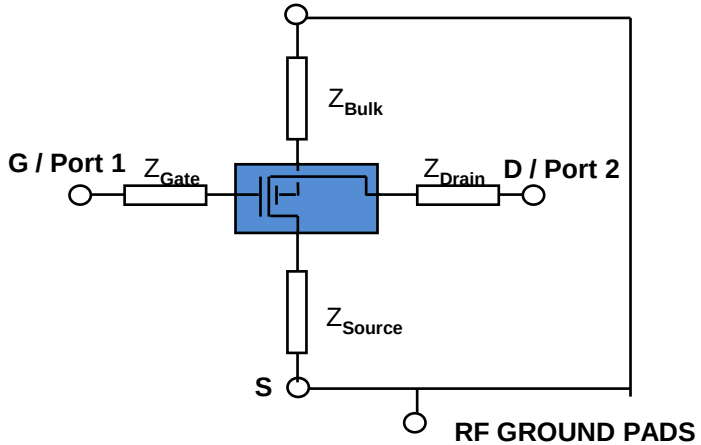
- Unclear DUT reference plane
- **Erroneous SHORT dummy**

Source connection



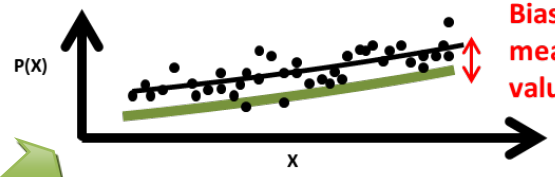
Critical for PMOS or isolated Nmos or SOI MOS

# RF TEST STRUCTURES

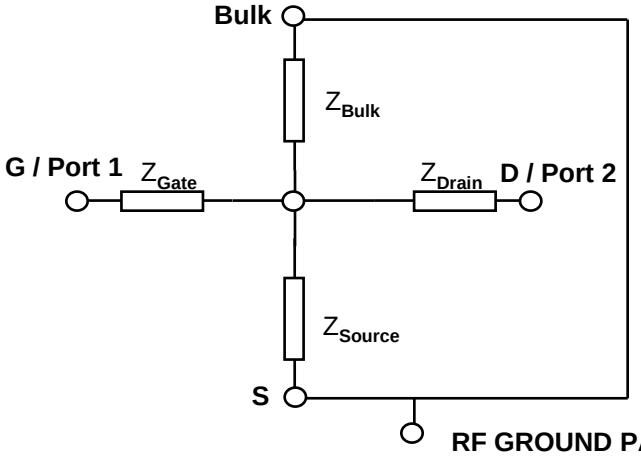


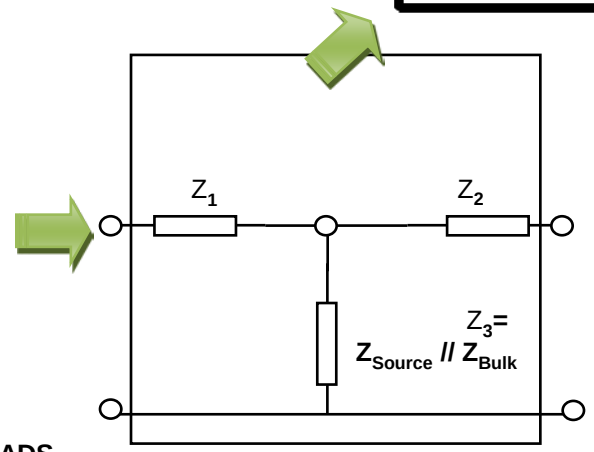

**The SHORT dummy underestimated the Z3 impedance by a factor 2**

**The source path to ground is not correct !**




**Bias between measured and real value !**



# RF TEST STRUCTURES

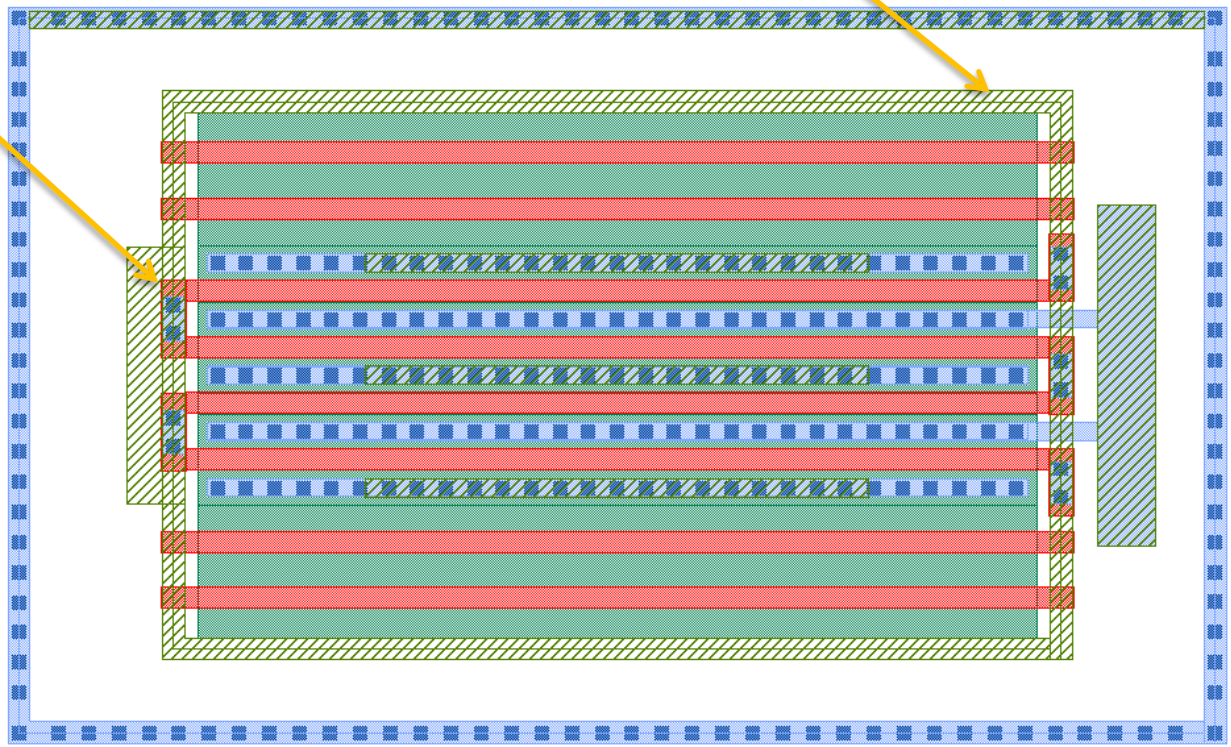
Common mistakes

Only one contact per gate finger

The model may or may not include this contact resistance, but this degrades performance

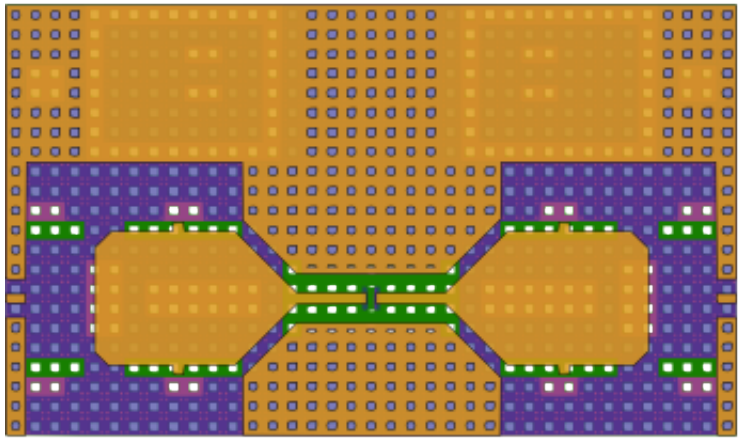
1 via can have the same order of magnitude as the gate poly resistance

Other side of gate finger connected with inductive / resistive path



# RF TEST STRUCTURES

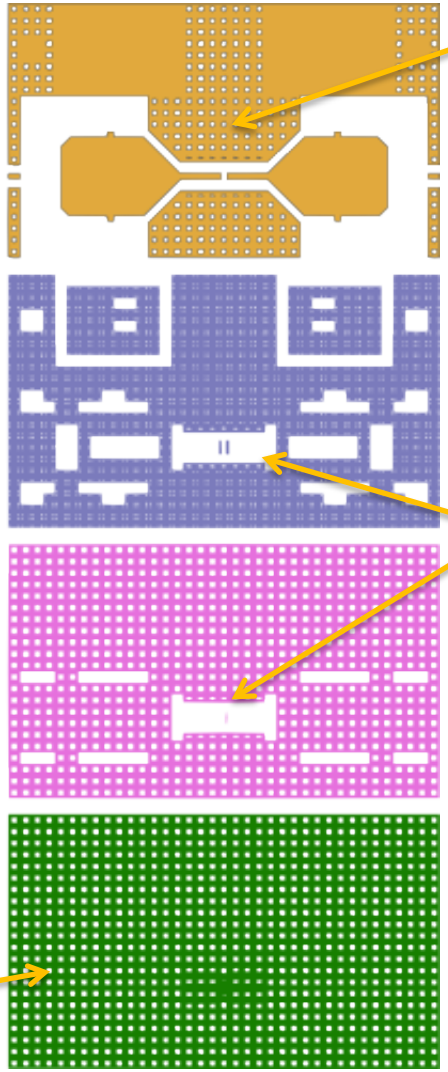
A better example



The whole structure complies with DRC density requirements

No random dummy filling / cheesing needed -> no extra parasitic

M1 ground shield avoids direct substrate coupling + better HF behavior



Mtop helps minimizing the ground return path

Small pad area

Ground pads are shared

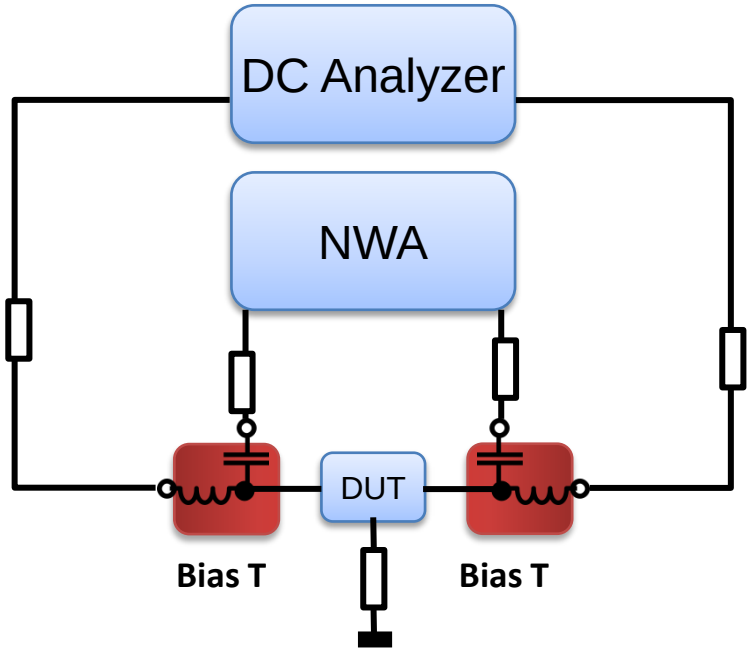
M2, M3, Mi ground walls allow clear DUT reference plane

Any connection (S/B) to ground is in place (vertical)

# Parasitic resistances in DC

**Let us consider a typical S parameter test setup**

- The de-embedding will remove the parasitic elements from S parameters but not from the DC data !

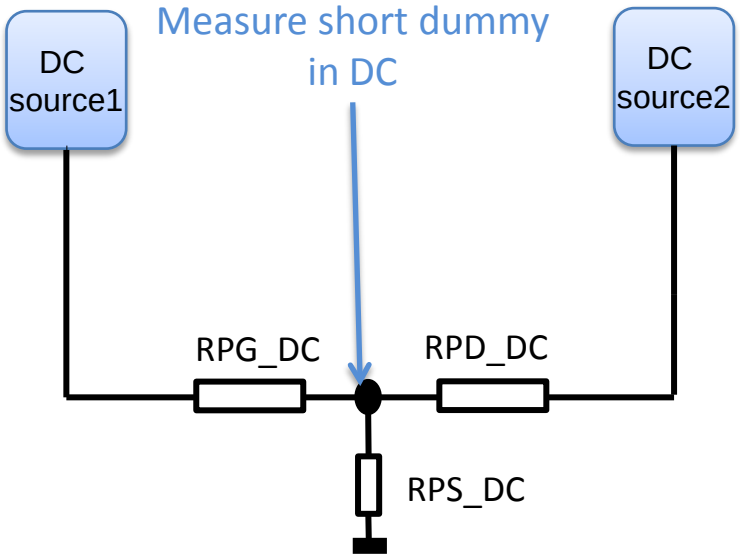


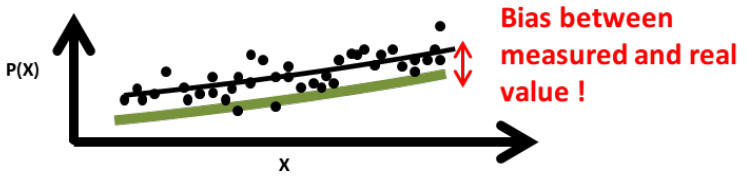

The DC path is usually longer, with more series resistance due to bias Tees
(Ground return path has to be considered too)

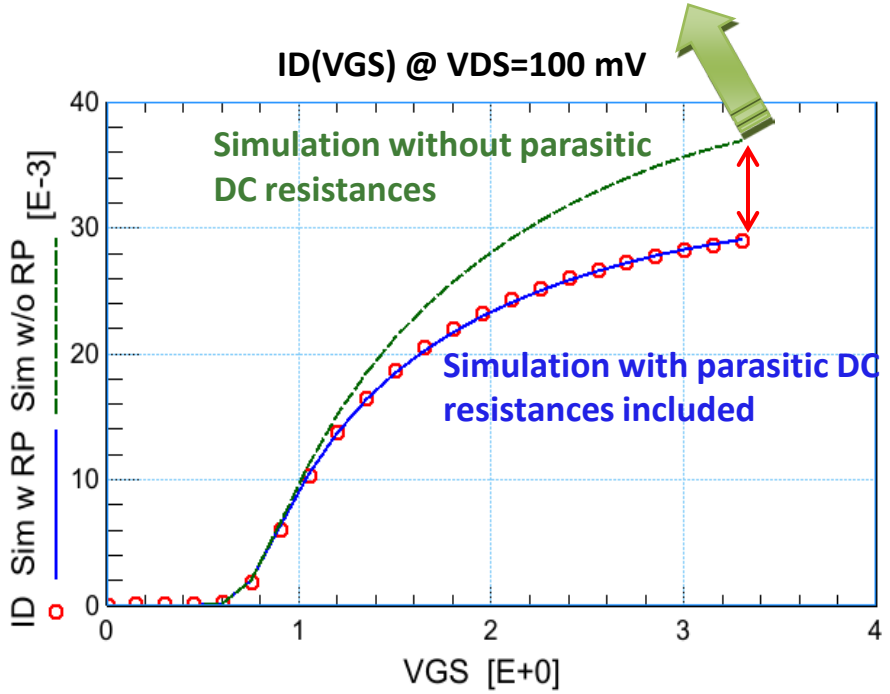
# Parasitic resistances in DC

Measured DC parasitic resistances values:

- RPG_DC= 525 mΩ
- RPD_DC= 585 mΩ
- RPS_DC= 154 mΩ



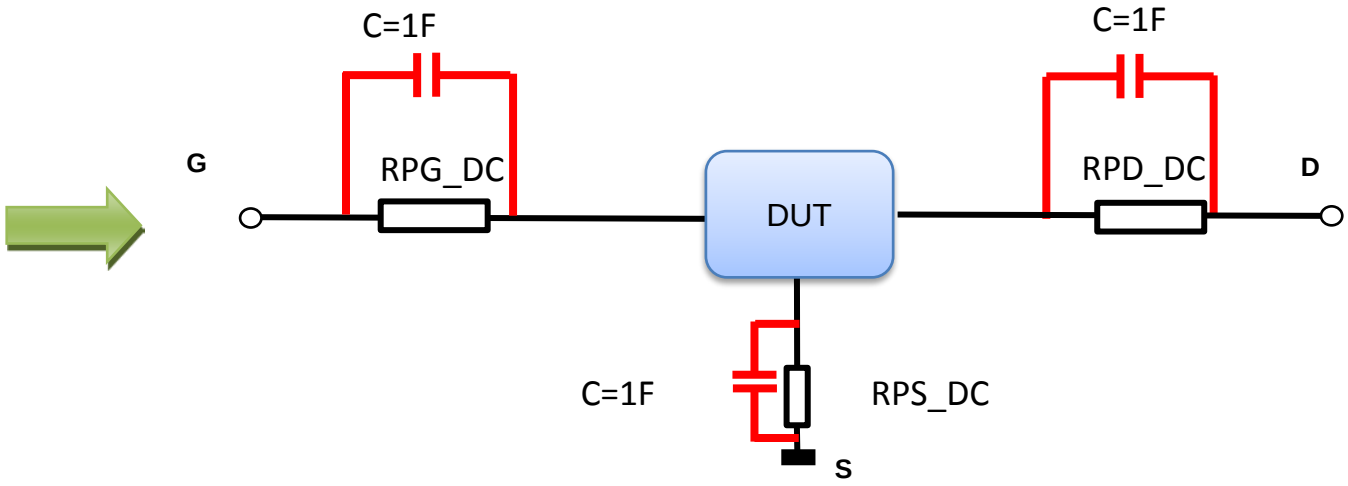

NMOS structure, W=10 µm, L=0.35, **NF=64**

# Parasitic resistances in DC



Parasitic DC series resistances need to be modeled via an embedding sub-circuit

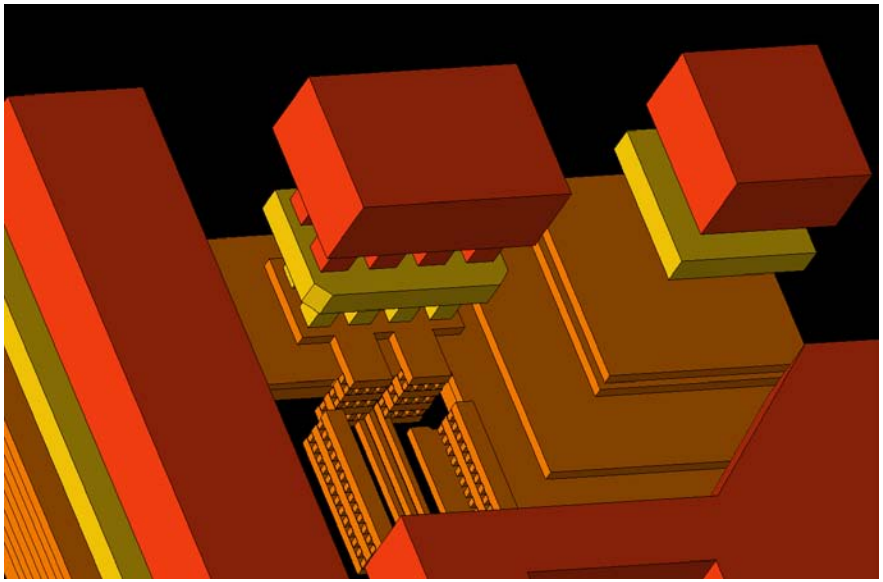
They are not removed by de-embedding !



# Parasitic resistances in DC

**The SHORT Dummy structure must be consistent and well designed**

- **How to insert the shorting layer ?**



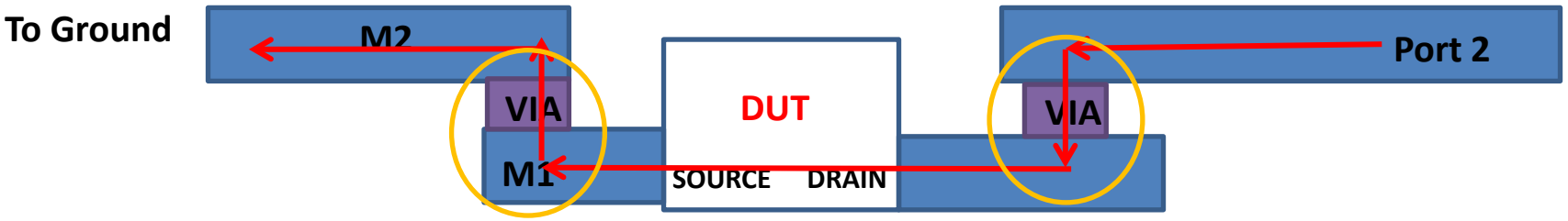
Metal stack down to transistor adds series resistance too

# Parasitic resistances in DC

- Schematic Cross section of RF structure
- Critical if  number of vias to DUT is small

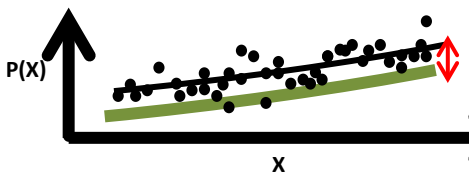
Main resistive contributions

Current **flow from P2 to GND in DUT connection**



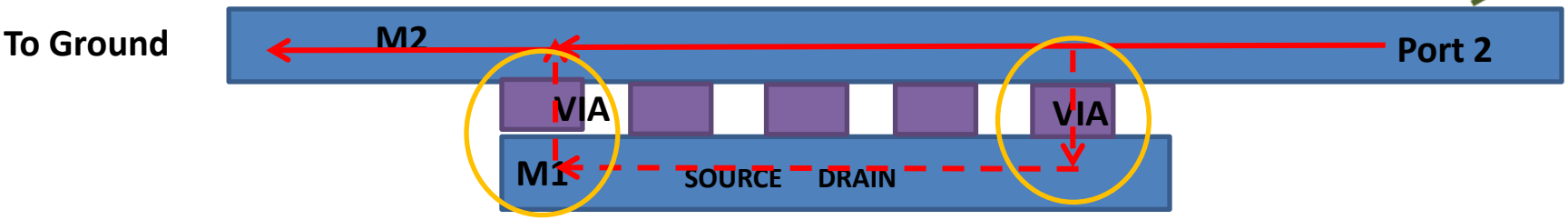
# Parasitic resistances in DC

How to insert the shorting layer ?

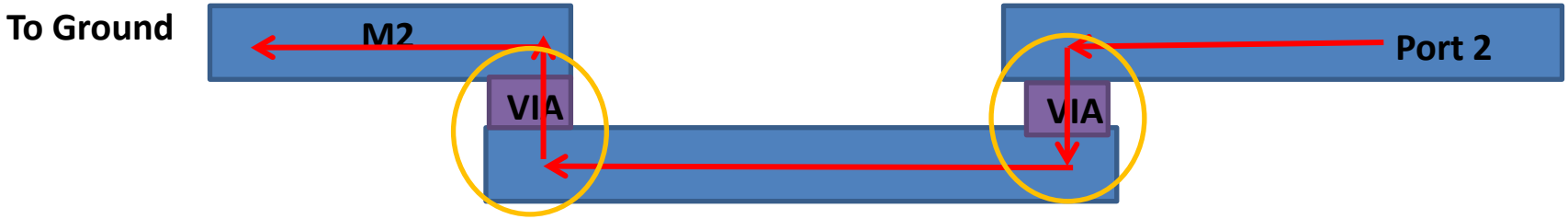



Bias between measured and real value !

The SHORT dummy below ignores 2 of the main parasitic series contributions

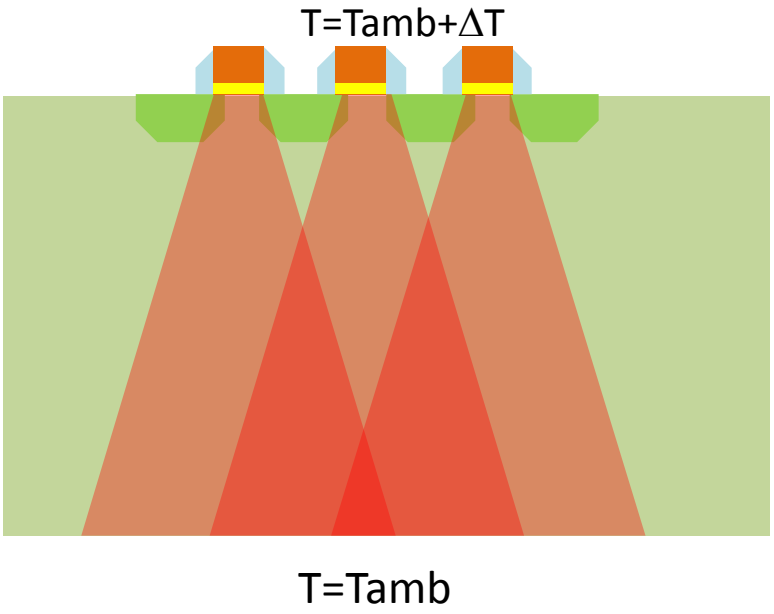


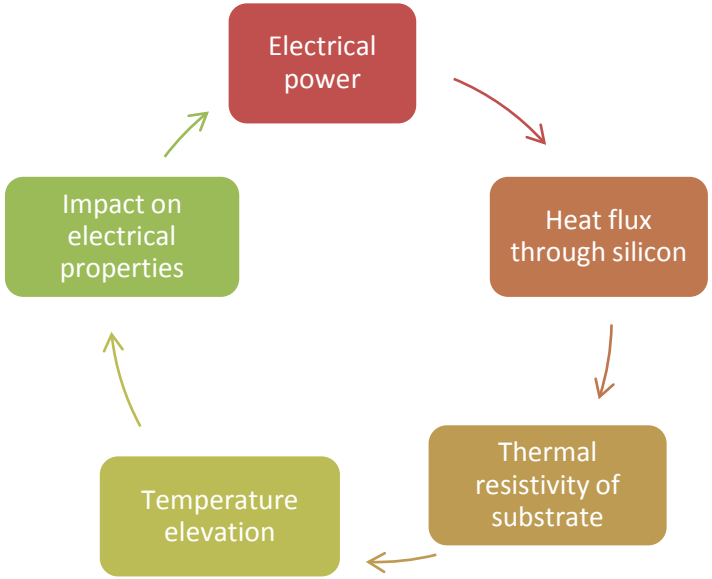

This SHORT dummy correctly takes into account the last via contribution

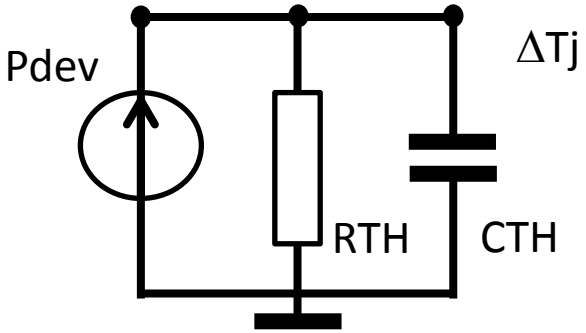


# SELF-HEATING

## What is self heating ?



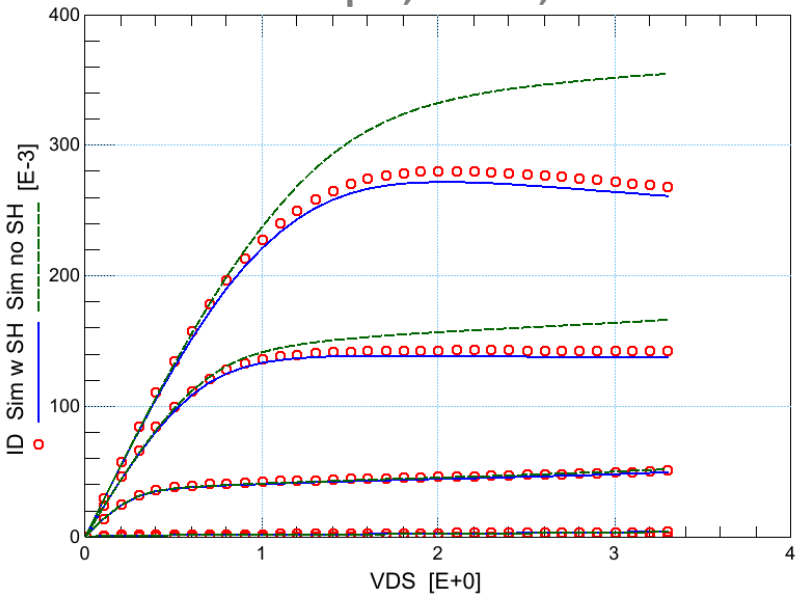



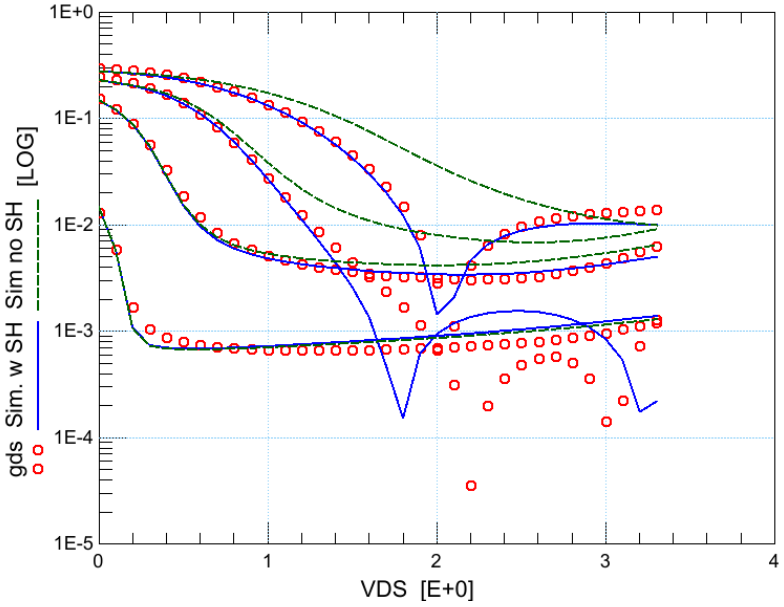
# SELF-HEATING

## Self-heating has significant impact for large devices

- ID(VDS) curve & gds (VDS) are strongly impacted
- Negative slope for large devices is easy to detect: need to use self-heating model (such as PSP 103.3)

NMOS W=10 µm, L=0.35, **NF=64**



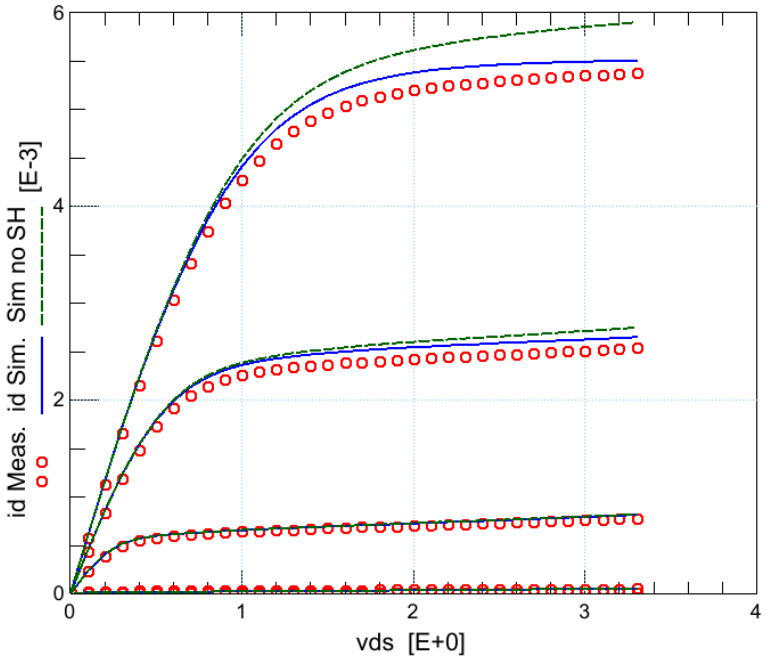
# SELF-HEATING

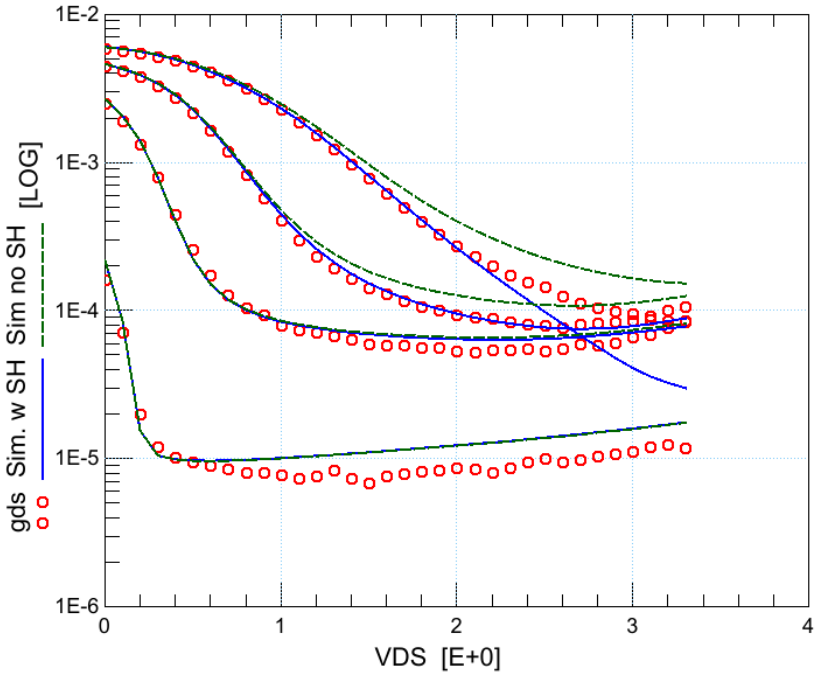
## Self-heating still important for smaller geometries: why ?

- ID(VDS) curve & gds (VDS) are still impacted
- No observed negative slope : but self-heating model still required !
- Self heating could be compensated by tuning saturation voltage and DIBL parameters

**Catastrophic for RF model !**

NMOS W=10 µm, L=0.35, **NF=1**

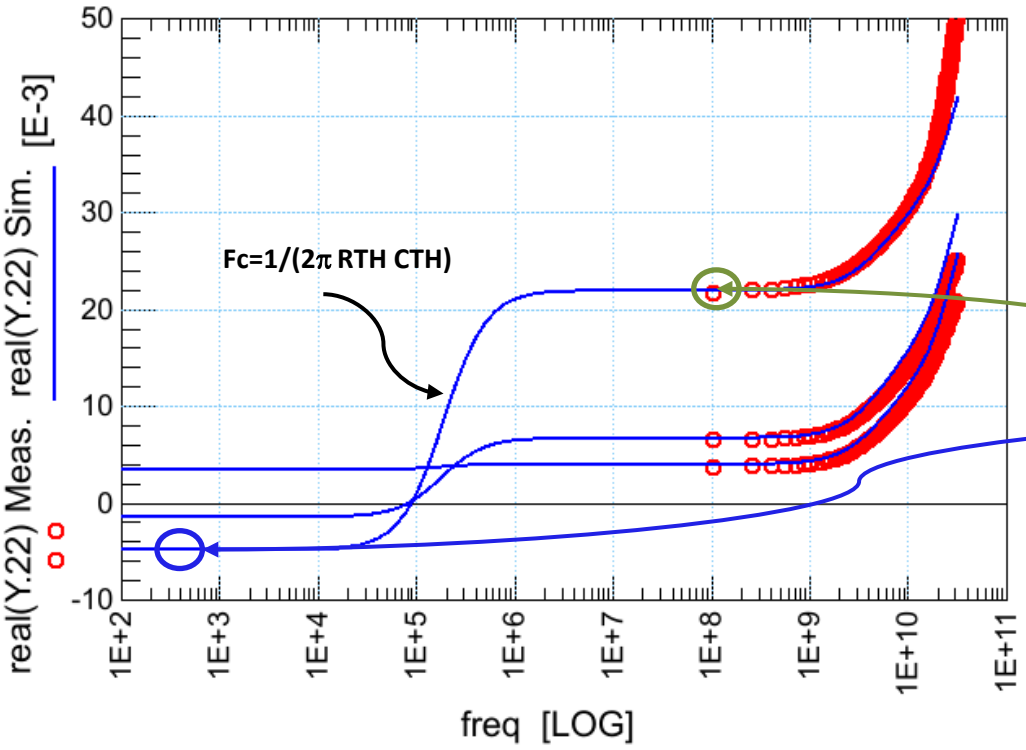


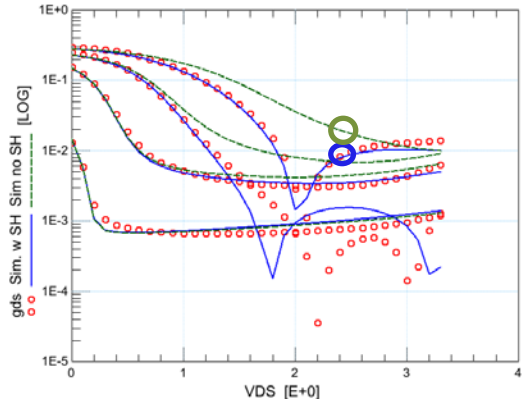



# SELF-HEATING

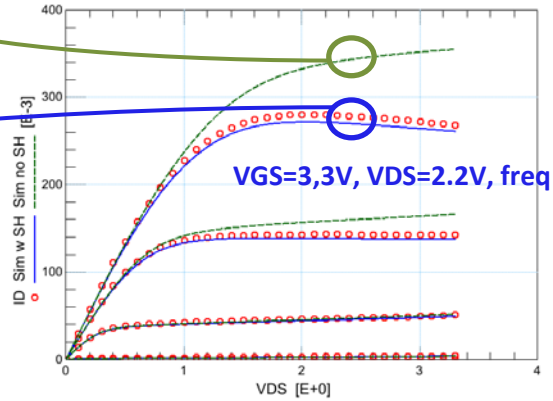
Self heating is a DC / low frequency effect (thermal resistance is shunted by thermal capacitance for frequencies larger than a few MHz)

NMOS W=10 µm, L=0.35, **NF=64**




VGS=3,3V, VDS=2.2V, freq > 1MHz

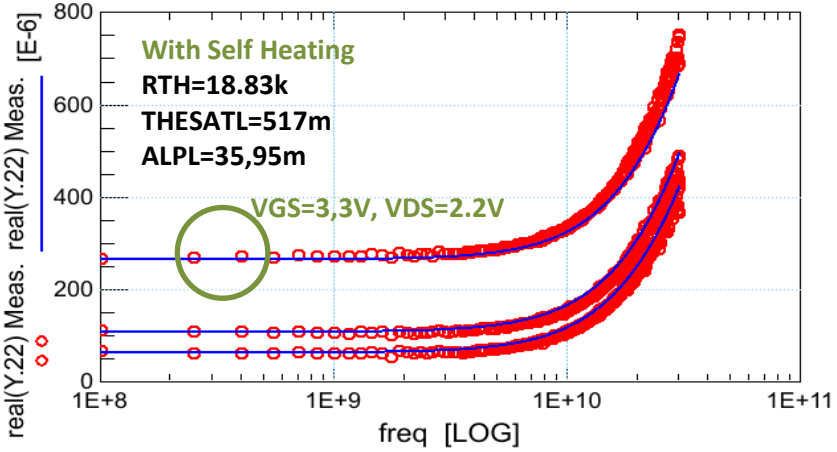


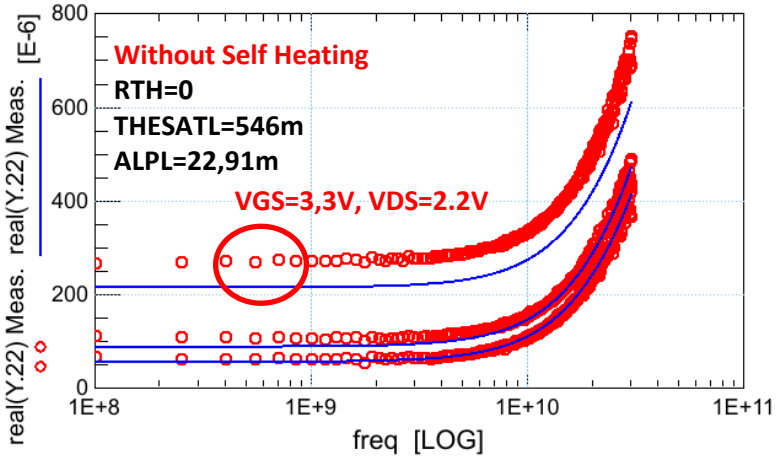

VGS=3,3V, VDS=2.2V, freq -> 0

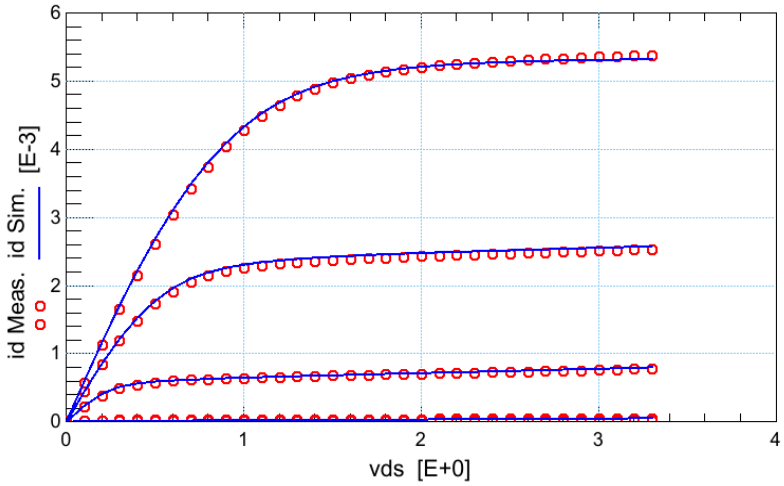
# SELF-HEATING

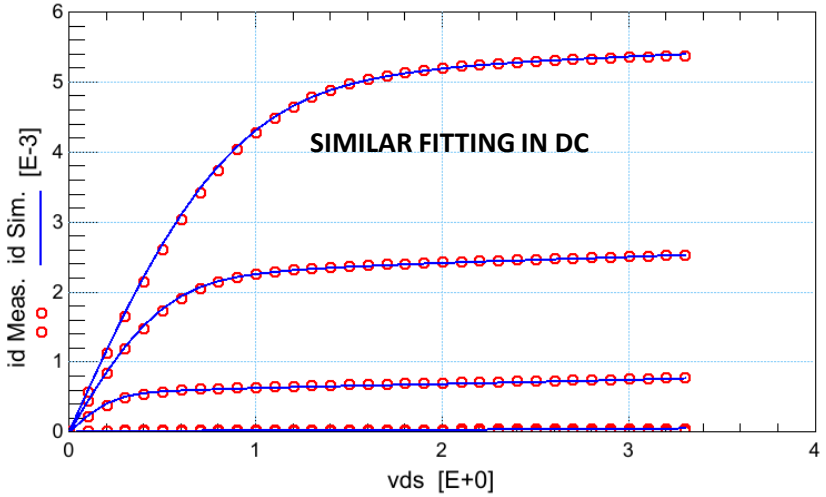
What if neglecting the self heating effect in baseband model ?

NMOS W=10 µm, L=0.35, **NF=1**



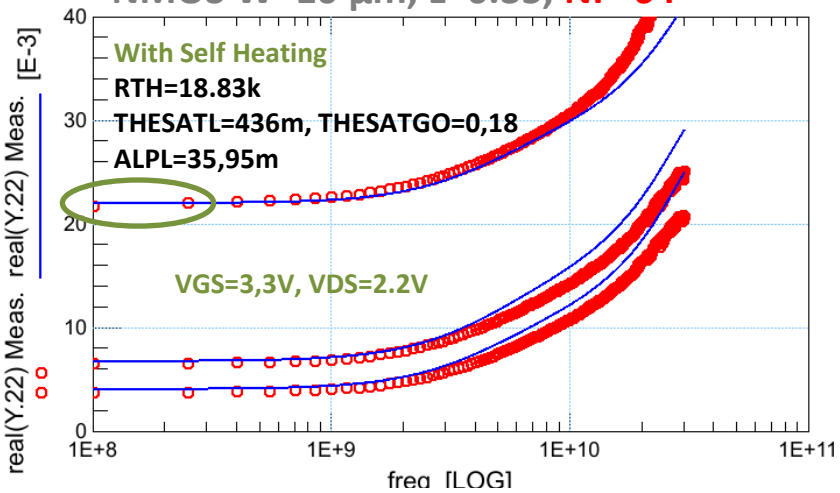



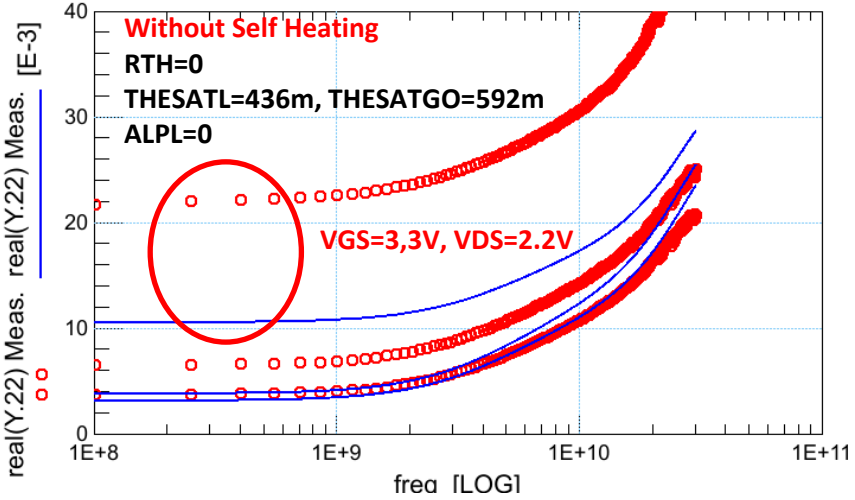



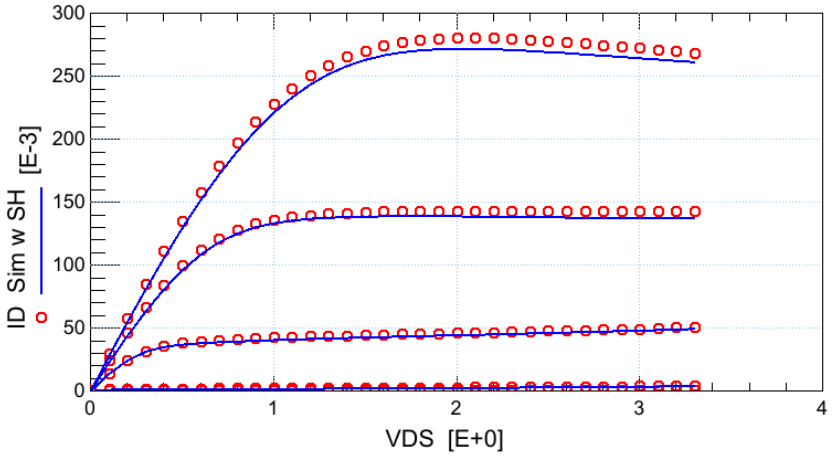
# SELF-HEATING

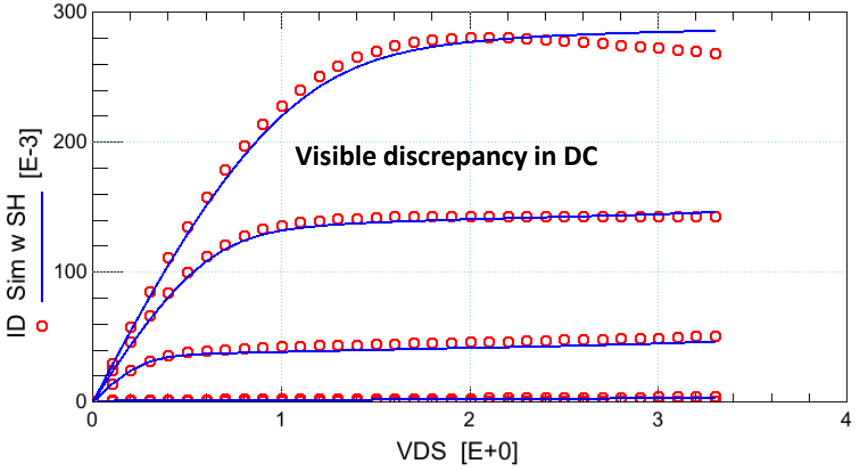
For larger device, the situation is worse

NMOS W=10 µm, L=0.35, **NF=64**



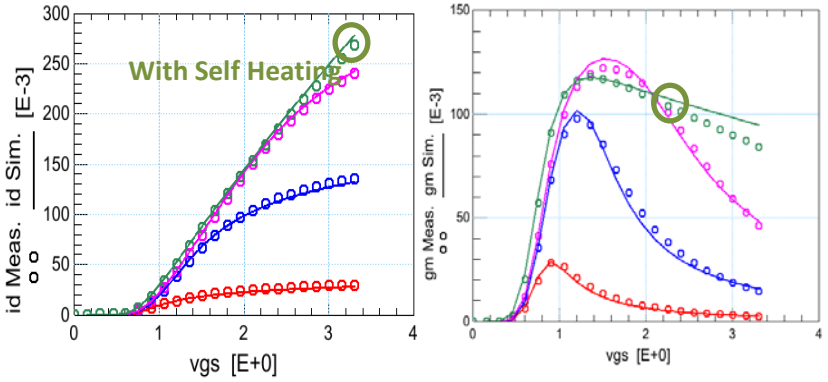



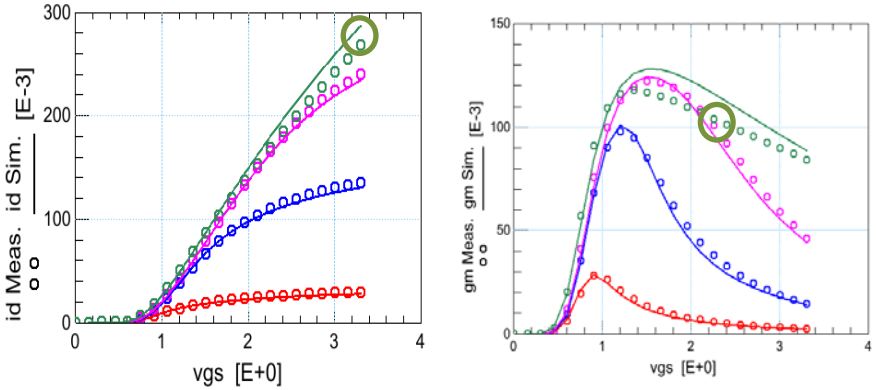



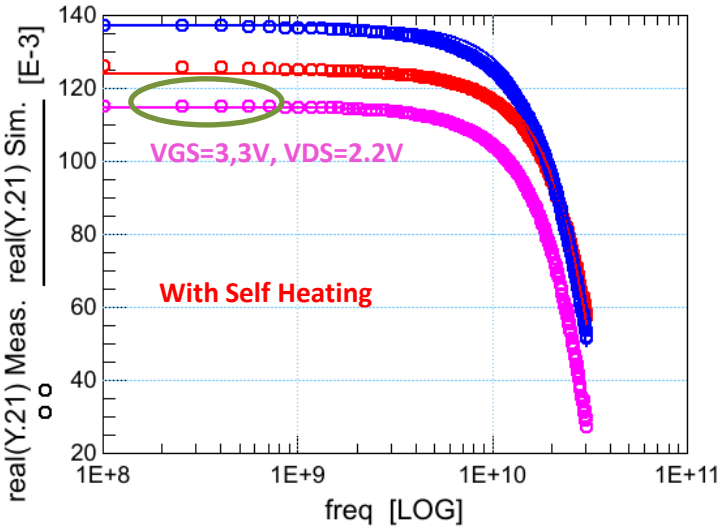
# SELF-HEATING

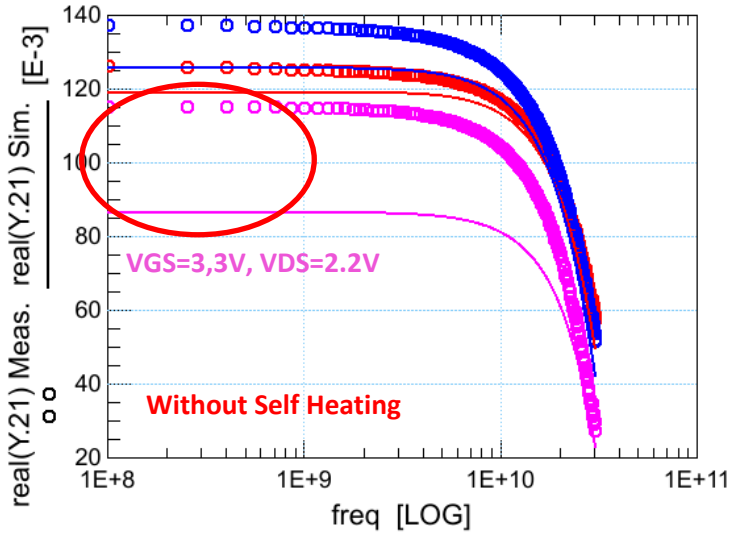
Same situation for gm

NMOS W=10 µm, L=0.35, **NF=64**



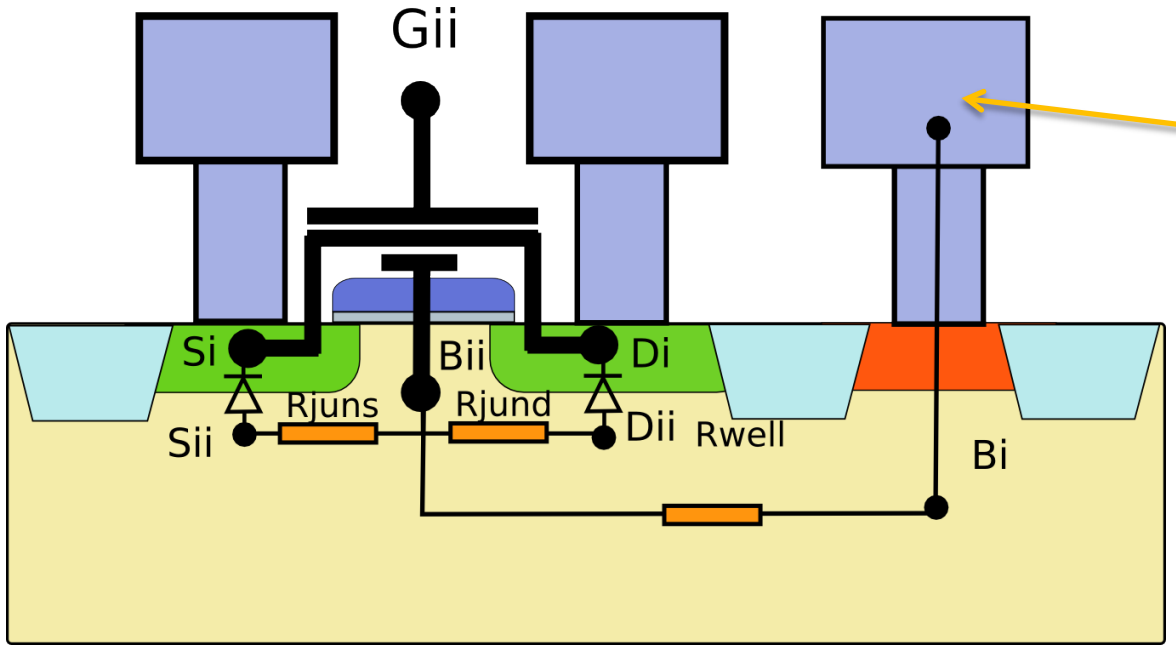



# SUBSTRATE MODELING

Simple substrate network model:
Each elements has its own scaling equation (inside sub-circuit model) to take into account NF, W and L variations

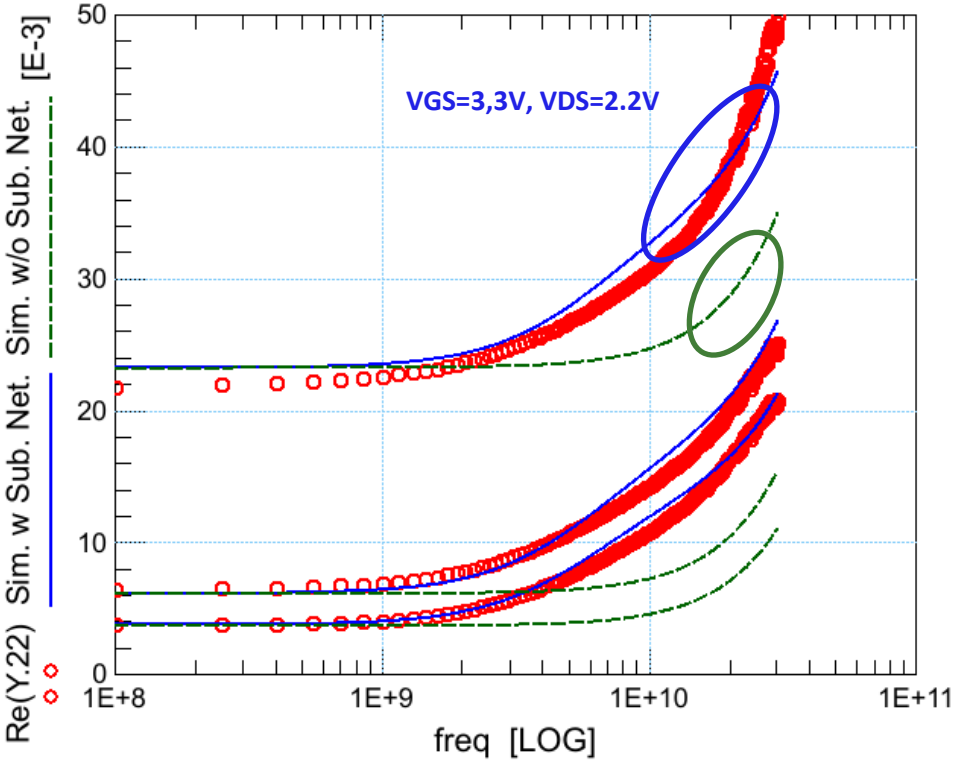



**Easier to determine with specific test structure e.g., Body connected to Port 1 and S/D to Port 2 and G grounded**

# SUBSTRATE MODELING

## Re(Y22) with and without substrate network

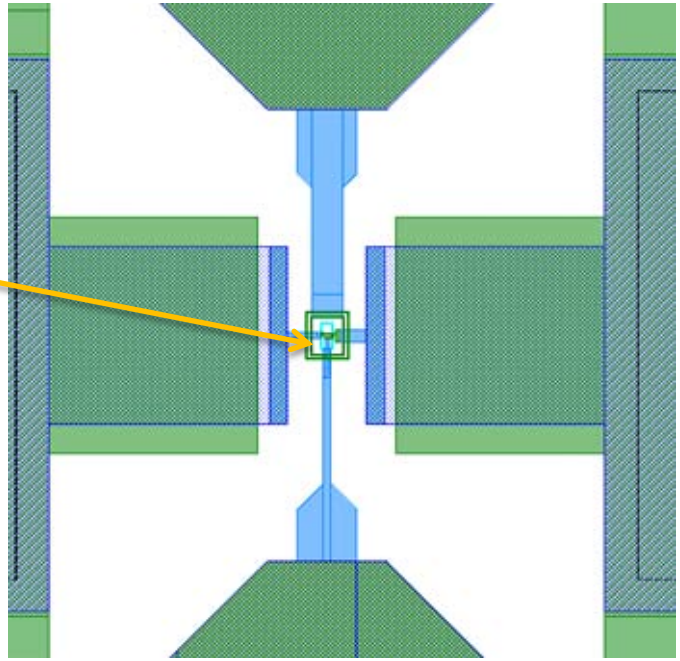
NMOS W=10 µm, L=0.35, **NF=64**



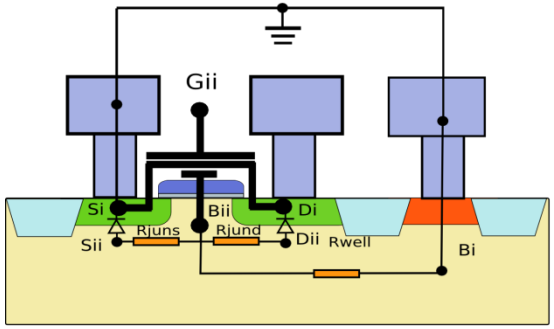
# SUBSTRATE MODELING

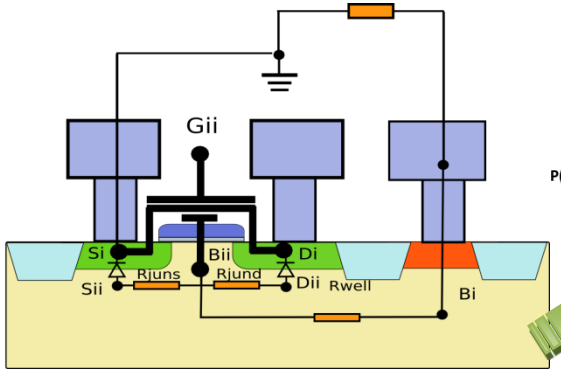
Test structure design matter again !

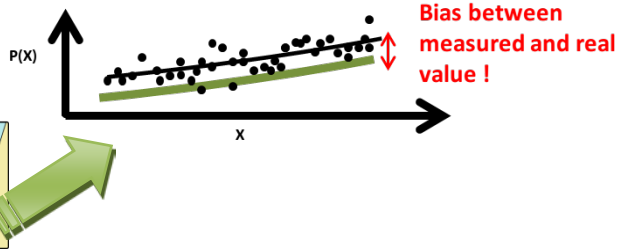
Substrate ring must be tied to Source here



**Otherwise substrate network impact is erroneous !**



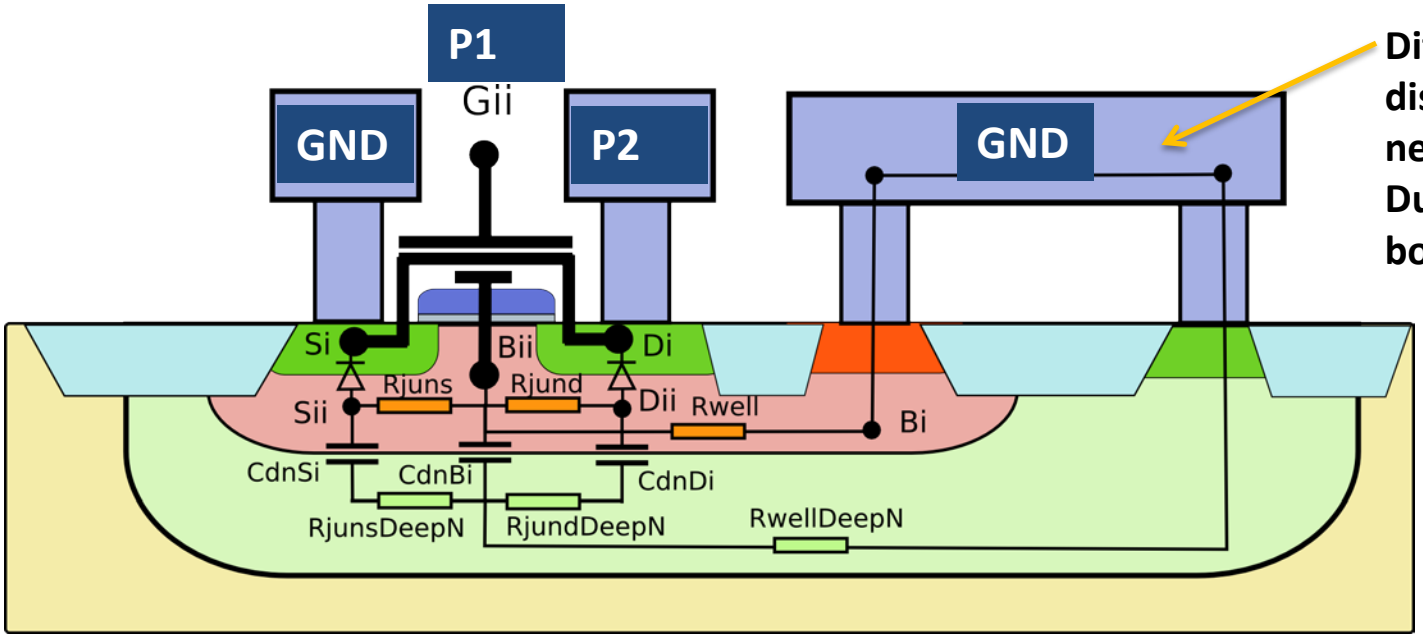



# SUBSTRATE MODELING

PMOS and Isolated NMOS need more elaborate networks

- In order to precisely determine each parasitic element, specific test structures are required
- Port access to Body, Deep Nwell and Psub are required
- W, L and NF variations are required




**Difficult to discriminate all network elements Due to body/Nwell short**

# CONCLUSION

- Understanding de-embedding methods is crucial to design RF test keys
- OPEN/SHORT dummies define DUT reference plane, i.e., Model reference plane
- Optimal RF test structures is a plus (small C, low R, low L)
- Consistent RF test structures is **must** to avoid measurement errors
- DC parasitic series resistance need to be modeled
- Baseband models are usually not accurate enough to be used as is in RF models (due to the lack of test structure quality and absence of Self Heating)
- Self Heating is of utmost importance for accurate RF models
- Substrate parasitic network require a lot of work (scaling equations, test structures design, specific test keys)


# THANK YOU