

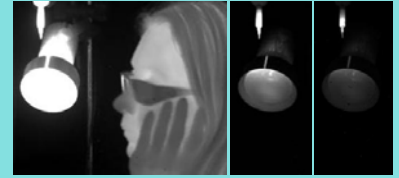
Extraction of Low Frequency Noise and Transistor Mismatch Parameters at Cryogenic Temperature for Design of CMOS Imagers in a 0.18 μm Mixed Analog-Digital Process

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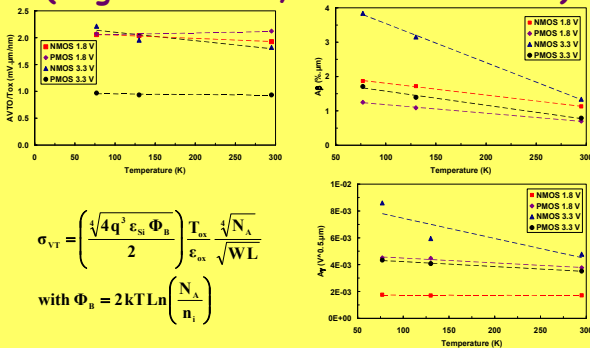
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Aim of this work

- Design of high performance (cooled) infrared image sensors for night vision
- Example of circuit: 320 x 256 pixels, pitch 25 μm, pixel-level 15 bits ADC, high dynamic range, NEDT < 2 mK
- CMOS process: 0.18 - 0.35 μm (1.8 V - 3.3 V MOSFETs) for digital & analog blocks
- Extraction of DC, AC, low frequency (LF) noise and mismatch parameters of MOSFET at low temperature (77 K - 200 K)



Transistor mismatch parameters (Pelgrom's model, Low VT MOSFETs)



$$\sigma_{VT} = \left(\frac{\sqrt{4q^3 \epsilon_{Si} \Phi_B}}{2} \right) \frac{T_{ox}}{\epsilon_{ox}} \sqrt{\frac{N_A}{WL}}$$

with $\Phi_B = 2kT \ln \left(\frac{N_A}{n_i} \right)$

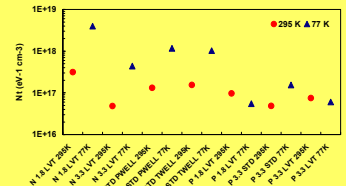
- $\Delta\beta$ and $\Delta\gamma$ systematically increase at LT
- $\Delta VT0$ either constant or increases due to enlargement of depletion layer \Rightarrow higher number of dopants

Low Frequency noise

Trap density extracted from LF noise measurements for different transistors

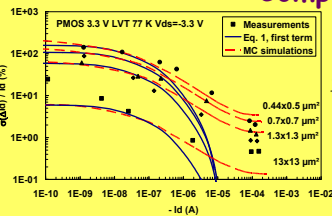
$$S_{V_{th}}(f) = \frac{kT q^2 \lambda N_t (E_f)}{WL C_{ox}^2} \frac{1}{f^2}$$

Low-Frequency Noise in a 0.18 μm Mixed-Mode CMOS Technology at Low Temperature, P. Martin, M. Cavellier and G. Ghibaudo, ICNF 2009, Pisa



- NMOSFET noisier at 77 K by a factor 7 ~ 13
- PMOSFET only noisier by a factor 0.6 ~ 3
- Increase of N_t at 77 K related to higher trap density as getting closer to the band edge at low temperature

Comparison between transistor matching and LF noise

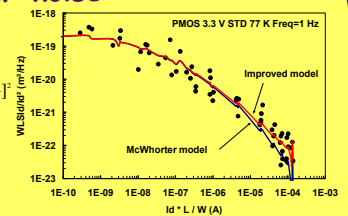


Monte-Carlo simulations with EKV2.6 parameters

$$\sigma^2(\Delta I_d) = \left(\frac{G_m}{I_d} \right)^2 \sigma^2(\Delta VT0) + \frac{\sigma^2(\Delta\beta)}{\beta^2} \iff \frac{S_{I_d}}{I_d^2} = \left(\frac{G_m}{I_d} \right)^2 S_{V_{th}}(f) [1 + \alpha \mu C_{ox} \frac{I_d}{G_m}]$$

Similar behavior of normalized fluctuations:

- Plateau in weak inversion
- Need for $\Delta\beta$ (matching) or $\Delta\mu$ (LF noise) contribution at high current



Conclusion

- Extraction of LF noise and mismatch parameters in a 0.18 μm mixed-mode CMOS process at low temperature
- Degradation of transistor matching at LT \Rightarrow strong implications for analog design of cooled CMOS imagers
- Similar behavior between the two fluctuations mechanisms: LF noise (traps at Si interface) and matching (dopants)

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