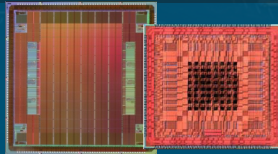
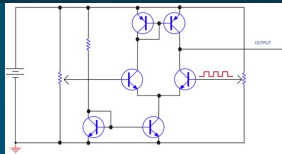




Xyce/ADMS and the Xyce Verilog-A Path Forward



PRESENTED BY

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What is Xyce/ADMS...

- XML templates that provide a code-generating “back-end” to ADMS

Can compile many standard models for built-in use

Verilog-A can be compiled as a shared-library plug-in

- Requires a special build of Xyce
- Many models need hand-modifications before they will compile

...there are limitations

- Requires `@(initial_model)` and `@(initial_instance)` to indicate blocks that should be executed only once
- Missing data types
- Limited support for expressions (such as `ddt`)
- Missing analog behaviors
- ...see the [Xyce/ADMS Users Guide](https://xyce.sandia.gov/) at <https://xyce.sandia.gov/>

Full support of modern compact models requires modification of the ADMS source code (C)

Xyce Verilog-A Path Forward



Develop an in-house Verilog-A compiler targeted at Xyce

- A known, reliable code base, owned by Sandia
- Specialized capabilities for multi-physics, including radiation effects

Leverage work from DAGADO

- a DAG-based differentiation library, written in Python, developed at Sandia

allows for...

Ease development of compact models

- Simplify the shared library approach taken by Xyce/ADMS

Xyce compatibility with modern PDKs

- Dynamic compilation (eventually)

Will release under GPL3 as part of Xyce

Timeline... to be announced, but work is commencing now.

Xyce Team Acknowledgements



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