

Qucs-S: A short overview on development status

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- What is Qucs-S?
 - Qucs-S provides a universal GUI for different circuit simulation kernels; Ngspice is recommended for usage with Qucs-S;
 - Qucs-S doesn't provide simulator and/or Verilog-A compiler by itself; It should be installed separately;
 - Qucs-S was forked from originally Qucs in 2016 and since 2017 has been developed independently;
 - Qucs-S is cross-platform software and could be run on Linux, Windows, and FreeBSD;
 - In February 2022 Qucs-S was ported to Qt5 and 0.0.23 release was prepared;
 - Compact modelling features implemented using Qucsator+ADMS;
 - Verilog-A synthesizer allows to export subcircuit into Verilog-A code;
- What simulators are supported by Qucs-S?
 - Ngspice <https://ngspice.org>
 - Xyce <https://xyce.sandia.gov/>
 - SpiceOpus <http://www.spiceopus.si/>
 - Qucsator <http://github.com/qucs/qucsator>
- Qucs-S is not related to the "modular Qucs" developed by main project!

Qucs-S main window

The screenshot displays the Qucs-S main window with the following components:

- Menu Bar:** File, Edit, Positioning, Insert, Project, Tools, Simulation, View, Help.
- Main Dock:** ne5532.sch
- Component Libraries:**
 - lumped components:** Resistor US (selected), Resistor, Capacitor, Inductor.
 - Libraries:** R Resistor, C Capacitor, L Inductor, K coupling, Ground, Subcircuit Port, Current Probe, Voltage Probe.
- Circuit Diagram:** A circuit schematic featuring an operational amplifier (OP1, NE5532) configured as an inverting amplifier. The input is connected to a voltage source (V2, 10 mV, 1 kHz) through a capacitor (C5, 0.33u) and a resistor (R1, 1k). The feedback network consists of a resistor (R2, 33k) and a capacitor (C2, 1000p) in parallel. The output is connected to a load resistor (R4, 10k) through a capacitor (C3, 0.33u). Other components include resistors R3 (200), R5 (10k), R6 (10k), and a DC voltage source (V1, 12V).
- Simulation Parameters:**
 - transient simulation:** TR1, Type=in, Start=0, Stop=5 ms.
 - ac simulation:** AC1, Type=log, Start=1 Hz, Stop=100 kHz, Points=101.
- Plots:**
 - Transient Plot:** Shows the output voltage (ngspice/trans.v(out)) and input voltage (ngspice/trans.v(in)) over time. The output is a sinusoidal wave with an amplitude of approximately 0.3 V.
 - AC Plot:** Shows the magnitude of the output voltage (ngspice/acK) versus frequency. The plot is a smooth curve peaking at approximately 30 dB around 1 kHz.

Ngspice no warnings: 593 / 382

Currently Qucs-S development roadmap

- The main task is to improve Qt5 compatibility. Qt5 porting is finished in 0.0.23;
 - Qt5 migration checklist https://github.com/ra3xdh/qucs_s/issues/72
- Prepare sources for porting to Qt6
 - QtScript is deprecated; It's need to get rid of QtScript dependency. It is essential for Verilog-A support;
https://github.com/ra3xdh/qucs_s/issues/77
 - Provide compatibility with Qt5.15
https://github.com/ra3xdh/qucs_s/issues/75
- The main simulator should be Ngspice; the second simulator is Xyce;
- Add support for new Xyce features like Verilog-A modules compilation on the fly; <https://xyce.sandia.gov/documentation-tutorials/xyce-adms-users-guide/>
- Add new component models to the libraries;
- Switch from Qucsator+ADMS to Xyce+ADMS for compact modelling;
- Unforking and merging as module for modular Qucs is not considered in the near future;

Where to find Qucs-S?

- Qucs-S repository on Github: https://github.com/ra3xdh/qucs_s/
- Website: <https://ra3xdh.github.io/>
- Release 0.0.23 page: https://github.com/ra3xdh/qucs_s/releases
- Windows 64-bit portable binaries could be downloaded from release page;
- Linux repositories (built with OBS):
<http://download.opensuse.org/repositories/home:/ra3xdh/>
- Issue tracker to report bugs:
https://github.com/ra3xdh/qucs_s/issues