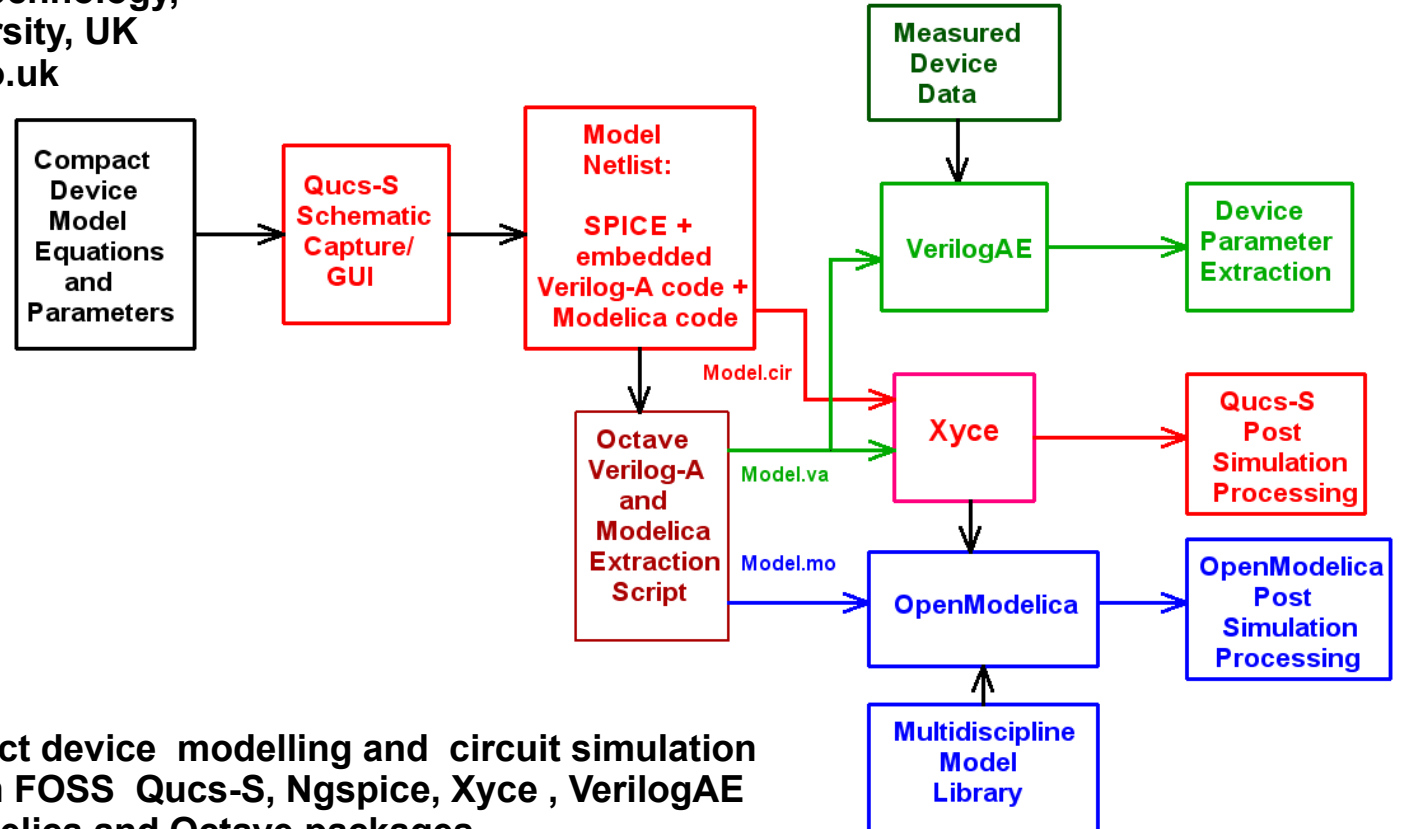


Advances in Qucs-S schematic capture for compact modelling and simulation

Mike Brinson
Centre for Communications Technology,
London Metropolitan University, UK
mbrin72043@yahoo.co.uk



Proposed compact device modelling and circuit simulation tool-set based on FOSS Qucs-S, Ngspice, Xyce, VerilogAE, OpenModelica and Octave packages



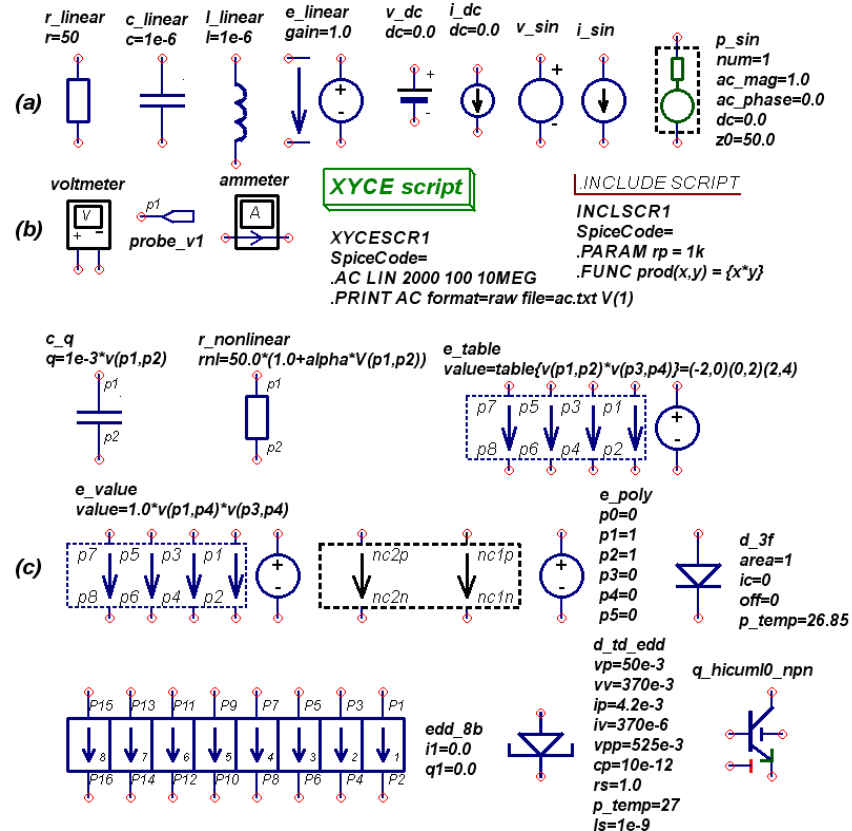
Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/Xyce Modular Libraries: New schematic symbols and models

Test library for Qucs-S/Xyce

Points to note:

1. Component and device models in this library are not hard wired into Qucs-S program code;
2. Xyce SPICE dialect becomes the Qucs-S/Xyce netlist format;
3. The functionality of each schematic symbol is set by Xyce SPICE code.



THE CONTENT OF EACH LIBRARY IS DEFINED BY USERS

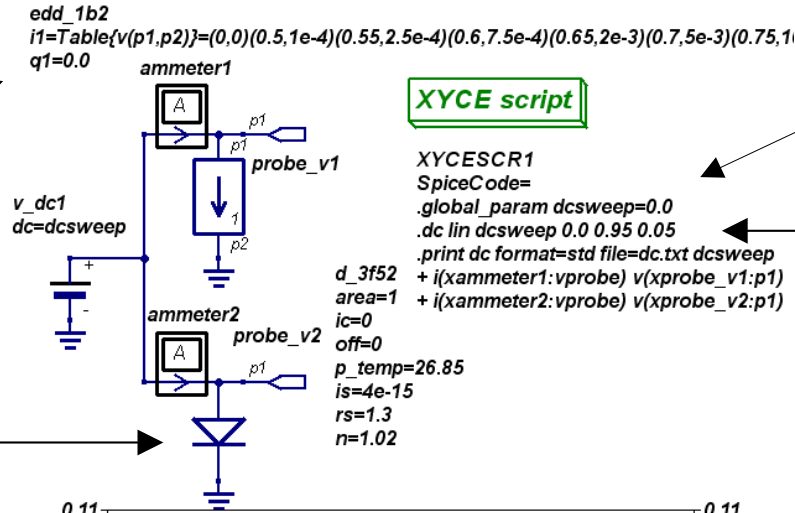


Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/Xyce Modular Libraries: Schematic symbols and global variables; 1

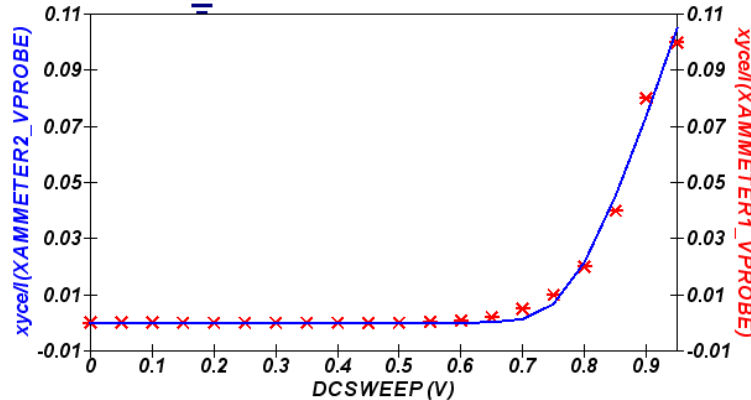
Extended EDD diode model:
Diode I_d/V_d characteristic constructed from a numeric Table passed as a subcircuit parameter, allowing the diode model current to be set by the voltage across EDD internal nodes p1 and p2.

SPICE diode model



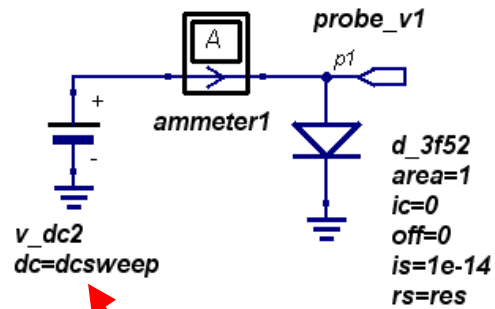
Global parameter dcsweep is Equivalent to a variable that can be changed during simulation.

dcsweep value changed by .dc



Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/Xyce Modular Libraries: Schematic symbols and global variables; 2



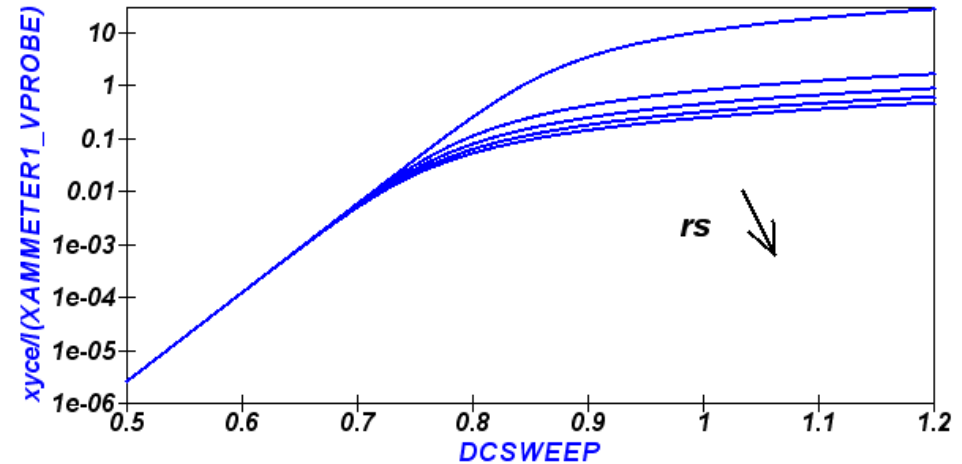
.global_param

1. dcsweep
2. res

XYCE script

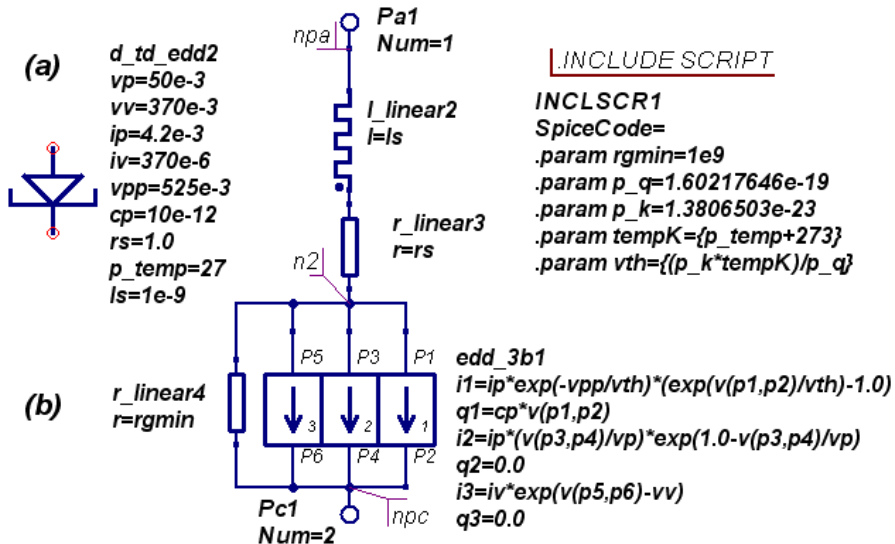
```
XYCESCR1  
SpiceCode=  
.global_param dcsweep = 0.0  
.global_param res=1e-3  
.dc lin dcsweep 0.5 1.2 0.02  
.step lin res 0.01 1.0 0.2  
.print dc format=std file=dc.txt dcsweep  
+ i(xammeter1:vprobe) v(xprobe_v1:p1)
```

**Xyce .dc and .step commands
set dcsweep and res values**



Advances in Qucs-S schematic capture for compact modelling and simulation

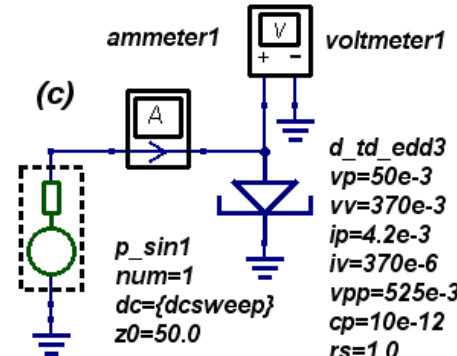
Qucs-S/XYce Modular Libraries: Schematic symbols and global variables; 3



INCLUDE SCRIPT

```

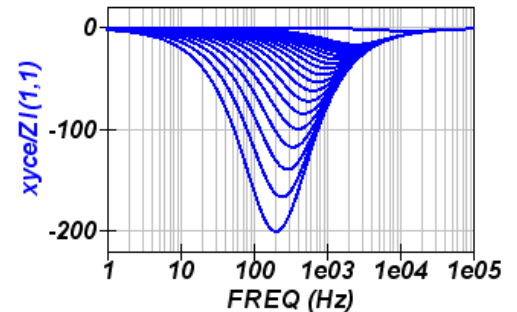
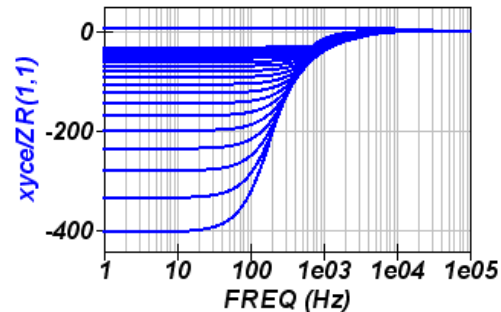
INCLSCR1
SpiceCode=
.param rgmin=1e9
.param p_q=1.60217646e-19
.param p_k=1.3806503e-23
.param tempK={p_temp+273}
.param vth={{(p_k*tempK)/p_q}
    
```



XYCE script

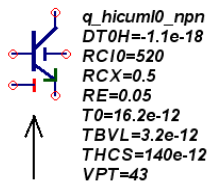
```

XYCESCR1
SpiceCode=
.global_param dcsweep=0.0
.ac dec 20 1 1e5
.step dcsweep 0.1 0.3 0.01
.lin format=touchstone sparcalc=1 lintype=z
.print ac format=std file=sparam.txt dcsweep
+ zr(1,1) zi(1,1) zm(1,1) zp(1,1)
    
```



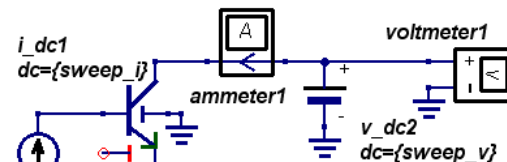
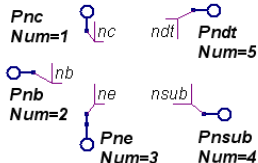
Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/Xyce Modular Libraries: CMC Verilog-A standardized device models



INCLUDE SCRIPT

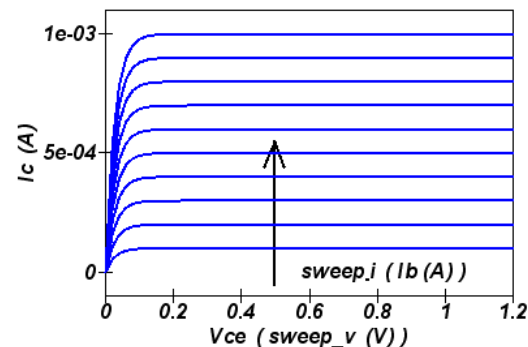
```
INCLSCR1
SpiceCode=
rnc nc 0 1e9
rnb nb 0 1e9
rne ne 0 1e9
rnsb nsub 0 1e9
rndt ndt 0 1e9
*
Q1 nc nb ne nsub ndt HICUML0_npn
.MODEL HICUML0_npn npn (Level=230
+AF={AF} AHC={AHC} AHQ={AHQ} AJE={AJE} AJEDC={AJEDC}
+ALCES={ALCES} ALEAV={ALEAV} ALIQFH={ALIQFH} ALIT={ALIT}
+ALKAV={ALKAV} ALQF={ALQF} ALT0={ALT0} ALVS={ALVS}
+AVER={AVER} CBCPAR={CBCPAR} CBEPAR={CBEPAR} CJC10={CJC10}
+CJCX0={CJCX0} CJE0={CJE0} CJS0={CJS0} CTH={CTH} DT0H={DT0H}
+DVGBE={DVGBE} EAVL={EAVL} F1VG={F1VG} F2VG={F2VG} FBC={FBC}
+FGEO={FGEO} FIQF={FIQF} FLNQS={FLNQS} FLSH={FLSH} GTE={GTE}
+IBCS={IBCS} IBES={IBES} IQF={IQF} IQFH={IQFH} IQR={IQR} IRES={IRES}
+IS={IS} ISCS={ISCS} IT_MOD={IT_MOD} ITSS={ITSS} KAVL={KAVL}
+KF={KF} KIQFH={KIQFH} KT0={KT0} MBC={MBC} MBE={MBE} MCF={MCF}
+MCR={MCR} MRE={MRE} MSC={MSC} MSF={MSF} RBI0={RBI0} RBX={RBX}
+RC10={RC10} RCX={RCX} RE={RE} RTH={RTH} T0={T0} TBVL={TBVL}
+TEF0={TEF0} TEF_TEMP={TEF_TEMP} TFH={TFH} THCS={THCS}
+TNOM={TNOM} TR={TR} TYPE={TYPE} VCES={VCES} VDCI={VDCI}
+VDCX={VDCX} VDE={VDE} VDEDC={VDEDC} VDS={VDS} VEF={VEF}
+VER={VER} VGB={VGB} VGC={VGC} VGE={VGE} VGS={VGS} VLIM={VLIM}
+VPT={VPT} VPTCI={VPTCI} VPTCX={VPTCX} VPTS={VPTS}
+VR0C={VR0C} VR0E={VR0E} ZCI={ZCI} ZCX={ZCX} ZE={ZE} ZEDC={ZEDC}
+ZETABET={ZETABET} ZETACI={ZETACI} ZETACT={ZETACI}
+ZETAIQF={ZETAIQF} ZETARBI={ZETARBI} ZETARBX={ZETARBX}
+ZETARCX={ZETARCX} ZETARE={ZETARE}
+ZETARTH={ZETARTH} ZETAVER={ZETAVER} ZETA VGBE={ZETA VGBE} )
```



XYCE script

```
q_hicuml0_npn1
DT0H=-1.1e-18
RC10=520
RCX=0.5
RE=0.05
T0=16.2e-12
TBVL=3.2e-12
THCS=140e-12
VPT=43

XYCESCR1
SpiceCode=
.global_param sweep_v=0.0
.global_param sweep_i=0.0
.dc lin sweep_v 0 1.2 0.02
.step lin sweep_i 1u 10u 1u
.print dc format=std file=dc.txt
+ sweep_v i(xammeter1:vprobe)
+v(xvoltmeter1:pton)
```



**Xyce Verilog-A
HICUML0 BJT model
with default parameters -
except where changed
in symbol parameter list**



Advances in Qucs-S schematic for capture compact modelling and simulation

Qucs-S/Xyce Modular Libraries: Tunnel diode netlist code

**Xyce model
SPICE
subcircuits**

* C:/Users/mbrinl/qucs-s/mixdes2021/prj/TDexample.sch

```
.SUBCKT Xyce_voltmeter gnd p1 p2
rp p1 p2 1e9
gout 0 pton p1 p2 1.0
rout pton 0 1.0
.ENDS
```

```
.SUBCKT Xyce_ammeter gnd p1 p2
vprobe p1 p2 dc 0.0
.ENDS
```

```
.SUBCKT Xyce_p.sin gnd p1 p2 num=1 ac.mag=1.0 ac.phase=0.0
+ dc=0.0 z0=50.0 tran_vo=0.0 tran_va=1.0 tran.frequency=1000.0
+ tran.phase=0.0
port p1 p2 dc {dc} port={num} z0={z0} ac {ac.mag} {ac.phase}
+ sin {tran.vo} {tran.va} {tran.frequency} {tran.phase}
.ENDS
```

```
.SUBCKT Xyce_r.linear gnd p1 p2 r=50 m=1 tc1=0.0 tc2=0.0 tce=0.0
+ p.temp=26.58 dtemp=0.0
r.linear p1 p2 {r} m={m} tc1={tc1} tc2={tc2} tce={tce}
+ temp={p.temp} dtemp={dtemp}
.ENDS
```

```
.SUBCKT Xyce_l.linear gnd p1 p2 l=1e-6 m=1.0 tc1=0.0 tc2=0.0
+ p.emp=26.58
l.linear p1 p2 {l} m={m} tc1={tc1} tc2={tc2} temp={p.temp}
.ENDS
```

```
.SUBCKT Xyce_edd_3b gnd p1 p2 p3 p4 p5 p6 i1=0.0 q1=0.0
+ i2=0.0 q2=0.0 i3=0.0 q3=0.0
bb1 p1 p2 i=i1
cb1 p1 p2 q=q1
*
```

```
bb2 p3 p4 i=i2
cb2 p3 p4 q=q2
*
```

```
bb3 p5 p6 i=i3
cb3 p5 p6 q=q3
.ENDS
```

```
.SUBCKT Xyce_d.td.edd gnd npa npc vp=50e-3 vv=370e-3 ip=4.2e-3
+ iv=370e-6 vpp=525e-3 cp=10e-12 rs=1.0 p.temp=27 ls=1e-9
.param rgmin=1e9
.param p.q=1.60217646e-19
.param p.k=1.3806503e-23
.param tempK={p.temp+273}
.param vth={{p.k*tempK}/p.q}
Xr.linear1 0 .net0 n2 Xyce_r.linear r={RS} m=1 tc1=0.0
+ tc2=0.0 tce=0.0 p.temp=26.58 dtemp=0.0
Xl.linear1 0 npa .net0 Xyce_l.linear l={LS} m=1.0 tc1=0.0
+ tc2=0.0 p.temp=26.58
Xr.linear2 0 n2 npc Xyce_r.linear r={RGMIN} m=1 tc1=0.0
+ tc2=0.0 tce=0.0 p.temp=26.58 dtemp=0.0
Xedd_3b1 0 n2 npc n2 npc n2 Xyce_edd_3b
+ i1={IP*EXP(-VPP/VTH)}(EXP(V(P1,P2)/VTH)-1.0)}
+ q1={CP*V(P1,P2)}
+ i2={IP*(V(P3,P4)/VP)*EXP(1.0-V(P3,P4)/VP)}
+ q2=0.0
+ i3={IV*EXP(V(P5,P6)-VV)}
+ q3=0.0
.ENDS
```

```
Xvoltmeter1 0 .net0 Xyce_voltmeter
Xammeter1 0 .net1 .net0 Xyce_ammeter{-}
Xp.sin1 0 .net1 0 Xyce_p.sin num=1 ac.mag=1.0
+ ac.phase=0.0 dc={DCSWEEP} z0=50.0 tran_vo=0.0 tran_va=1.0
+ tran.frequency=1000.0 tran.phase=0.0
Xd.td.edd3 0 .net0 0 Xyce_d.td.edd vp=50E-3
+ vv=370E-3 ip=4.2E-3 iv=370E-6 vpp=525E-3
+ cp=10E-12 rs=1.0 p.emp=27 ls=1E-9
```

```
.global_param dcsweep=0.0
.ac dec 20 1 1e5
.step dcsweep 0.1 0.3 0.01
.lin format=touchstone sparcalc=1 lintype=z
.print ac format=std file=sparam.txt dcsweep
+ zr(1,1) zi(1,1) zm(1,1) zp(1,1)
.END
```

Device count summary	
B level 1	3
C level 1	3
G level 1	1
L level 1	1
R level 1	4
V level 1	2

Total Devices	14

**Subcircuit
X call
statements**

**Xyce control
and data output
statements**



Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/Xyce/Modelica: Multi-HDL schematic capture and code generation; 1



Symbol and SPICE component type

Multiple additional information lines: these allow long strings of SPICE and other HDL data to be passed to Xyce netlists to form a component specification

Qucs-S component template: built into C++ GUI code

```

R2
R=
R_Line 2=
R_Line 3=
R_Line 4=
R_Line 5=
    
```

Subcircuit: internal multi-HDL code (Xyce SPICE and Verilog-A)

```

INCLUDE SCRIPT
INCLSCR1
SpiceCode=
*va`include "disciplines.vams"
*va`include "constants.vams"
*va module NGenSub1 n1, n2;
*va inout n1, n2;
*va electrical n1, n2, n3;
*va parameter real R=1.5;
*va parameter real C=100e-6;
*va parameter real L=100e-9;
*va analog begin
L1
L={L}
L_Line 2=*va V(n1, n2) <+ ddt(L*1(n1,n2));
C1
C={C}
C_Line 2=*va I(n2, n3) <+ ddt(C*V(n2,n3));
R1
R={R}
R_Line 2=*va I(n3) <+ V(n3)/R;
P1 Num=1
P2 Num=2
    
```

SPICE netlist generated by Qucs-S GUI for Xyce simulation

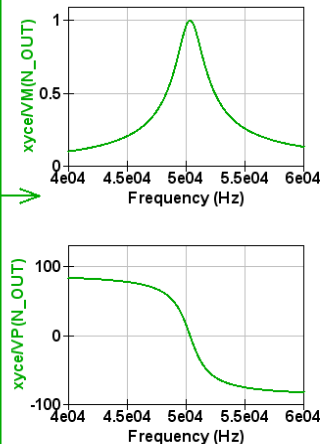
Xyce SPICE netlist with Verilog-A embedded HDL code

```

* Qucs 0.0.22 C:/Users/mbrinl/qucs-s/L/METResSemSlides_prij/testL.CRXYce.sch
.SUBCKT NGenSub1 _net0 n3 R=1 L=100n C=0.1u
*va`include "disciplines.vams"
*va`include "constants.vams"
*va module NGenSub1 n1, n2;
*va inout n1, n2;
*va electrical n1, n2, n3;
*va parameter real R=1.5;
*va parameter real C=100e-6;
*va parameter real L=100e-9;
*va analog begin
C1 n2 n3 {C}
*va I(n2, n3) <+ ddt(C*V(n2,n3));
R1 0 n3 {R}
*va I(n3) <+ V(n3)/R;
L1 n1 n2 {L}
*va V(n1, n2) <+ ddt(L*1(n1,n2));
.ENDS
V1 n_in 0 dc 0 ac 1
XLCR1 n_in n_out NGenSub1 R=1.5 L=100U C=100N
.AC lin 1000 4e4 6e4
.PRINT AC format=std file=ac.txt
+ V(n_in) V(n_out) Vm(n_in) Vm(n_out)
+ VP(n_in) VP(n_out)
*va end
*va endmodule
.END
    
```

Xyce

Qucs-S post-simulation data visualization



Note: lines with a * in column 1 are treated by Xyce as documentation COMMENTS

Xyce subcircuit

```

XYCESCR1
SpiceCode=
.AC lin 1000 4e4 6e4
.PRINT AC format=std file=ac.txt
+ V(n_in) V(n_out) Vm(n_in) Vm(n_out)
+ VP(n_in) VP(n_out)
*va end
*va endmodule
.END
    
```

Qucs-S schematic drawing

```

V1
V=dc 0 ac 1
LCR1
File=NGenSub1.sch
R=1.5
L=100u
C=100n
    
```


Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/Xyce/Modelica: Multi-HDL schematic capture and code generation; 2

```
* Qucs 0.0.22 C:/Users/mbrinl/qucs-s/LMETResSemSlides_prj/testLCRXyce.sch
.SUBCKT NGenSub1 _net0 n3 R=1 L=100n C=0.1u
```

```
*va `include "disciplines.vams"
*va `include "constants.vams"
*va module NGenSub1 n1, n2;
*va inout n1, n2;
*va electrical n1, n2, n3;
*va parameter real R=1.5;
*va parameter real C=100e-6;
*va parameter real L=100e-9;
*va analog begin
```

```
C1 n2 n3 {C}
*va I(n2, n3) <+ ddt(C*V(n2,n3));
R1 0 n3 {R}
*va I(n3) <+ V(n3)/R;
L1 n1 n2 {L}
*va V(n1, n2) <+ ddt(L*I(n1,n2));
```

```
.ENDS
V1 n_in 0 dc 0 ac 1
XLCR1 n_in n_out NGenSub1 R=1.5 L=100U C=100N
```

```
.AC lin 1000 4e4 6e4
.PRINT AC format=std file=ac.txt
+ V(n_in) V(n_out) Vm(n_in) Vm(n_out)
+ VP(n_in) VP(n_out)
*va end
*va endmodule
.END
```

```
function ExtractVa(ModuleName);
% An Octave function to extract a Verilog-A module from a
% Xyce/Ngspice netlist.
% (C) 2021 Mike Brinson: Published under GNU General
% Public License V2 or later.
% ===== Initialize variables =====
netlistName = strcat( ModuleName, ".cir");
VaModuleName= strcat( ModuleName, ".va");
fidread=fopen(netlistName,"r"); fidwrite=fopen(VaModuleName,"w");
% ===== Extract Verilog-A module =====
line=fgetl(fidread);
while 1
if strfind(line,"*va")
line=[line(4:end)];
fprintf(fidwrite,"%s\n",line);
endif
line=fgetl(fidread);
if feof(fidread)
% if ischar(line) fprintf(fidwrite,"%s\n",line); endif
break
endif
endwhile
fclose(fidread); fclose(fidwrite);
display("Verilog-A module extraction finished.\n");
return
```

```
`include "disciplines.vams"
`include "constants.vams"
module NGenSub1 n1, n2;
inout n1, n2;
electrical n1, n2, n3;
parameter real R=1.5;
parameter real C=100e-6;
parameter real L=100e-9;
analog begin
I(n2, n3) <+ ddt(C*V(n2,n3));
I(n3) <+ V(n3)/R;
V(n1, n2) <+ ddt(L*I(n1,n2));
end
endmodule
```

NGenSub1.cir

Octave Verilog-A
module extraction
function

NGenSub1.va



Advances in Qucs-S schematic capture for compact modelling and simulation

Qucs-S/XYce/Modelica: Multi-HDL schematic capture and code generation; 3

The tunnel diode model revisited

The image shows a Qucs-S schematic capture of a tunnel diode model. The schematic includes a DC voltage source V1, a tunnel diode model TunnelDiode1, and a probe PriTD. The tunnel diode model is defined by parameters: Vp=50e-3, Ip=4.2e-3, Vv=370e-3, Iv=370e-6, Vpp=525e-3, Cp=20e-12, Rs=1.0, Ls=5e-9, and TempC=27. A graph shows the current through the tunnel diode (xyce[VPRITD]) versus the DC voltage V1 (DC V), showing a characteristic tunneling current peak.

XYCE script

```

XYCESCR1
SpiceCode=
.DC LIN V1 0.01 525e-3 0.001
.PRINT DC format=std file=dc.txt
+ V(nTD) I(VPRITD)
*va end
*va endmodule
    
```

INCLUDE SCRIPT

```

INCLUDE SCRIPT
INCLSCR1
SpiceCode=
*va include "disciplines.vams"
*va include "constants.vams"
*va module TunnelDiode1(nP1, nP2);
*va inout nP1, nP2;
*va electrical nP1, nP2, nP3, nP4;
*va parameter real Vp=50e-3;
*va parameter real Ip=4.2e-3;
*va parameter real Vv=370e-3;
*va parameter real Iv=370e-6;
*va parameter real Vpp=525e-3;
*va parameter real Cp=20e-12;
*va parameter real Rs=1.0;
*va parameter real Ls=5e-9;
*va parameter real TempC=27;
*va real I1, I2, I3, TempK, VTH;
analog begin
TempK = TempC+273;
VTH = P_K*TempK/P_Q;
I(nP3, nP4) <+ V(nP3, nP4)/Rs;
V(nP1, nP3) <+ ddt(Ls*I(nP1, nP3));
I1= Ip*exp(-Vpp/VTH)*(exp(V(nP4, nP2)/VTH)-1.0);
I2= Ip*(V(nP4, nP2)/Vp)*exp(1-V(nP4, nP2)/Vp);
I3= Iv*exp(V(nP4, nP2)-Vv);
I(nP4, nP2) <+ ddt(Cp*V(nP4, nP2));
I(nP4, nP2) <+ I1+I2+I3;
end
endmodule TunnelDiode1.va
    
```

Equation

```

Eqn1
P_K=1.3806503E-23
P_Q= 1.60217682e-19
TempK= TempC+273.0
VTH=P_K*TempK/P_Q
    
```

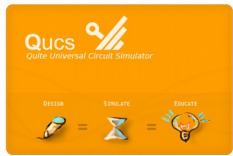
Model Equations

```

B1
I={ Ip*exp(-Vpp/VTH)*(exp(V(nP4, nP2)/VTH)-1.0) }
Line_2=va I1 = Ip*exp(-Vpp/VTH)*(exp(V(nP4, nP2)/VTH)-1.0);
B2
I={ Ip*(V(nP4, nP2)/Vp)*exp(1-V(nP4, nP2)/Vp) }
Line_2=va I2= Ip*(V(nP4, nP2)/Vp)*exp(1-V(nP4, nP2)/Vp);
B3
I={ Iv*exp(V(nP4, nP2)-Vv) }
Line_2=va I3= Iv*exp(V(nP4, nP2)-Vv);
B4
I={ V(n1)+V(n2)+V(n3) }
Line_2=va I(nP4, nP2) <+ I1+I2+I3;
C1
C={ Cp*V(nP4, nP2) }
C_Line_2=va I(nP4, nP2) <+ ddt(Cp*V(nP4, nP2));
R1
R={ Rs }
R_Line_2=va I(nP3, nP4) <+ V(nP3, nP4)/Rs;
    
```

Simulation Results

Time (s)	Current I (A)
0.0	0.0000
0.05	0.0040
0.1	0.0020
0.2	0.0005
0.3	0.0002
0.4	0.0001
0.5	0.0000



Tunnel Diode compact model example
 Mike Brinson and Daniel Tomaszewski
 Date: 30 1 2022 Revision: 1