PALMA DE MALLORCA
7-10 SEPTEMBER
ESSERC 2026

UNIVERSITAT ROVIRA i VIRGILI

UIB Universitat de les Illes Balears

Open-Source RFIC Design: Case Studies Using IIC-OSIC-TOOLS

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JKU

Johannes Kepler University, Linz, Austria

IEEE SSCS Electron Devices Society CAS

Acknowledgment

These slides present work from (alphabetical, incl. GitHub handles):

- **Simon Dorrer** (simi1505)
- **Patrick Fath** (p-fath)
- **Jonathan Hager** (jona250210)
- **Matthias Jung** (myzinsky)
- **David Kellerer-Pirklbauer** (davkel99)
- **Michael Köfinger** (michaelk99)
- **Martin Köhler** (martinjankoehler)
- **Clyde Laforge** (scafir)
- **Harald Pretl** (hpretl)
- **Ghaith Al Sabagh** (engghaith)
- **Georg Zachl** (mrhighvoltage)

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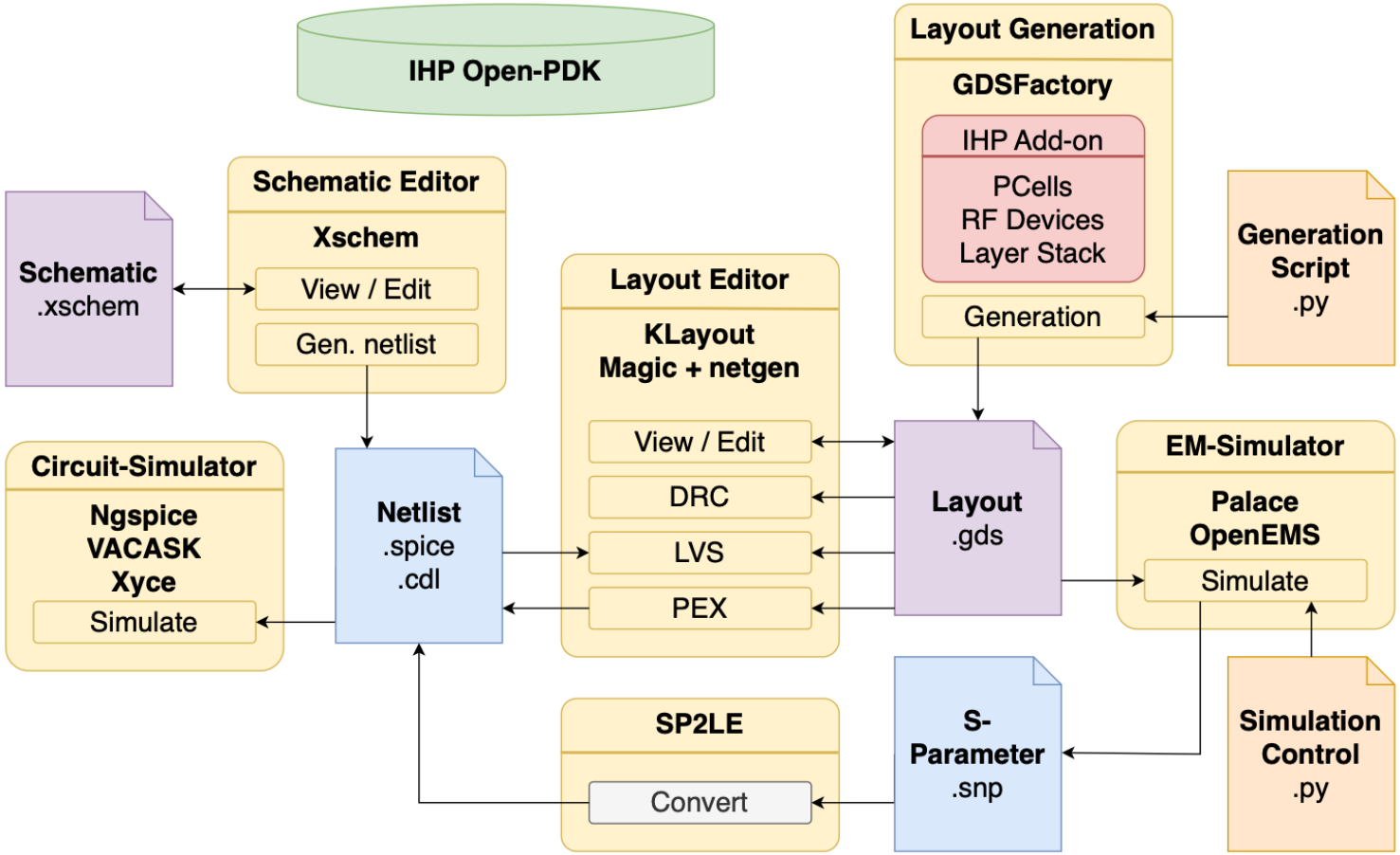
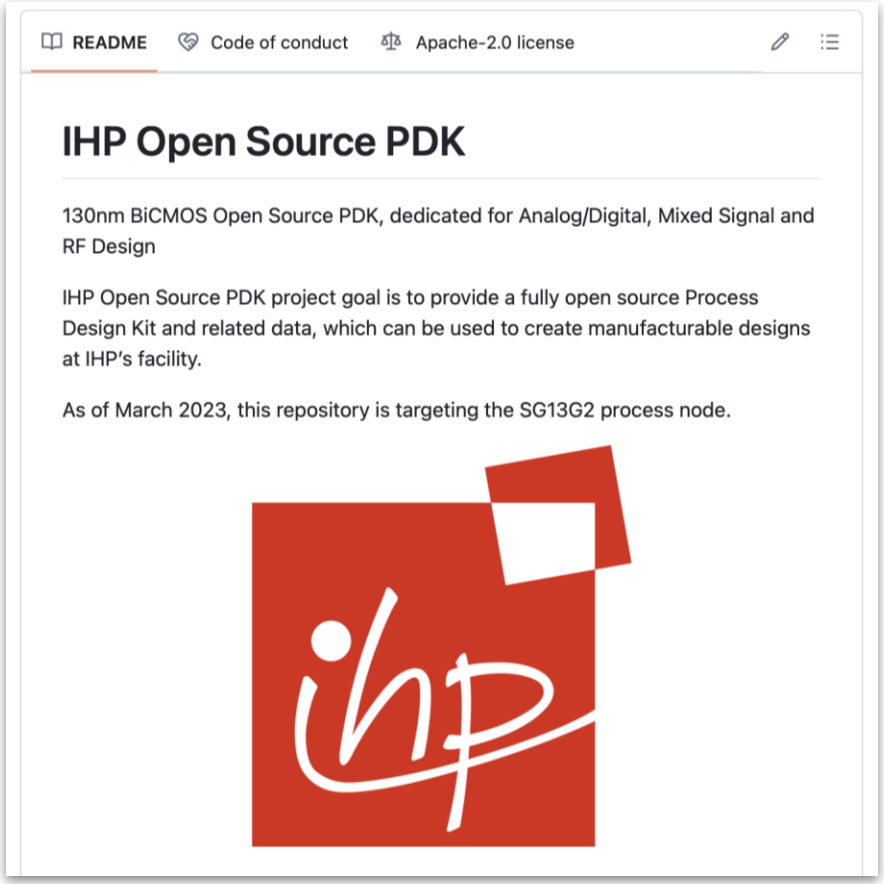
Content

- **The common thread - *IIC-OSIC-TOOLS***
- Mixed-Signal SoC - *TinyWhisper*
- 44-GHz RF Detector
- 150-GHz FMCW Radar - *mWATTBAT*
- 160-GHz mm-wave six-port - *SPARX*
- Conclusion

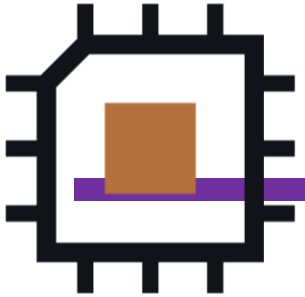
First, we need some tools ...



And some PDKs …



- https://github.com/IHP-GmbH/IHP-Open-PDK
- **130-nm SiGe:C BiCMOS**
- Core/IO MOSFETs (triple-well)
- 7x metals (2x thick)
- Poly resistors
- MIM/MOM capacitors
- **High-speed HBT (f_T > 300 GHz)**
- Additional variant:
  CMOS5L (No HBT, 5x metals, no MIM)



IIC-OSIC-TOOLS

OPEN-SOURCE IC DESIGN · JKU LINZ

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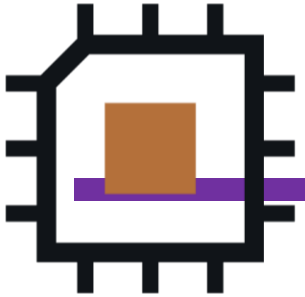
- Container-based **integrated** solution (based on Docker/Podman) available at https://www.osic.tools
  - Supporting **amd64/x86_64** and **arm64/aarch64** (runs on cloud, servers, desktops, Raspberry Pi)
  - Used globally for IC education and IC making
  - **930+ GitHub stars, 150+ forks, 100k+ downloads on Docker Hub**
- **Regular releases** since 2022.05, 39 images released so far, all still available
- Regression suite (growing) for QA
- Support via GitHub issues, pull requests (➔ **you** can ask for features)
- Many tools & PDKs preinstalled! **How many?**

THIS MANY!

abc Logic synthesis & formal verifiation
amaranth Python-based HDL toolchain
cace Circuit automatic characterization
charlib Standard cell characterization
ciel Open-source PDK version manager
cocotb Python-based HDL testbench library
covered Verilog code coverage
cvc Circuit validity checker (ERC)
edalize Python abstraction for EDA tools
fault Design-for-testing (DFT) solution
fusesoc SoC package manager & build tools
gaw3-xschem Waveform viewer for xschem
gds2palace Setup tools for palace EM sim
gds3d 3D viewer for GDS files
gdsfactory Python lib for GDS generation
gdsfill Dummy metal fill insertion
gdspy Python GDS file manipulation
gf180mcu PDK 180nm CMOS
ghdl VHDL simulator
ghdl-yosys-plugin VHDL plugin for yosys
gmsh 3D finite element mesh generator
gtkwave Digital waveform viewer
hdl21 Analog hardware description library
ihp-sg13g2 PDK 130nm SiGe:C BiCMOS
ihp-sg13cmos5l PDK 130nm CMOS (5 ML)
irsim Switch-level digital simulator
iverilog Verilog simulator
kactus2 IP-XACT graphical editor
kepler-formal LEC
klayout GDS/OASIS layout viewer & editor
klayout-pex Parasitic extraction for klayout
lctime CMOS cell characterization
libman Design library manager
librelane RTL-to-GDS flow
magic Layout editor with DRC & PEX
najaeda Post-synthesis EDA algorithms
netgen Netlist comparison (LVS)
ngspice analog/mixed-signal simulator
ngspyce Python bindings for ngspice
nvc VHDL simulator & compiler
open_pdks PDK setup scripts
openems EM field solver (EC-FDTD)
openram SRAM compiler
openroad RTL-to-GDS engine
opensta Static timing analyzer
openvaf Verilog-A compiler
osic-multitool Scripts & docs
padring Padring generation tool
palace 3D FEM EM solver
pulp-tools bender, verible, sv2v
pygmid Python gm/Id starter kit
pyopus Analog circuit optimization
pyrtl Pythonic RTL design library
pyspice Interface to ngspice/xyce
pyuvm Python UVM using cocotb
pyverilog Python Verilog toolkit
qflow RTL2GDS tools
qucs-s RF sim environment
rggen Register code generation
risc-v-toolchain GNU compiler
riscv-pk RISC-V kernel & boot
schemdraw Python schematics
scikit-rf RF and microwave toolkit
siliconcompiler HW build system
sky130 PDK 130nm CMOS
slang SV parser & translator
slang-yosys-plugin SV plugin
snp2le S-param to netlist conv
spicebind ngspice/HDL cosim
spicelib SPICE sim library
spike RISC-V ISA simulator
spyci ngspice/xyce data read
surelog SV/UHDM compiler
surfer Waveform viewer
svck SV linter (verible-based)
vacask Verilog-A simulator
verilator Verilog simulator
verible SV parser
veryl Modern HDL (SV-based)
vlsirtools Interchange formats
xcircuit Schematic editor
xschem Schematic editor
xyce Fast SPICE simulator
yosys SV/VHDL synthesis



IIC-OSIC-TOOLS

OPEN-SOURCE IC DESIGN · JKU LINZ

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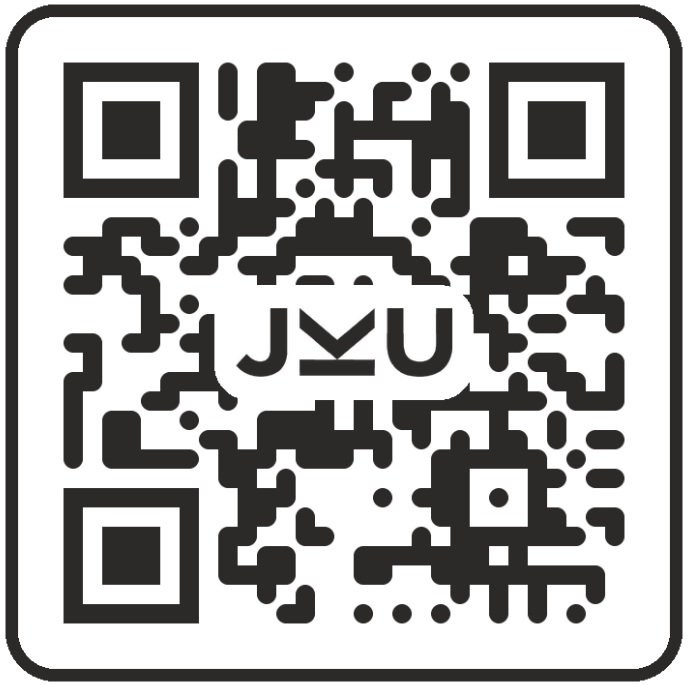
Want to install it? SCAN!



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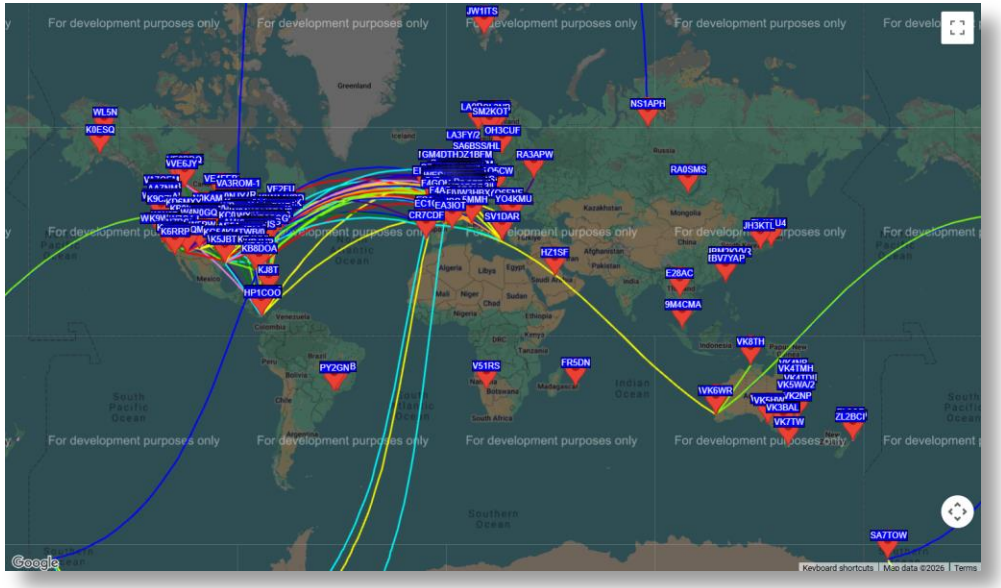
Mixed-Signal SoC for Ham Radio

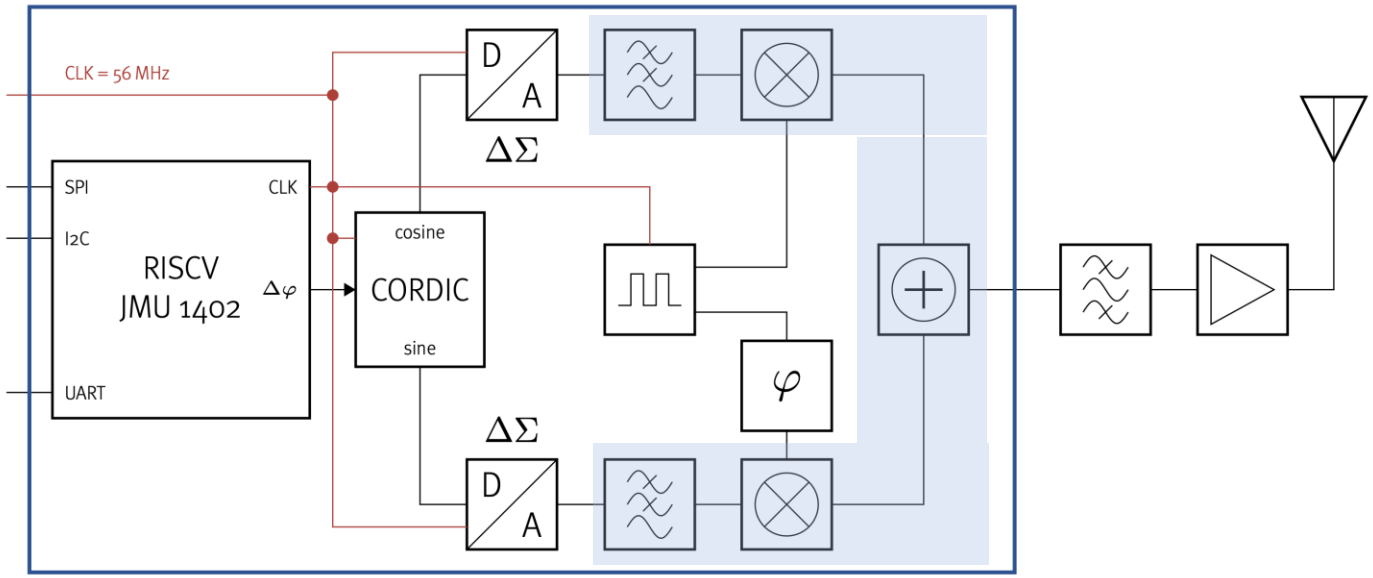
- Cooperation by JMU Würzburg & JKU Linz
- **Weak Signal Propagation Reporter (WSPR)**
  - Popular digital mode in ham radio
  - Propagation studies @ 80 m to 10 m bands
  - Transmit short messages (callsign, location, TX power)
  - Global receivers report to central database: https://www.wsprnet.org/drupal/wsprnet/map
  - 4-FSK modulation (Δf = 1.46 Hz, T = 0.683 s)
  - SNR = −31 dB (in 2500 Hz BW)



Band	RF Frequency	LO Frequency	IF (CORDIC)
80m	3.568600 MHz	3.5 MHz	68.600 kHz
40m	7.038600 MHz	7 MHz	38.600 kHz
20m	14.095600 MHz	14 MHz	95.600 kHz
10m	28.124600 MHz	28 MHz	124.600 kHz

Architecture: Maximize Digital

- **Target: digital and flexible, minimum analog**
- MODEM (coding, framing, symbol mapping) in FW (C-code) ➔ **CPU**
- No PLL ➔ LO generation via XO frequency division and **CORDIC**
  - XTAL offset trim also by CORDIC
- FSK modulation via passive **IQ-mixer** in voltage mode, dig-IQ generation by CORDIC
- D/A conversion using **1-bit 2nd-order DS-modulator** and **3rd-order lowpass**
- External BP filter and power-amp



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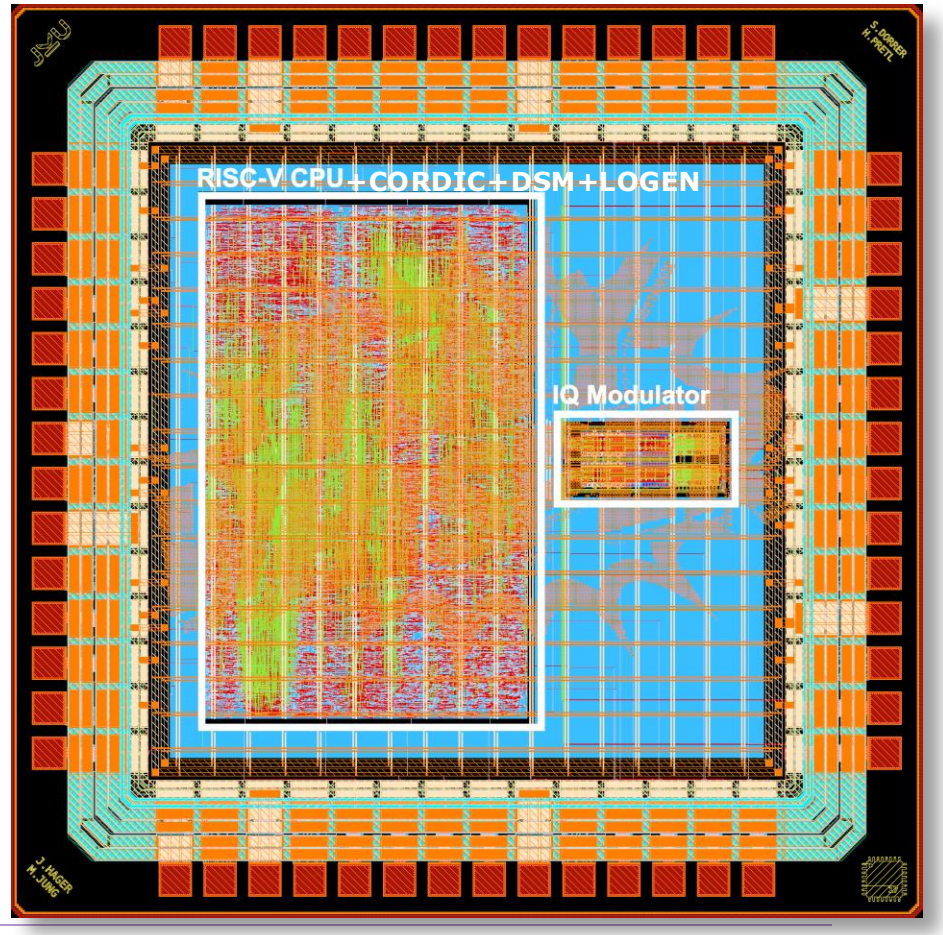
10m	28.124600 MHz	28 MHz	124.600 kHz

Realized RF SoC



- **IHP SG13CMOS** (CMOS5L)
- 2.0×2.0 = 4 mm²
- 56 die pads in a wire-bonded QFN-48 package
- Core supply V_{DD} = 1.5 V
- I/O supply V_{DDIO} = 3.3 V
- Chip in production!
- **Fully open-sourced w/ a permissive license: https://github.com/iic-jku/TinyWhisper**



SoC Toplevel Integration

- **Digital-on-top** integration with LibreLane/OpenROAD

  Pad frame gen., digital and custom analog macro P&R, fill & decoupling, DRC/LVS
- **HDL linting and simulation** using iverilog and Verilator plus FPGA prototyping
  - Mixing SystemVerilog and Verilog
  - Cocotb test-bench and Python data evaluation for DSMOD
- **Analog blocks** created in custom flow
  - Schematic in Xschem, simulation w/ ngspice (incl. mixed-mode and RCX); corner and Monte-Carlo simulations using CACE
  - Layout with KLayout, DRC/LVS with KLayout, RCX with KLayout-PEX
- **Top-level LVS w/o black-boxing**
  - Analog-on-top in Xschem w/ custom I/O cell symbols, several helper scripts
- **Highly automated** (Makefile-driven)

Everything Available Open-Source

TinyWhisper

HDL, schematics, layouts, sim TB, flow scripts, docs, …



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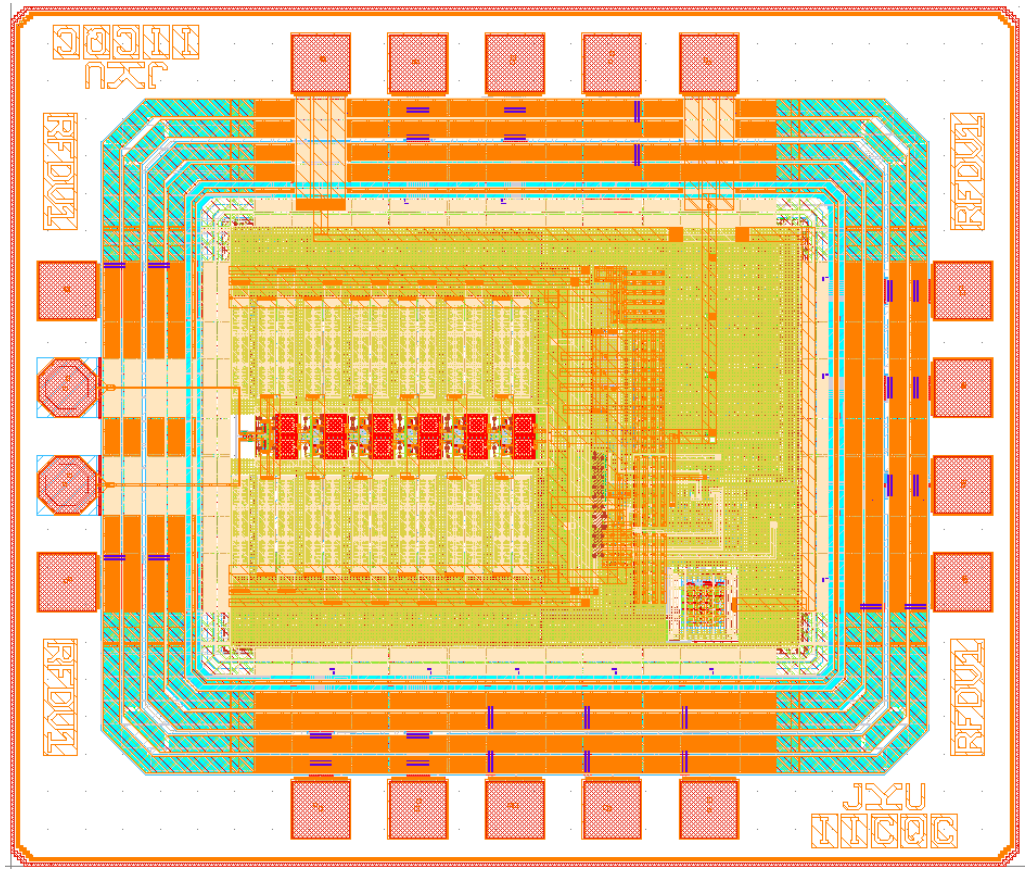
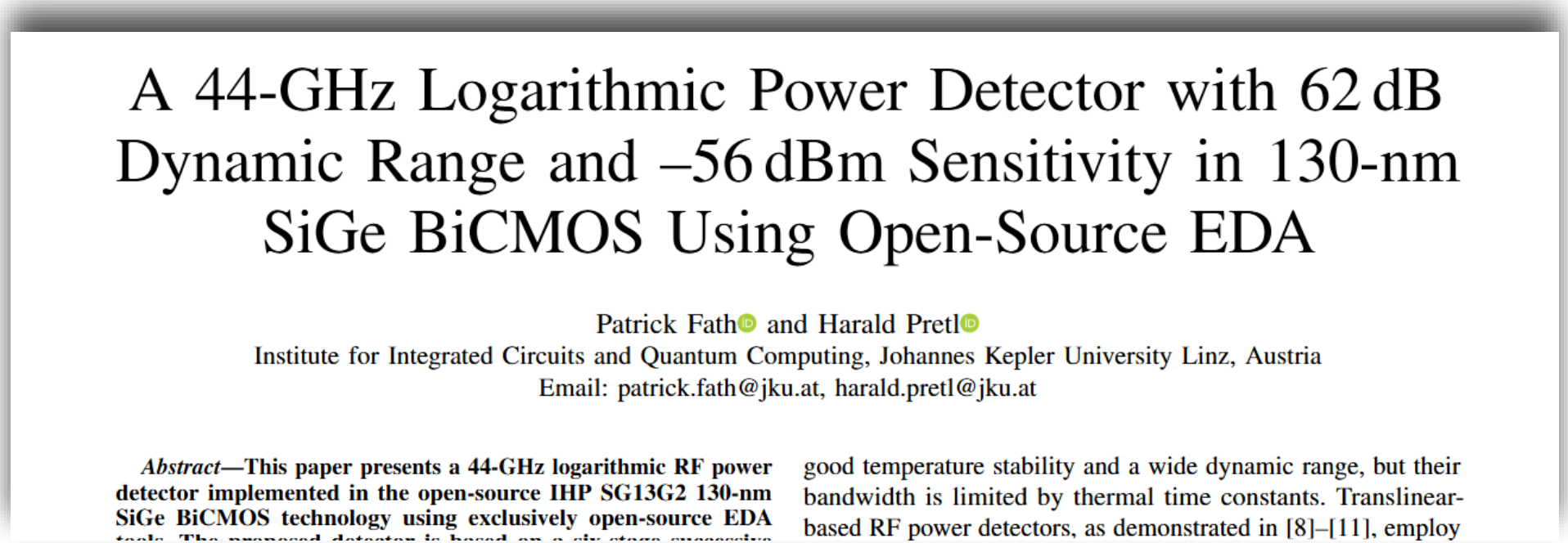
Logarithmic RF Detector

- **IHP SG13G2 BiCMOS**
- 1.4×1.2 = 1.68 mm^2
- Wide bandwidth (0.15 GHz to 44.7 GHz)
- 6-stage successive-detection logarithmic video amplifier
- Fast duty-cycling to minimize power consumption
- Applications incl. TX output power control, RX automatic gain control, RF signal monitoring
- Open-source EDA/PDK does not mandate open-sourcing everything ➔ design is **closed-source**
- Chip in production!



Logarithmic RF Detector

- Detailed design to be presented at **IEEE APCCAS** in Oct. 2026



A 44-GHz Logarithmic Power Detector with 62 dB Dynamic Range and –56 dBm Sensitivity in 130-nm SiGe BiCMOS Using Open-Source EDA

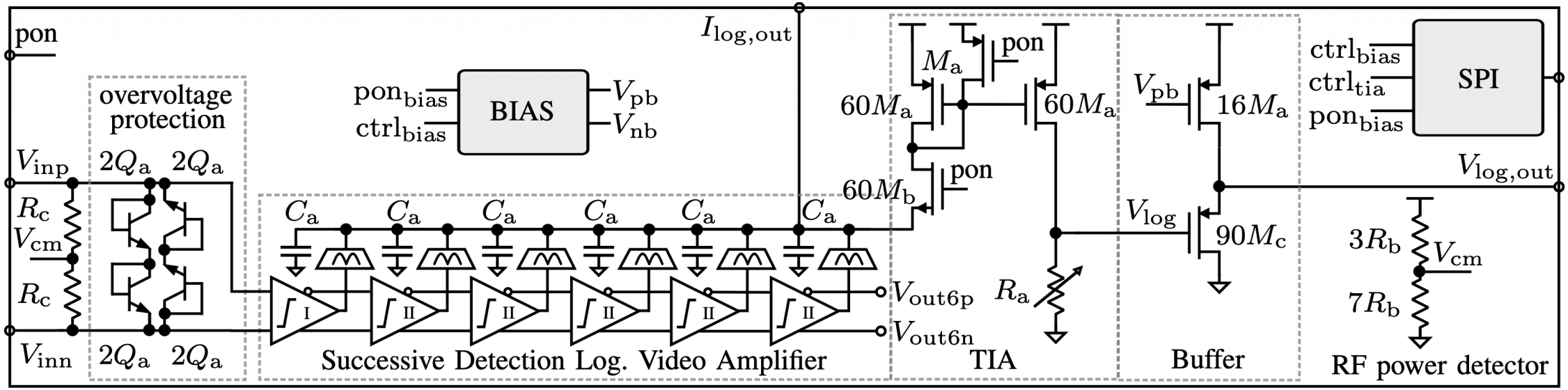
Patrick Fath and Harald Pretl
Institute for Integrated Circuits and Quantum Computing, Johannes Kepler University Linz, Austria
Email: patrick.fath@jku.at, harald.pretl@jku.at

***Abstract*—This paper presents a 44-GHz logarithmic RF power detector implemented in the open-source IHP SG13G2 130-nm SiGe BiCMOS technology using exclusively open-source EDA**

good temperature stability and a wide dynamic range, but their bandwidth is limited by thermal time constants. Translinear-based RF power detectors, as demonstrated in [8]–[11], employ

Logarithmic RF Detector Design

- RF signal path using **HBTs for speed**
- IF path and biasing implemented in **CMOS**
- **SPI interface** for tuning & control



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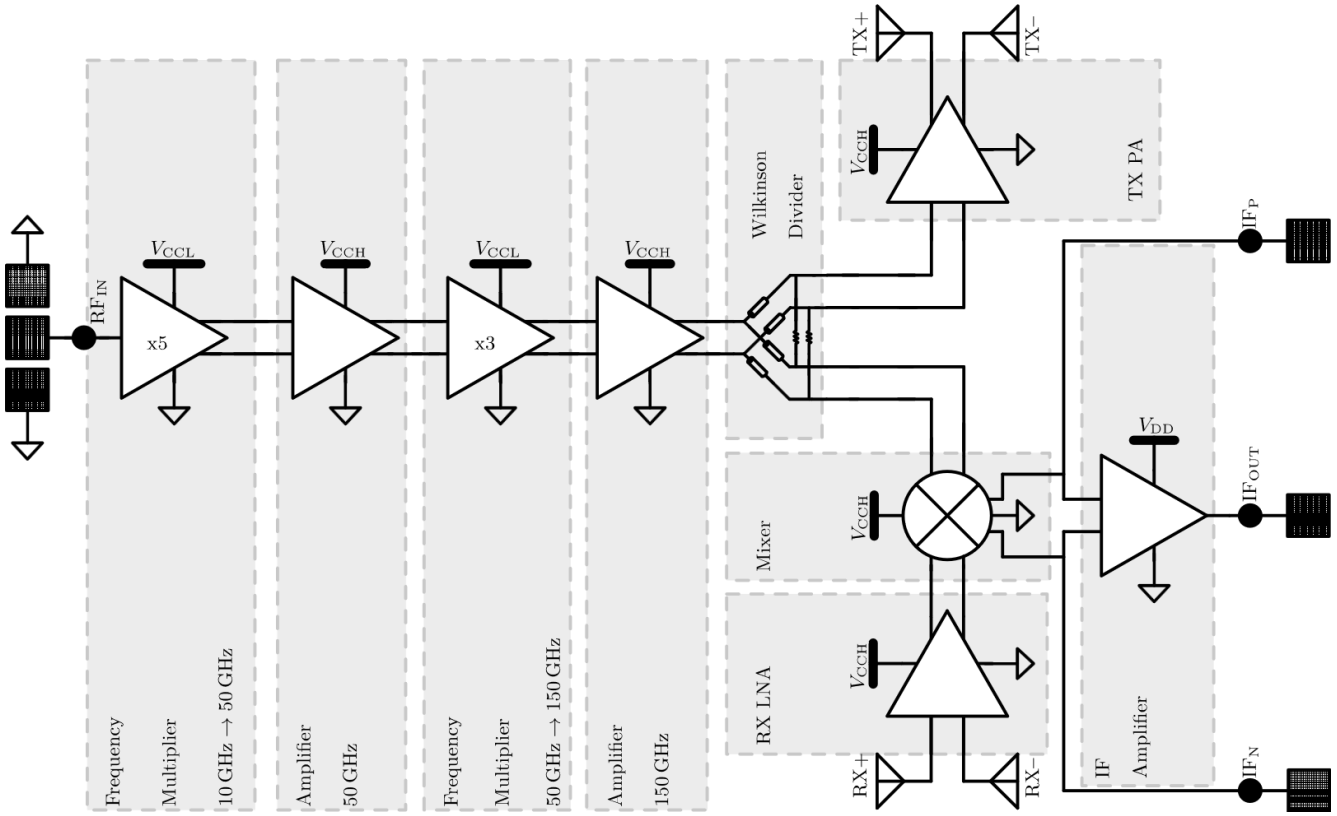
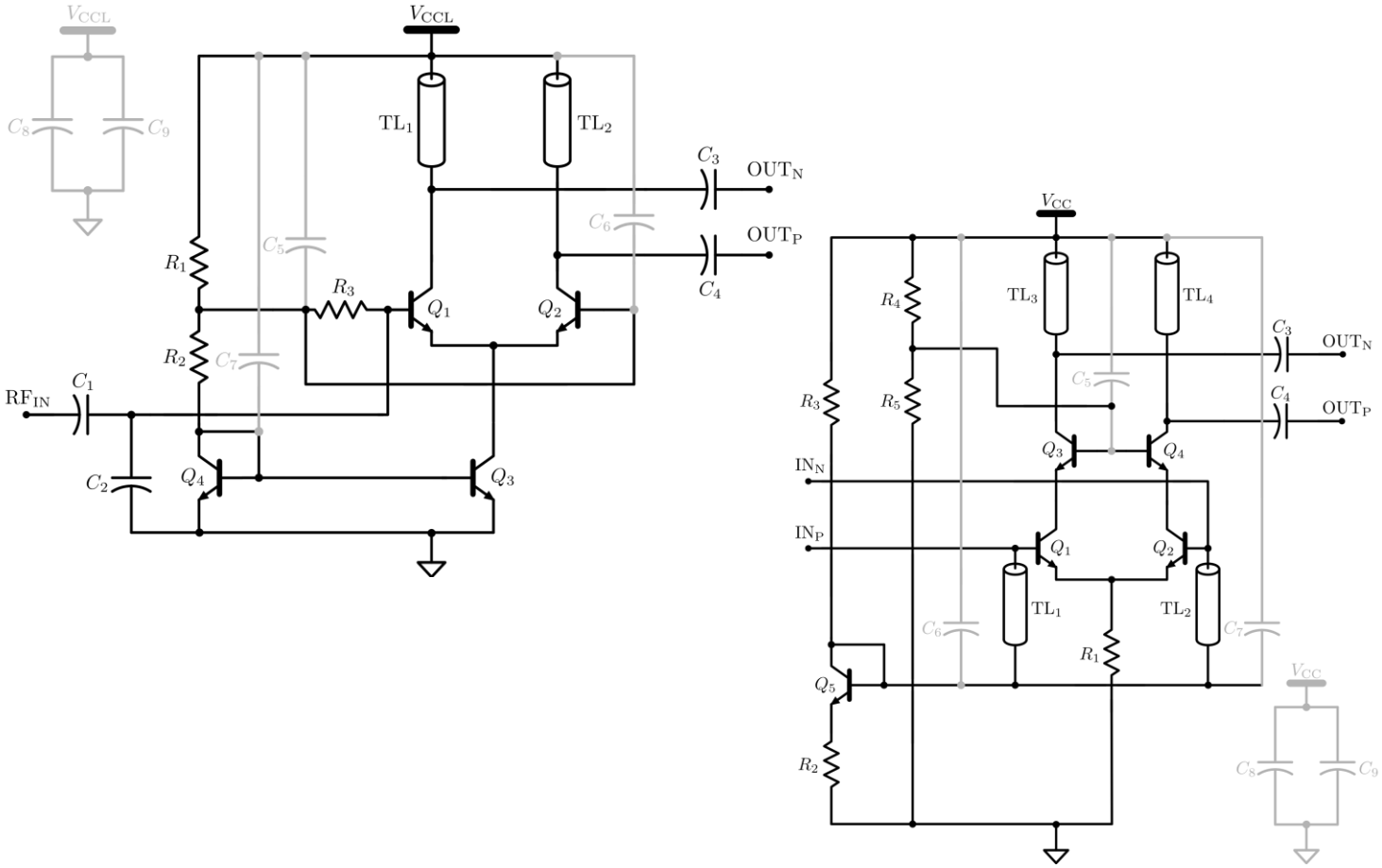
150-GHz FMCW Radar

- **D-band FMCW radar**
- 2.0×1.0 = 2.0 mm²
- Target range of **1.5 m** (gesture recognition)
- 10-GHz external frequency ramp
- ×15 multiplication, integrated PA/LNA
- differentially-driven **on-chip patch antennas**
- Detailed description in **Ghaith Al Sabagh's master's thesis**
- Chip in production



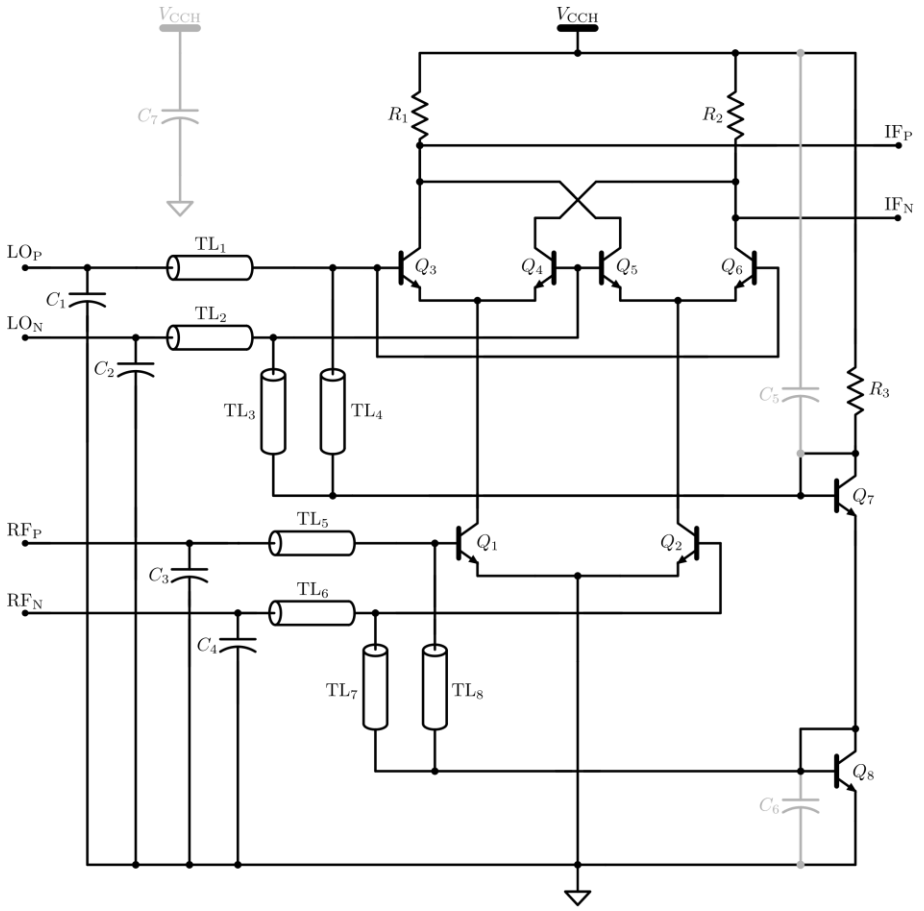
Circuit Design (Amplifiers, Multiplier)

- Input **multiplier** (×5) based on harmonically-tuned hard-driven diff-pairs
  - Single-ended input (resistive 50 Ω matching), differential out
- **Amplifiers** are cascoded diff-pairs with TL-based input/output matching
  - 50-GHz amplifier, tripler, 150-GHz amplifier, TX PA, RX LNA w/ different sizing



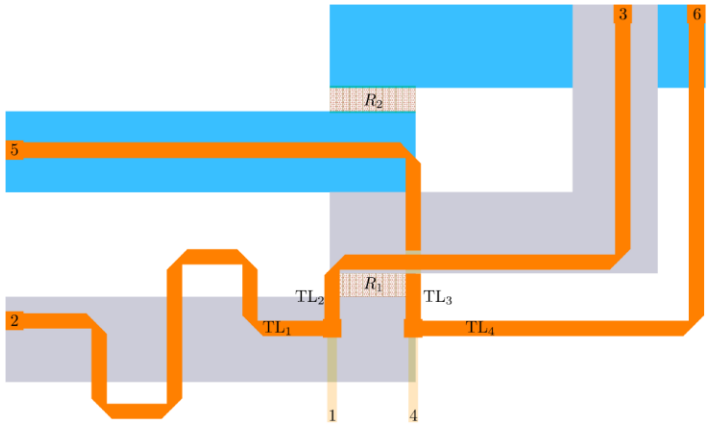
Circuit Design (Mixer)

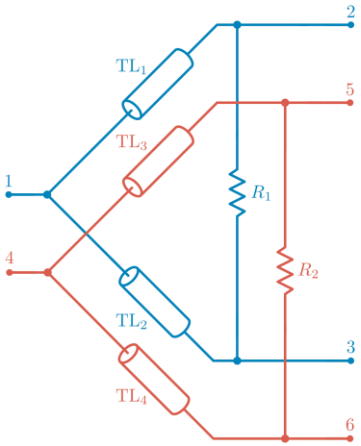
- Differential **Gilbert-cell mixer**
- During design time mixer NF could **not** be simulated (only **estimated** from large-signal gain simulation)
  - VACASK now offers **transient noise** simulation ➔ can simulate **mixer NF** and oscillator **noise**
  - VACASK has more great features, and is rapidly evolving



Passives Design

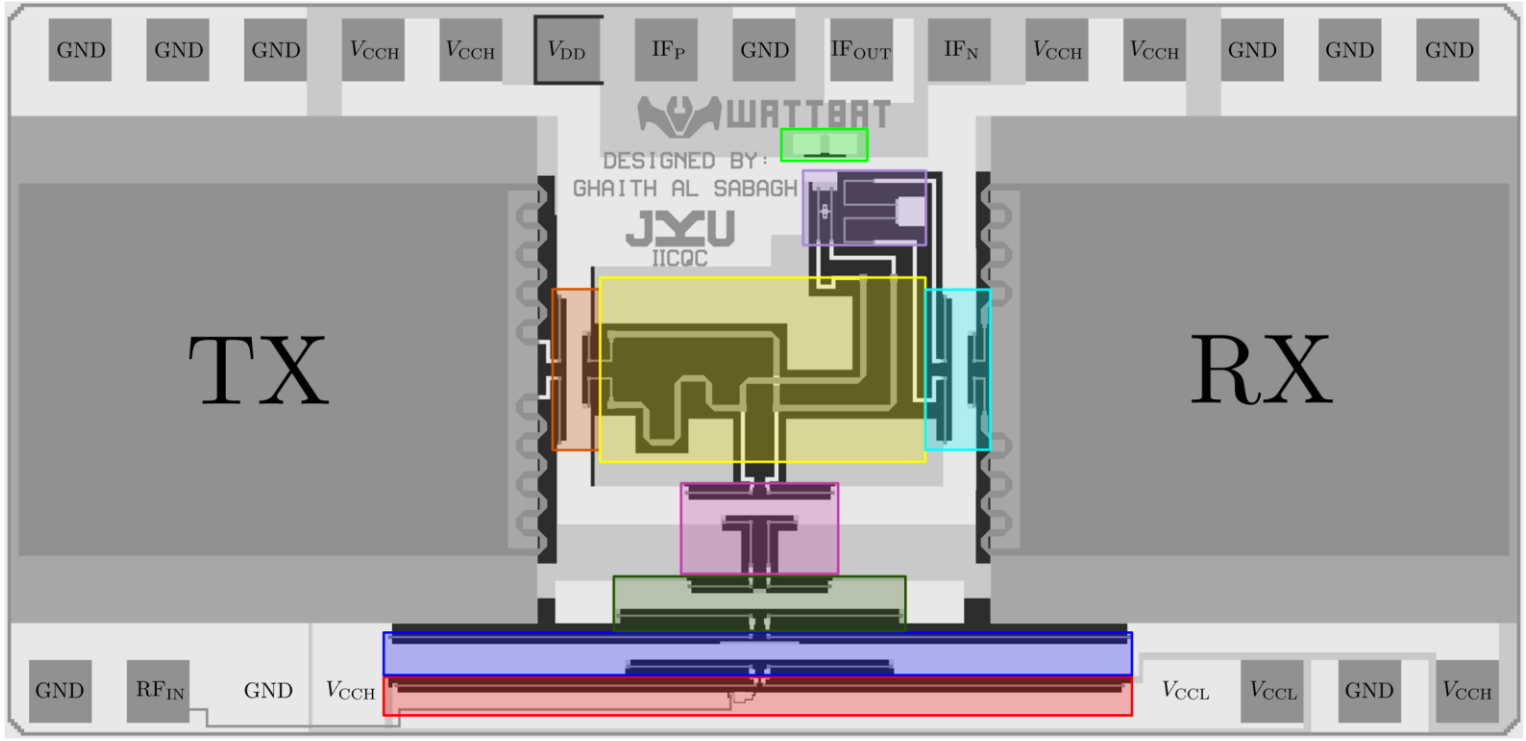
- Length-matched differential Wilkinson power divider
  - Six-port EM simulation (EC-FDTD) in openEMS
  - RL ≈ 20 dB, IL ≈ 4 dB
- Differential-feed on-chip patch antenna
  - 626×476 µm², radiator in TM2, reflector in M1
  - Antenna gain ca. −0.5 dBi, EIRP ≈ 9 dBm







Again, Completely Open-Source!





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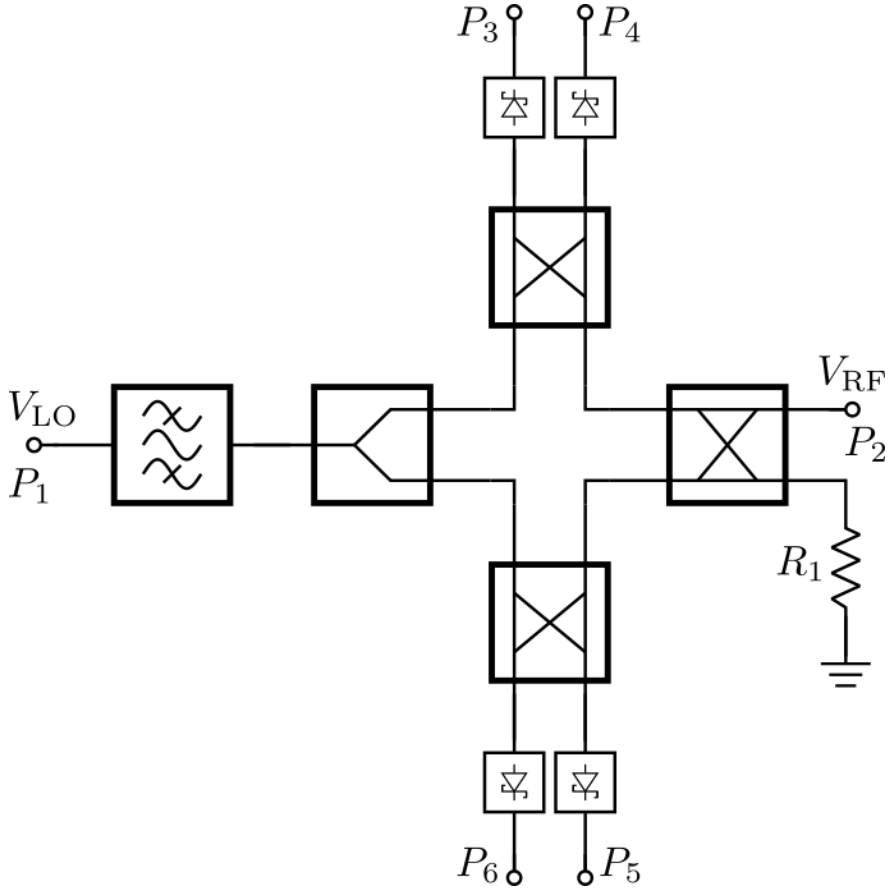
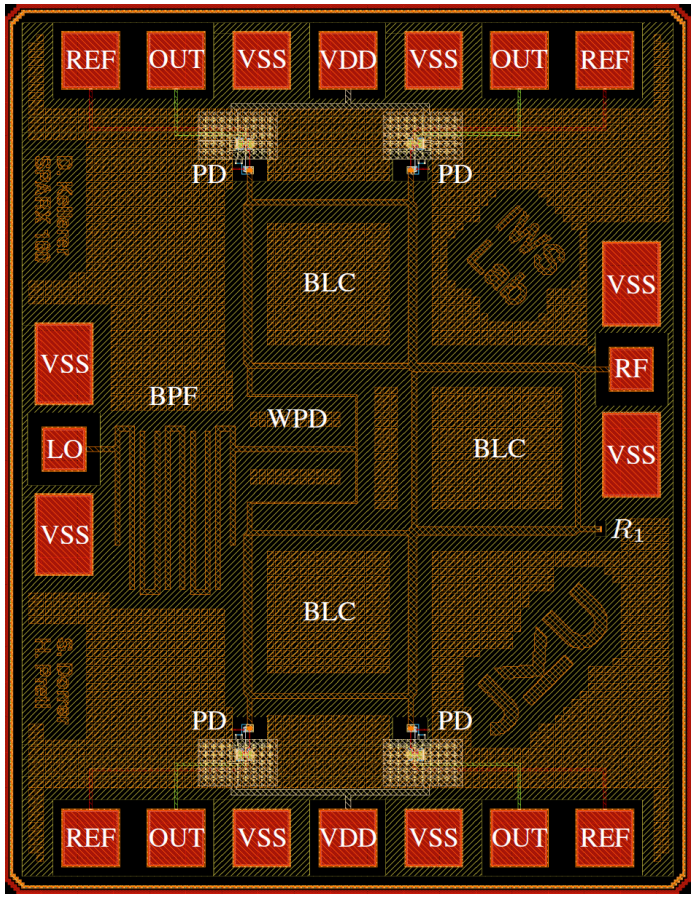
160-GHz Six-Port Receiver (SPARX)

- **Target: Build a 160-GHz six-port receiver w/ high automation in IHP SG13G2**
  - Layout generation, EM simulation, visualization ➔ all scripted in **Python**
  - **Complete flow Makefile-driven**
- **Methodology gaps to solve**
  - Layout generation of **distributed mm-wave structures** (Machine-Learning vs. Closed-form approach)
  - Layout generation of **lumped components** (pads, HBTs, resistors, capacitors, MOSFET, SBD)
  - Integrate EM-sim results in circuit simulations



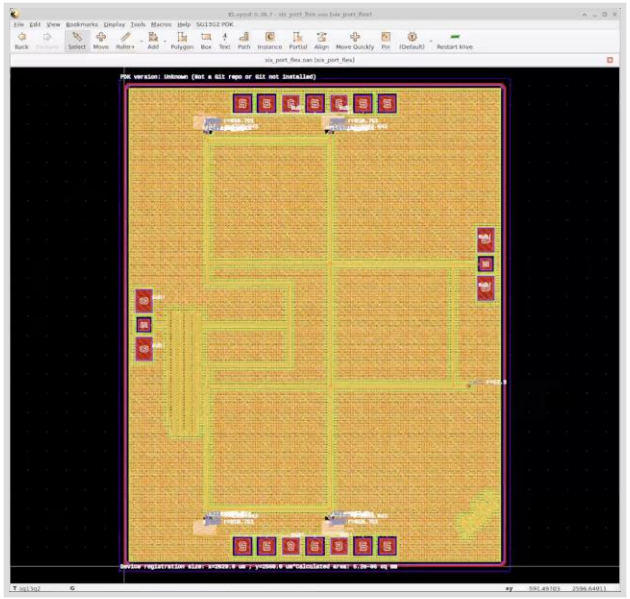
Automated Layout Generation

- **Python Library based on for mm-wave components**
  - Base building-block: Transmission lines
  - branch line coupler, Wilkinson power divider, hairpin coupled-line filter, edge-coupled t-lines
  - Instantiation of original **IHP p-cells** (HBT, res, cap, SBD, MOSFET) via wrapper function
  - Interface to AWS Palace for EM simulation
- **No ML or optimization,** just closed-form equations
- Complete **DRC-clean chip GDS** built from **code**
- Runs in **seconds** (ca. 2900 lines of code; incl. pads, seal ring, fillers, logos, etc.)
- **Chip in production** (150-GHz implementation)

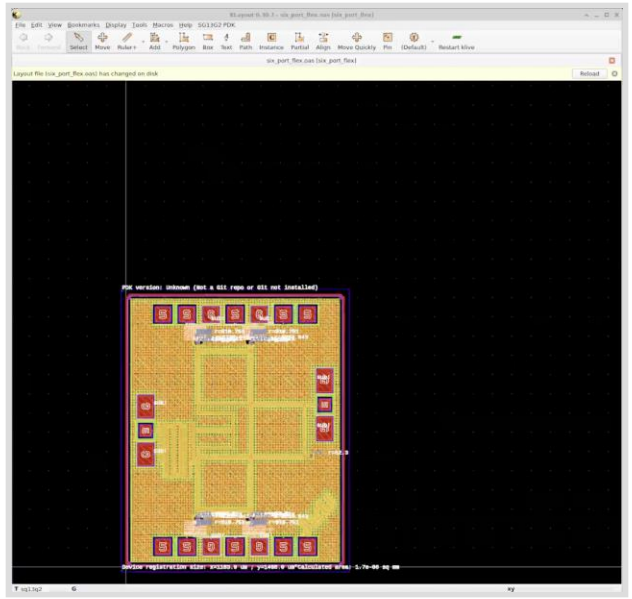


Ultimate Flexibility & Efficiency

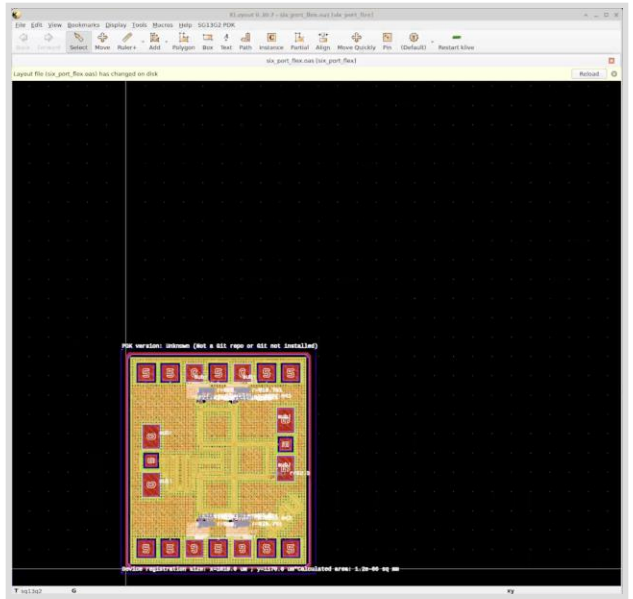
- Since chip layout created in Python ➔ scale complete design from 60 GHz to 300 GHz by changing **one constant** (frequency) in code



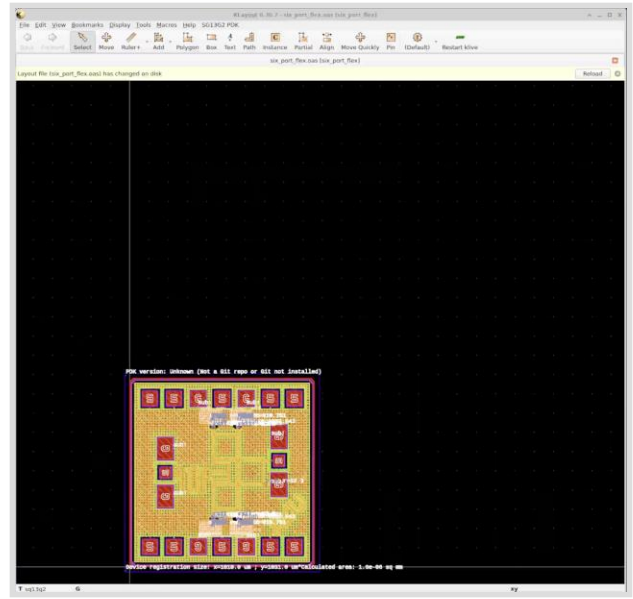
60 GHz



140 GHz



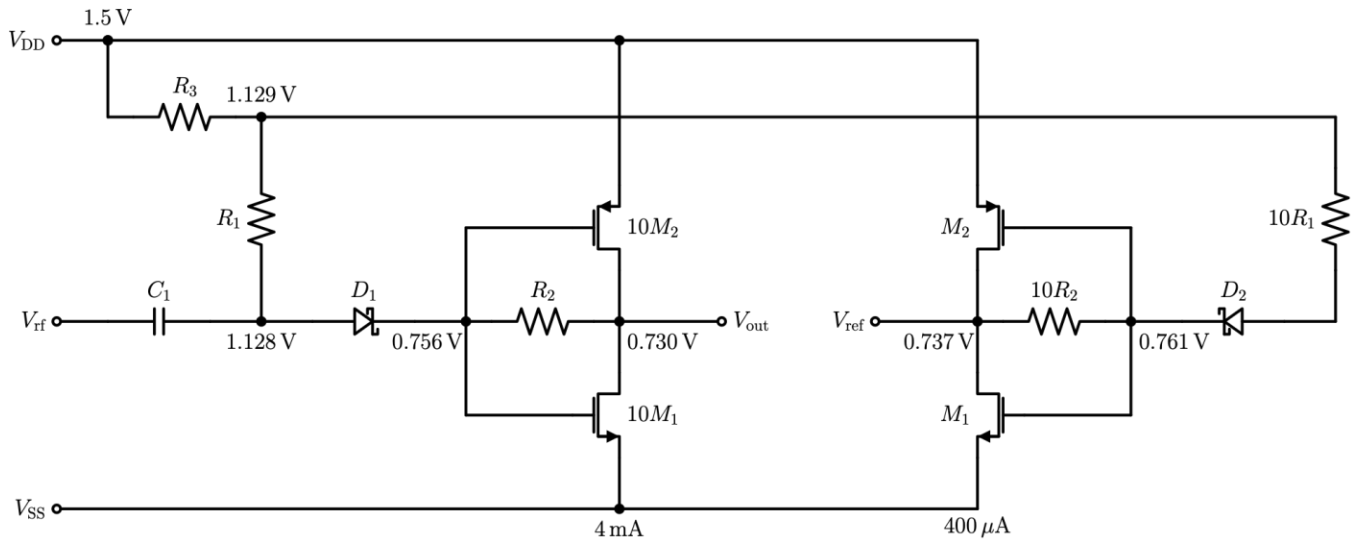
220 GHz



300 GHz

Mixer Design

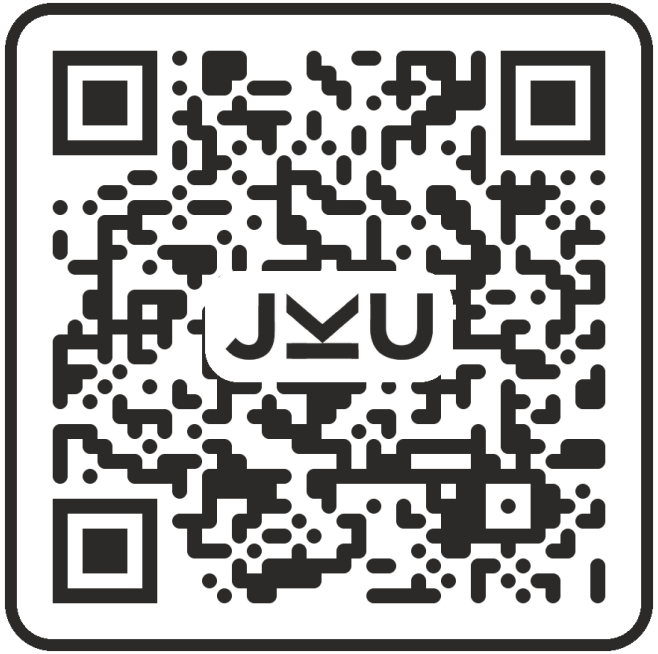
- Mixer based on Schottky barrier diode (SBD) plus TIA
- Circuit design in Xschem (manually), layout via Python
- Simulation together with EM-structures in VACASK (harmonic balance, transient noise WIP)



Everything Available Open-Source

SPARX

scalable six-port



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Conclusion

- All presented designs **currently in production**
  no silicon-proven results yet ➔ plenty to measure in the coming months
- Open-Source Tools and PDKs have seen huge progress in the last years!
  - Collaborative tool development
  - Collaborative design, Open-Source IP
- Biggest improvements for RFIC design:
  - VACASK brings many new simulation modes
  - SNP2LE allows integration of S-Parameter simulations to circuit simulations
  - Different options for
    - **EM simulation** (OpenEMS, AWS Palace)
    - **PEX** (magic+netgen, Klayout PEX)available

Questions?

Thank you!

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