PALMA DE MALLORCA
7-10 SEPTEMBER
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UNIVERSITAT ROVIRA i VIRGILI

UIB Universitat de les Illes Balears

Development of Cryogenic Model Libraries for FD-SOI Transistors



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Federal Ministry of Research, Technology and Space

SOLID

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IEEE SSCS Electron Devices Society CAS

Introduction

AdMOS GmbH: Advanced Modeling Solutions





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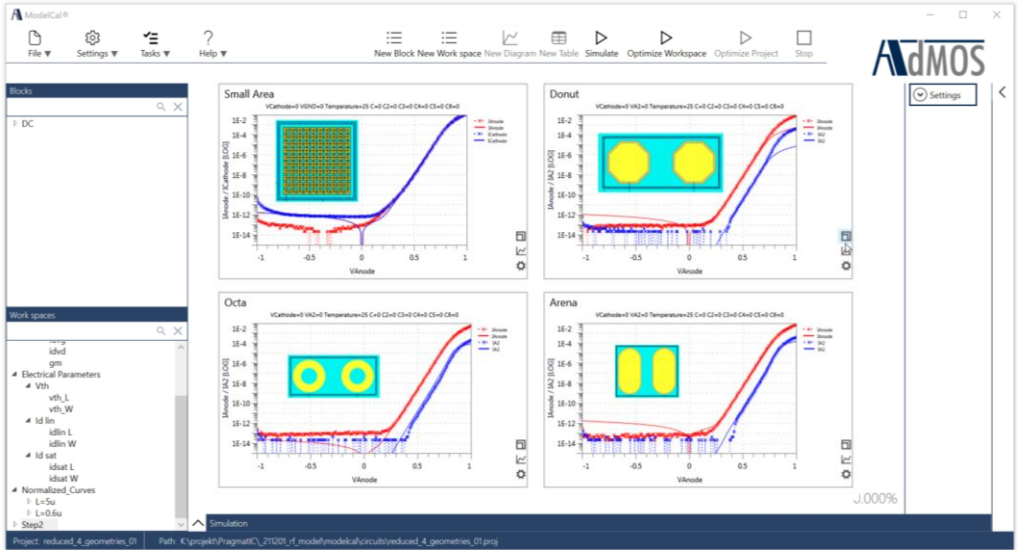
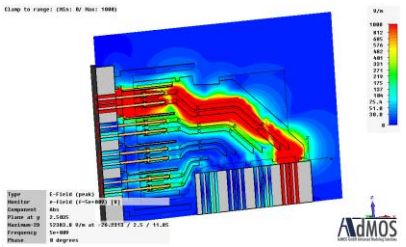
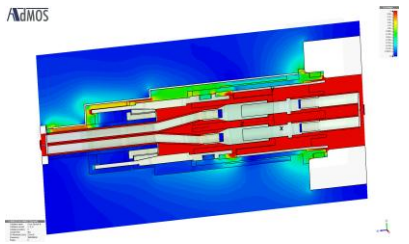
http://www.admos.de





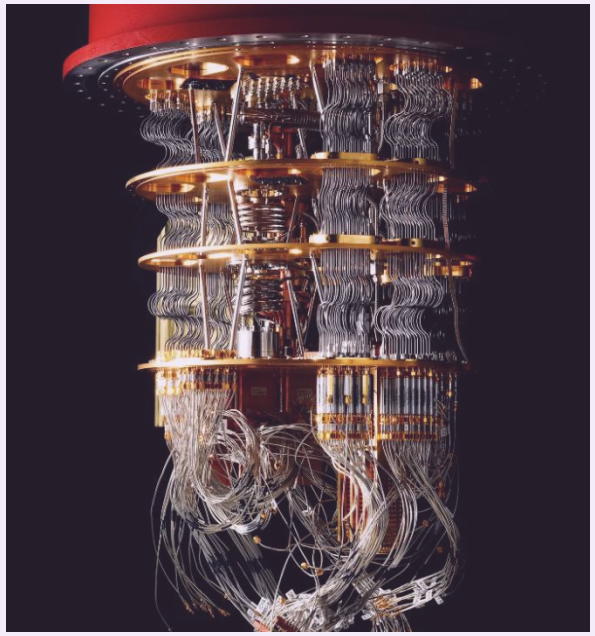




Cryogenic CMOS

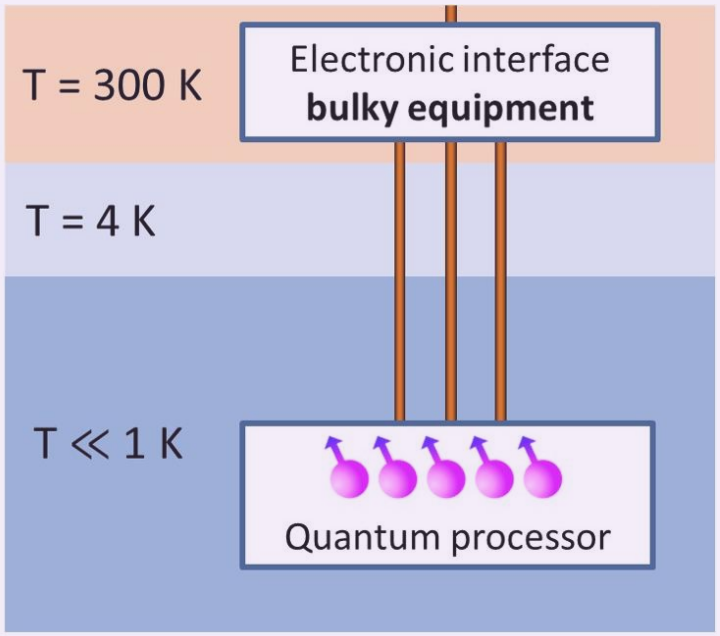
Quantum Computing: The wiring bottleneck!

Google Sycamore QC

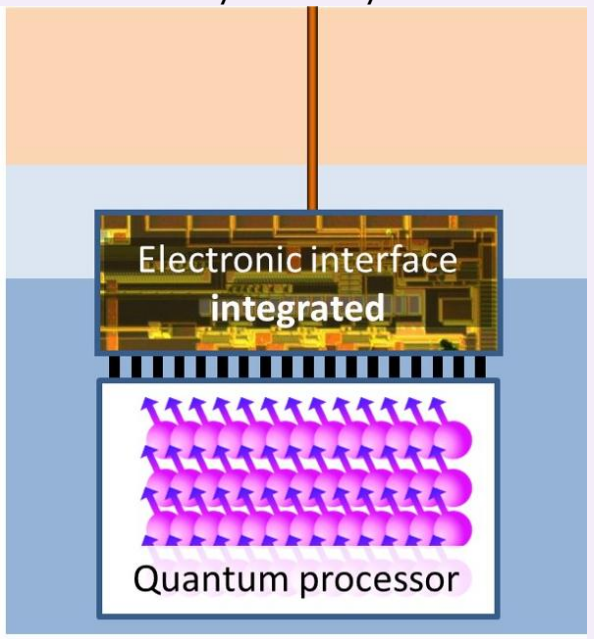


www.wired.co.uk/article/quantum-supremacy-google-microsoft-ibm

Classical Brute Force Approach



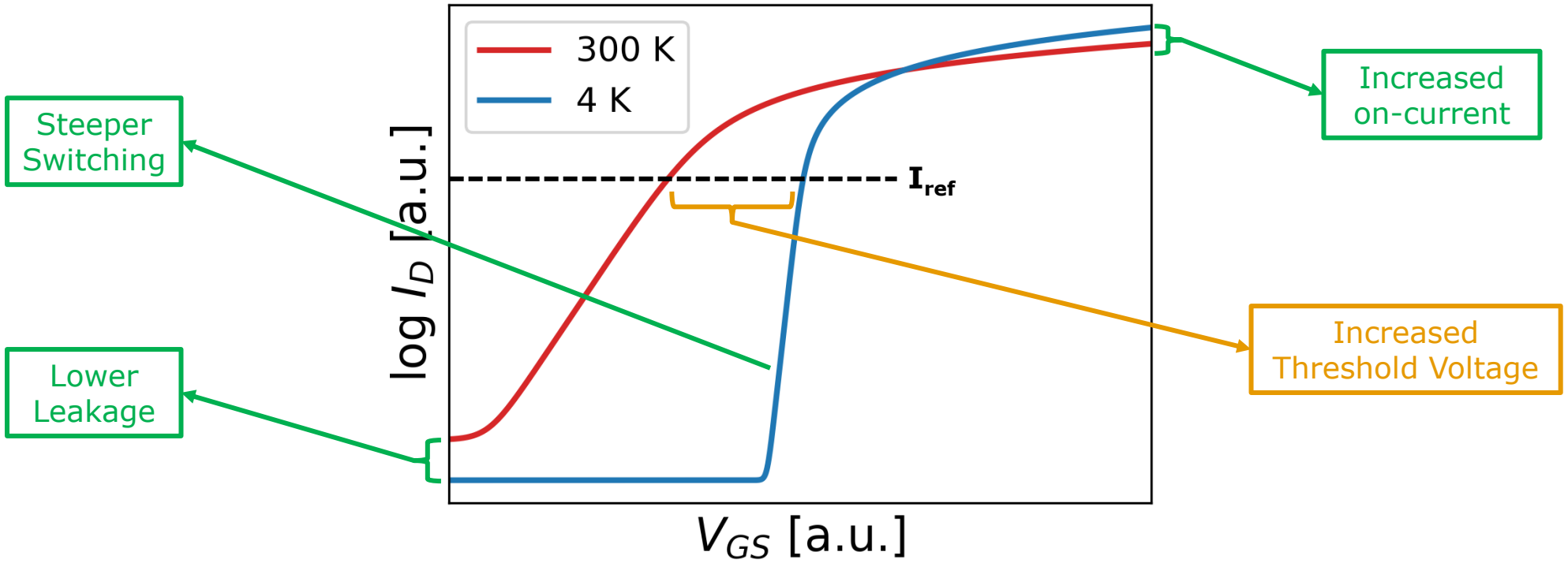
Scalabilty with Cryo-CMOS



F. Sebastiano *et al.*, "Cryo-CMOS Interfaces for Large-Scale Quantum Computers," *2020 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp. 25.2.1-25.2.4

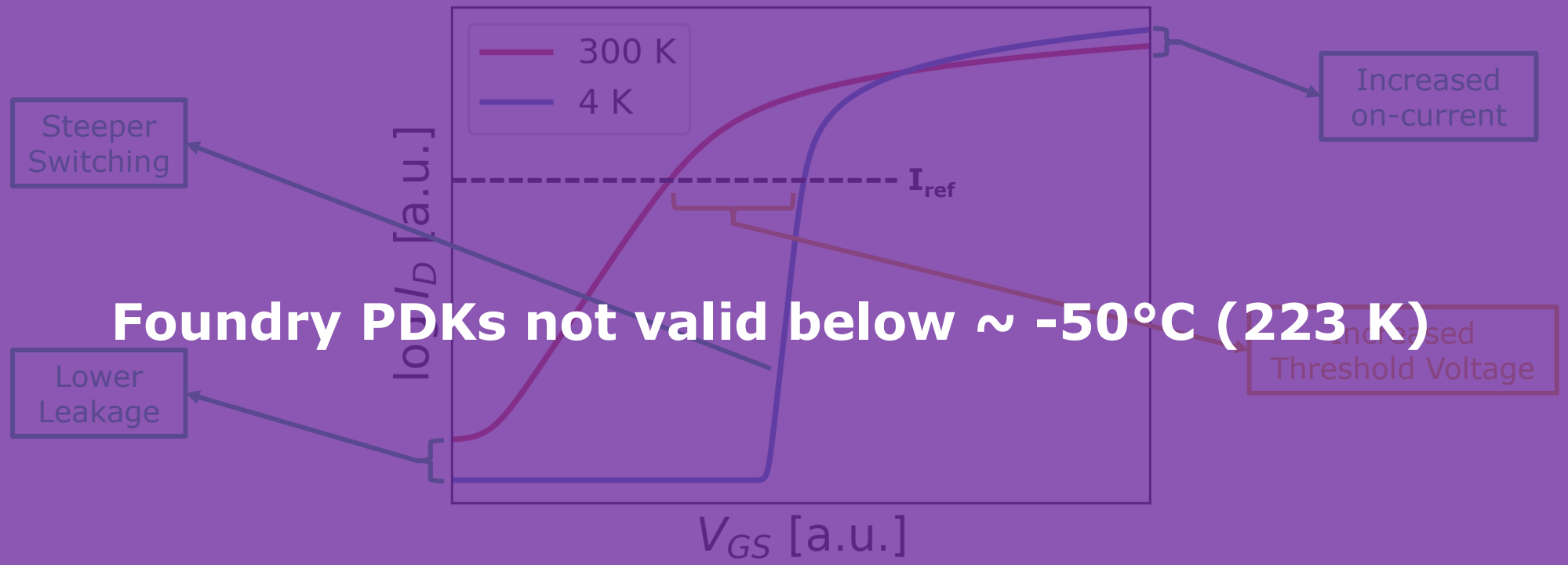
Cryogenic CMOS

MOSFET behavior at RT vs Cryo:



Cryogenic CMOS

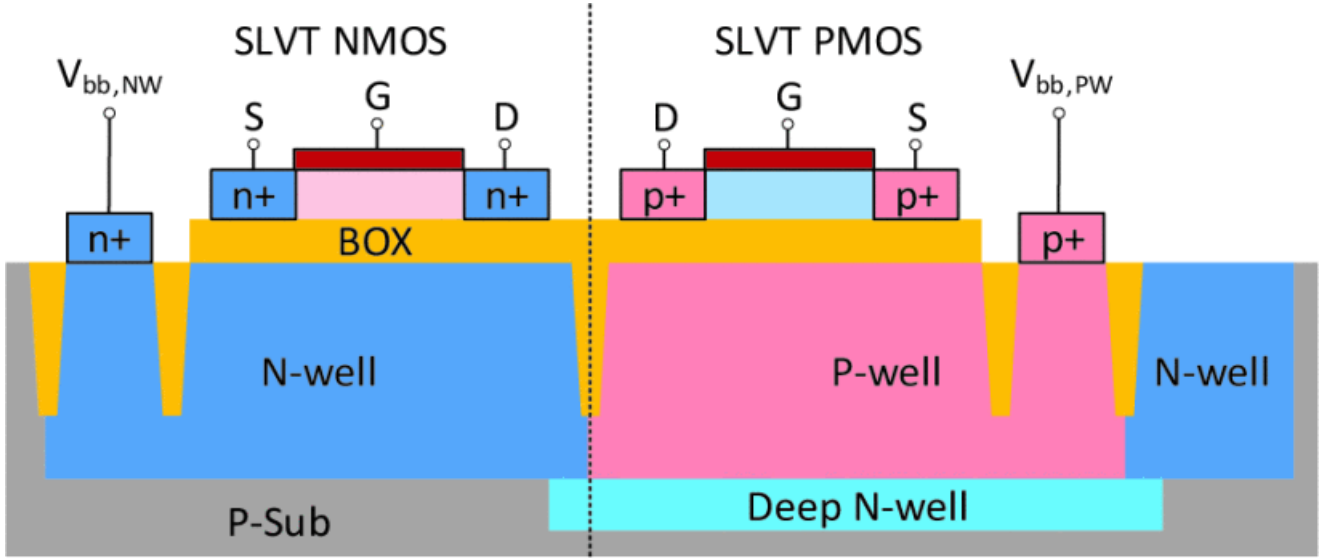
MOSFET behavior at RT vs Cryo:



Foundry PDKs not valid below ~ -50°C (223 K)

Measurements

Fully-Depleted Silicon-on-Insulator: GF 22 FDX

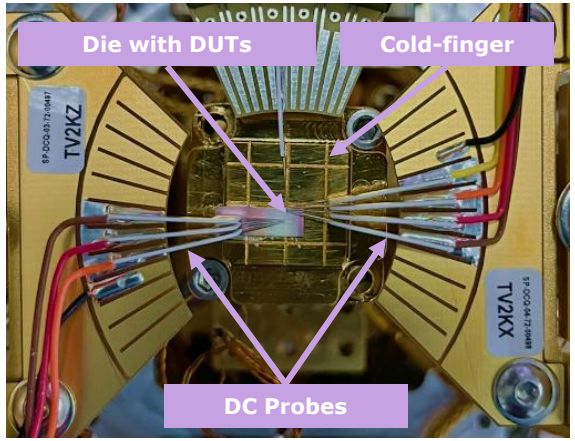


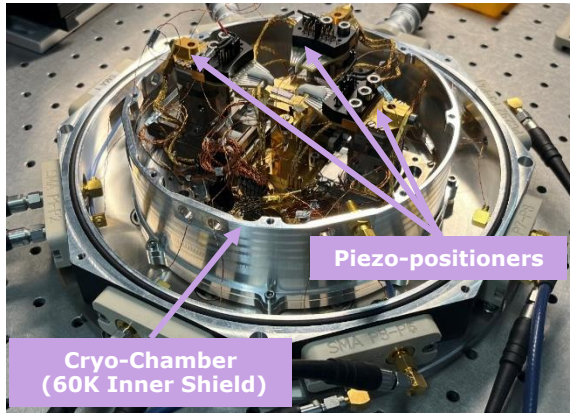
Lotfi et al, *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*

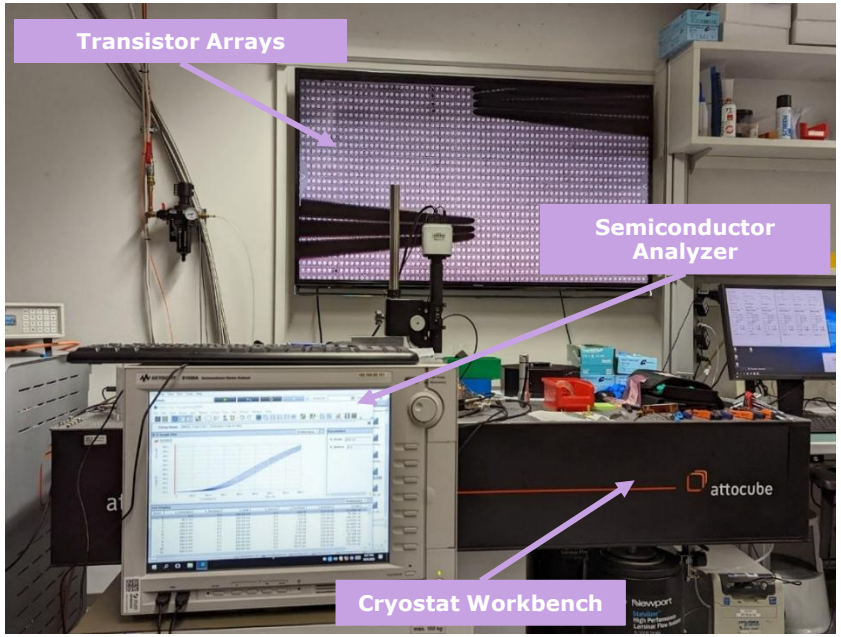
- Low Leakage
- Low Power Consumption
- Reduced Dopant Fluctuations
- Back-Biasing Capability

Measurements

Cryogenic Setup and DUTs



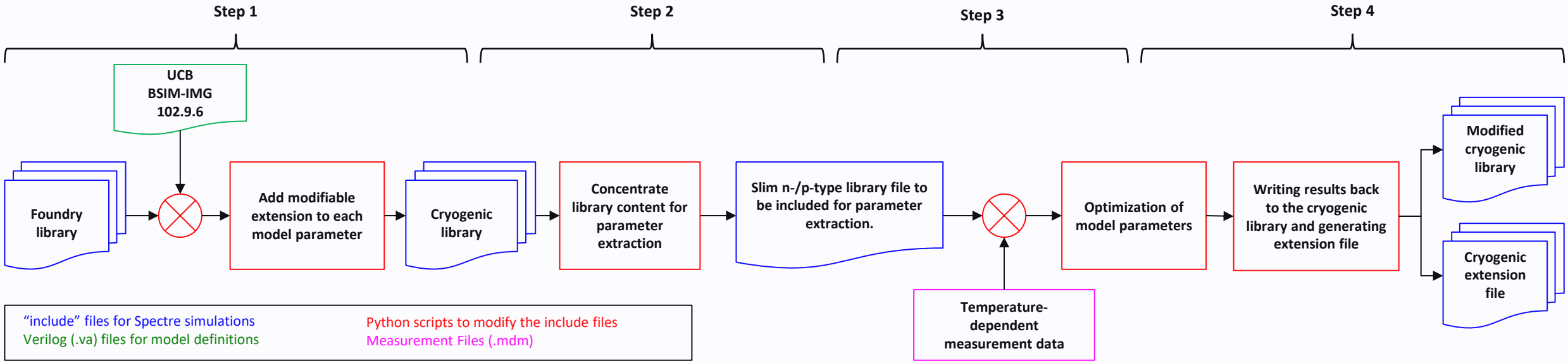




- 14 Thin-oxide; 10 Thick-oxide
- Both n- and p-types

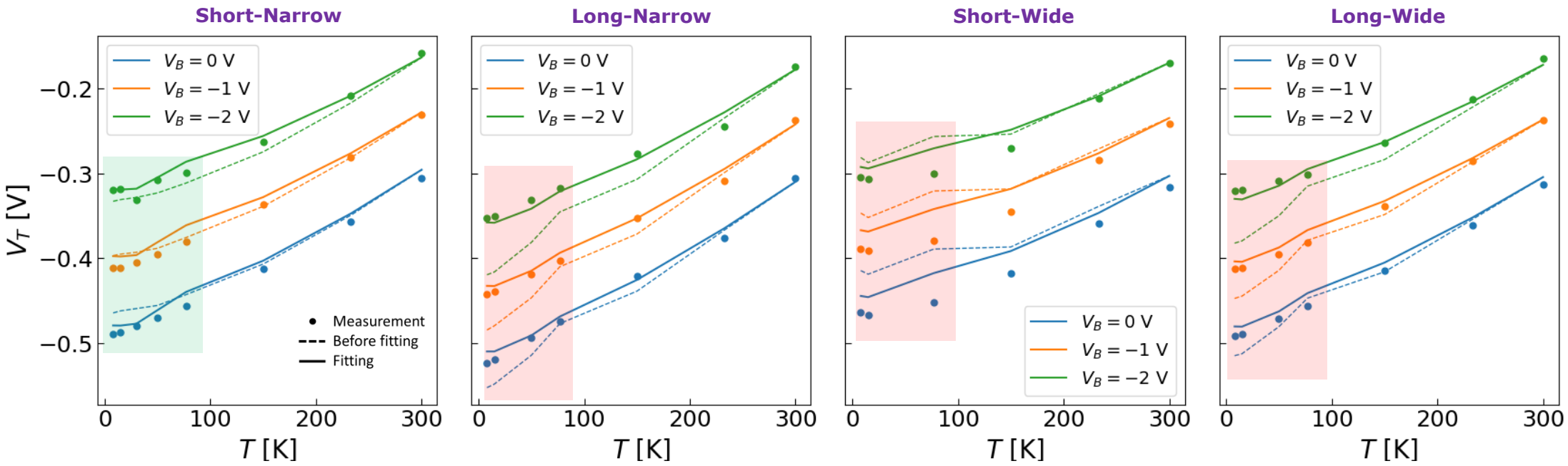
Modeling Approach

Overview:



Parameter Optimization

Example of pMOS Threshold Voltage (V_T):

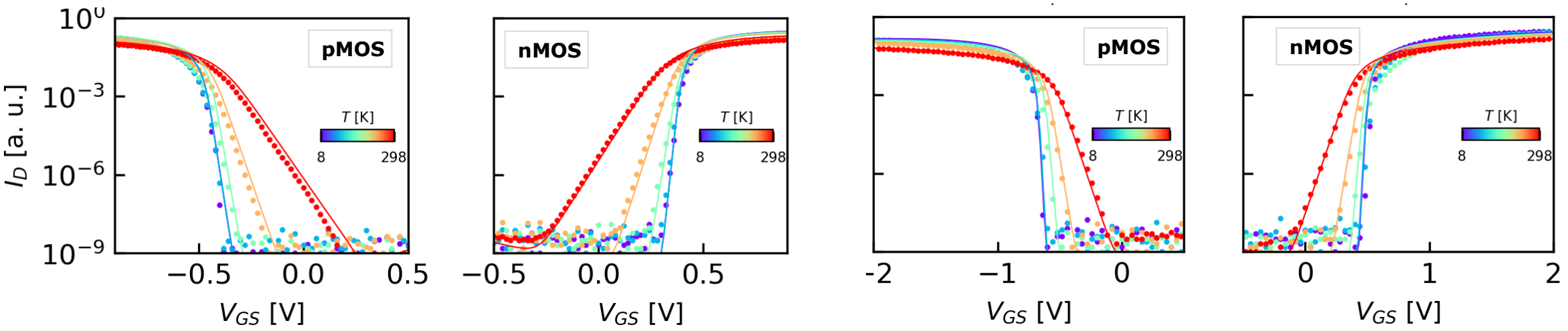


- **Before fitting** → Baseline BSIM-IMG with cryo-extension
- **Fitting** → Baseline BSIM-IMG with cryo-extension + Adjustable parameters

P. Chava *et al.*, "*Evaluation of Cryogenic Model Libraries for FDSOI CMOS Transistors*," in IEEE Transactions on Electron Devices, vol. 73, no. 5, pp. 2907-2914, 2026.

Model Validation

Single Transistors (Temperature Dependence)



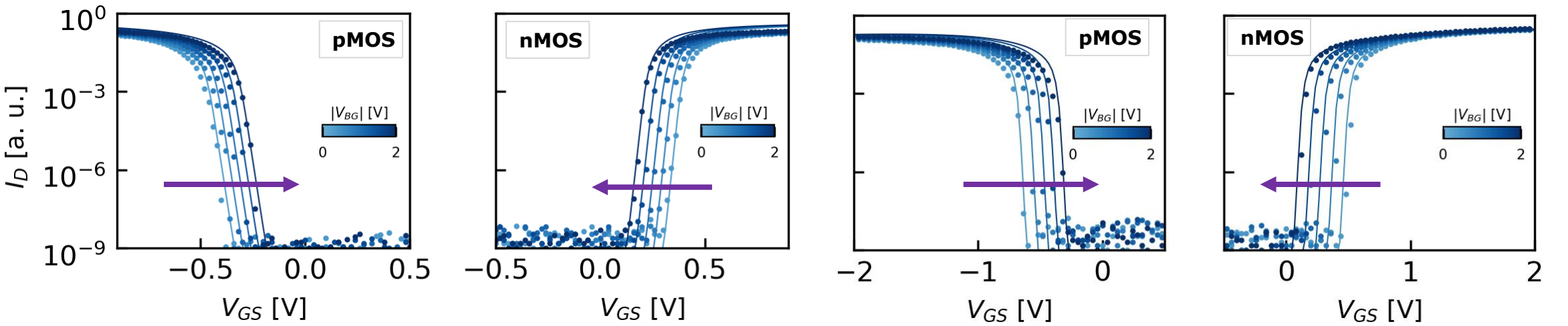
Thin Oxide (V_{nom} = 0.8 V)

Thick Oxide (V_{nom} = 1.8 V)

P. Chava et al., "*Cryogenic-Aware EDA-Compatible Design Libraries for FD-SOI Transistors*," 2026 10th IEEE EDTM, Penang, Malaysia, 2026, pp. 1-3

Model Validation

Single Transistors (Back-bias Dependence @ Cryo)



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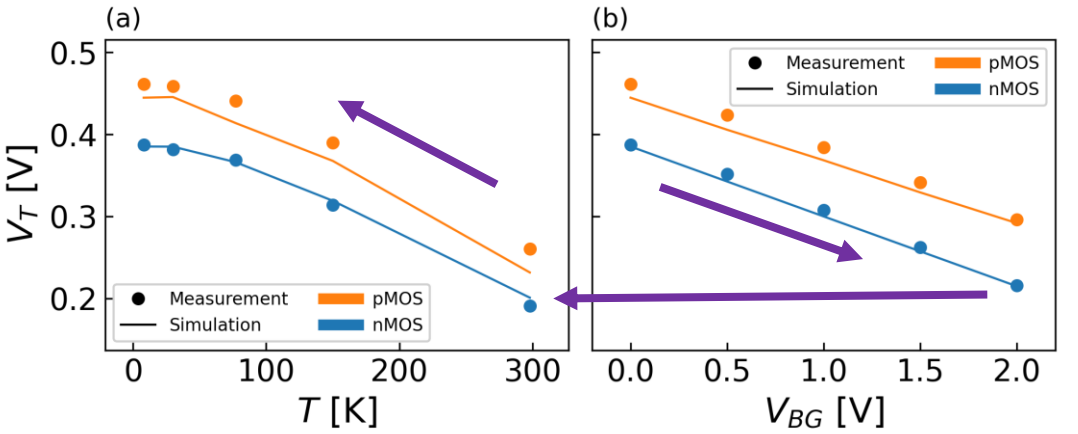
Model Validation

Threshold Voltages – vs. Temperature & Back-Bias



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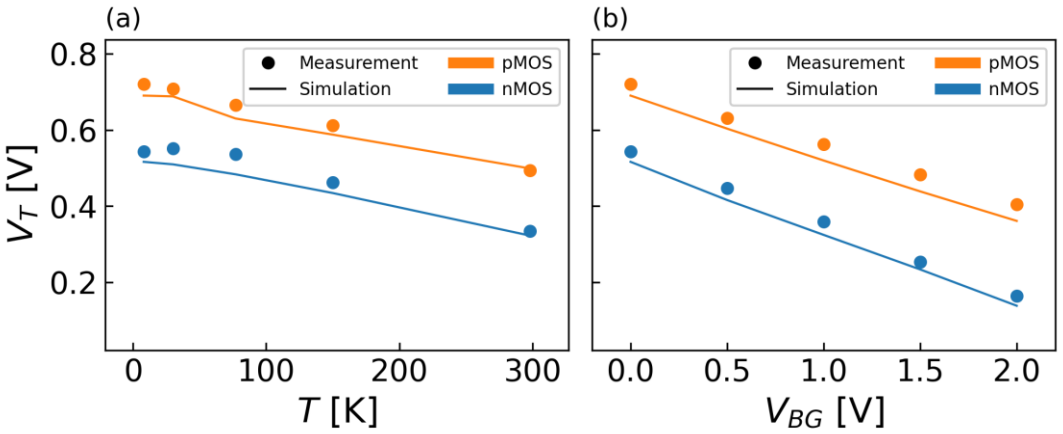

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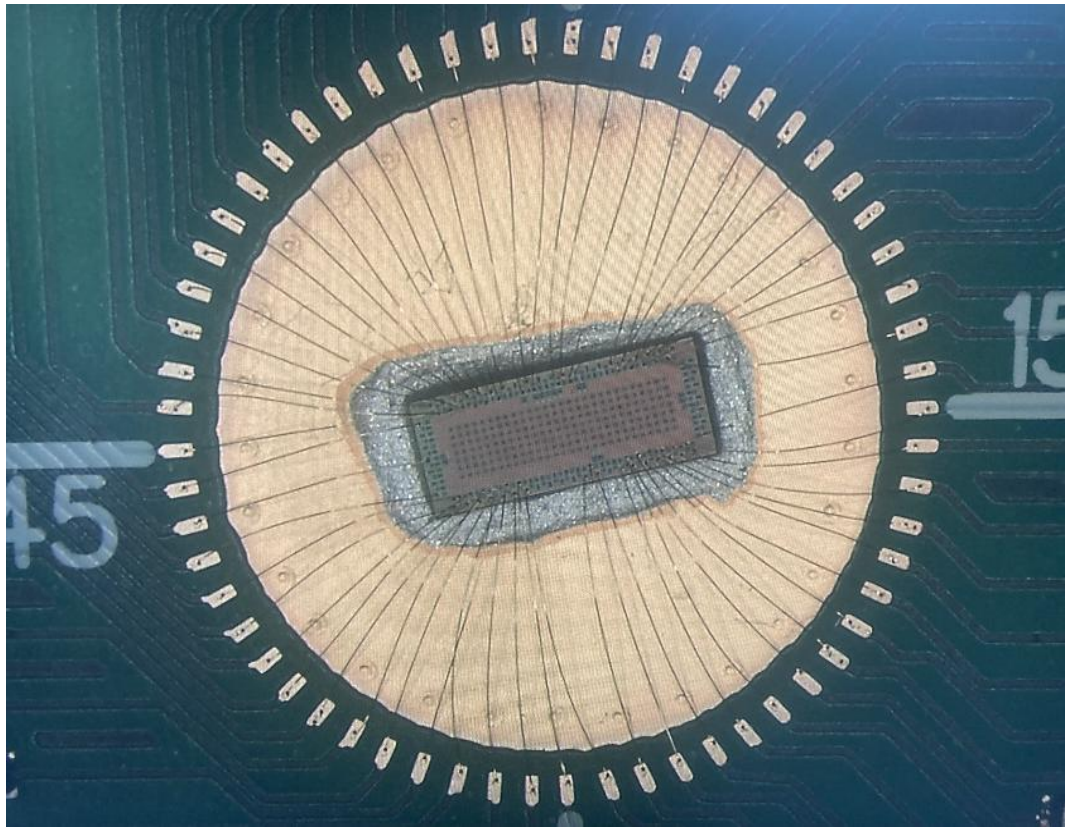
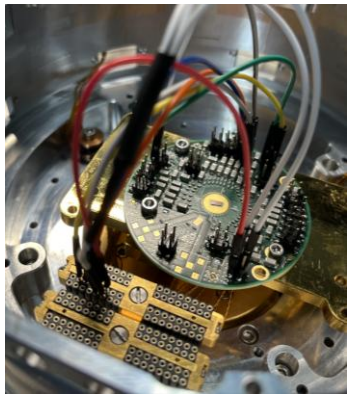
P. Chava et al., "*Cryogenic-Aware EDA-Compatible Design Libraries for FD-SOI Transistors*," 2026 10th IEEE EDTM, Penang, Malaysia, 2026, pp. 1-3

Model Validation

Dedicated Test-chip for Model Verification



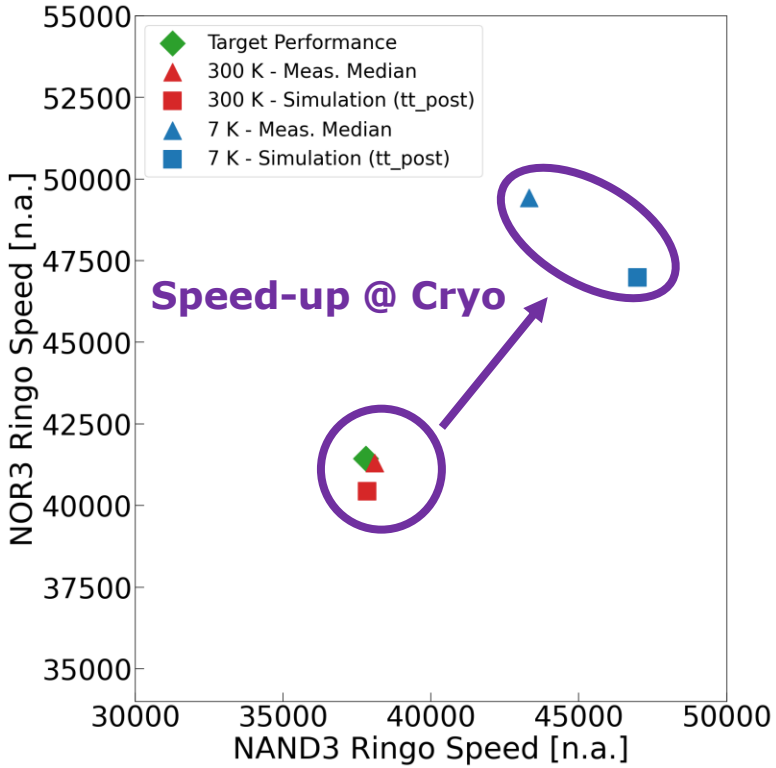


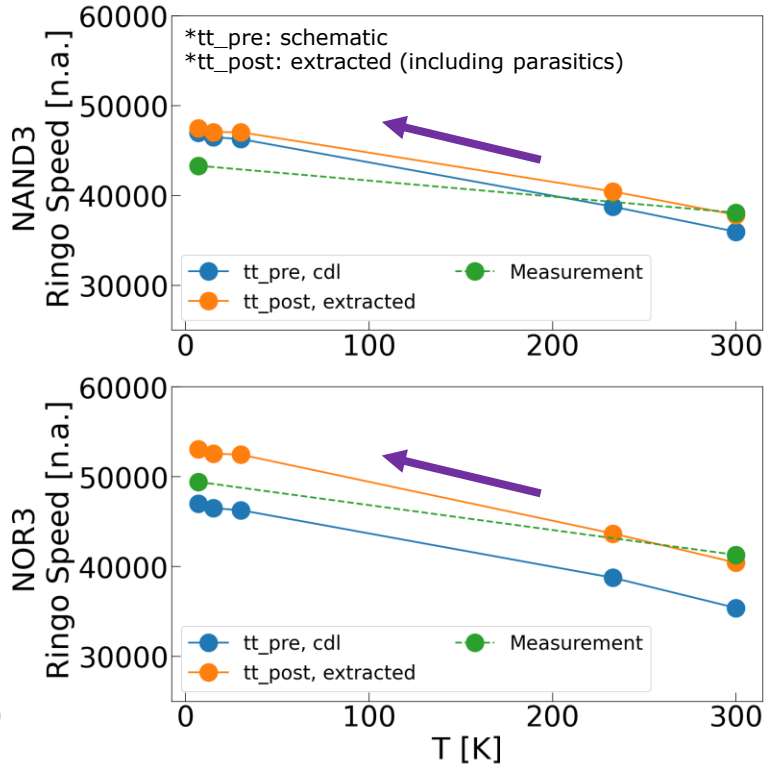
Racyics

- Circuit Blocks:
  - Ring Oscillators
  - TIA
  - SRAM
  - Temperature Sensors
- Adaptive-Body-Bias (ABB) Regulation Scheme for:
  - Different Speed Targets
  - Multiple Supply Voltages

Model Validation

NAND3 & NOR3 Standard Cell Logic Gates

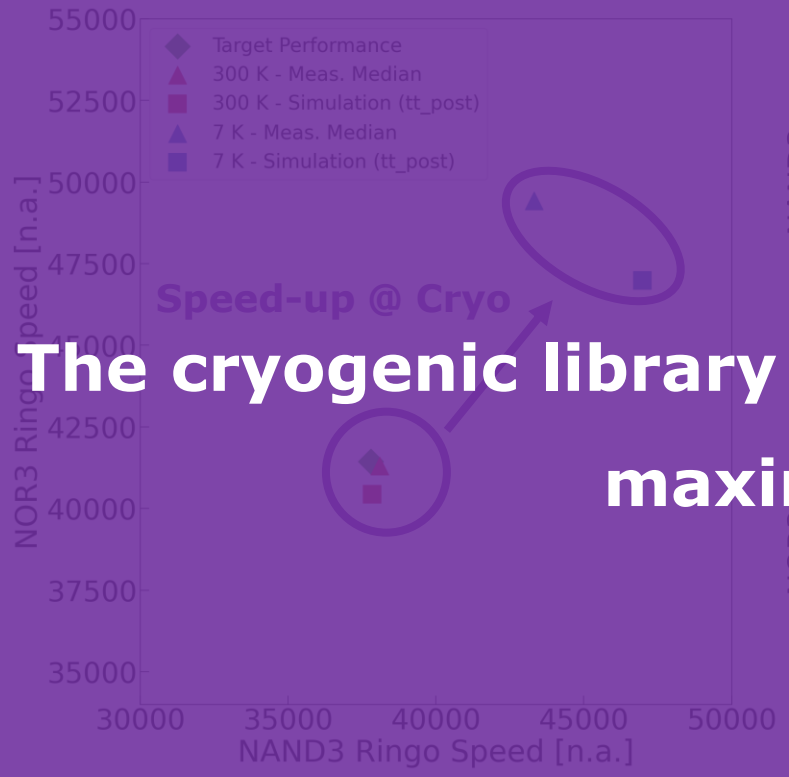


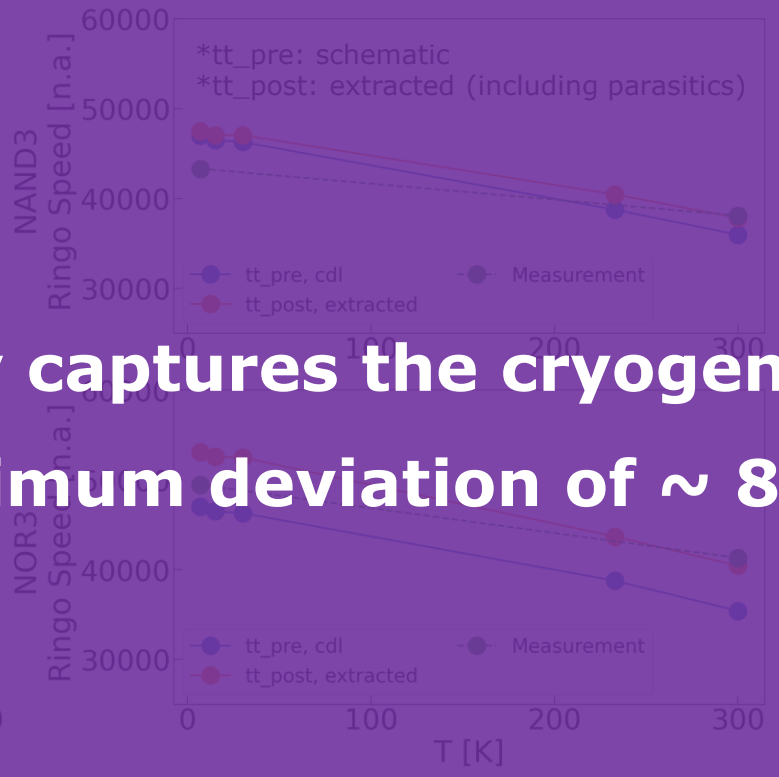


- NAND3: nMOS sensitive; NOR3: pMOS sensitive
- Multiple instances measured (Median values reported)
- Both NAND3 and NOR3 show ca. 15-20% speed-up at 7K

Model Validation

NAND3 & NOR3 Standard Cell Logic Gates



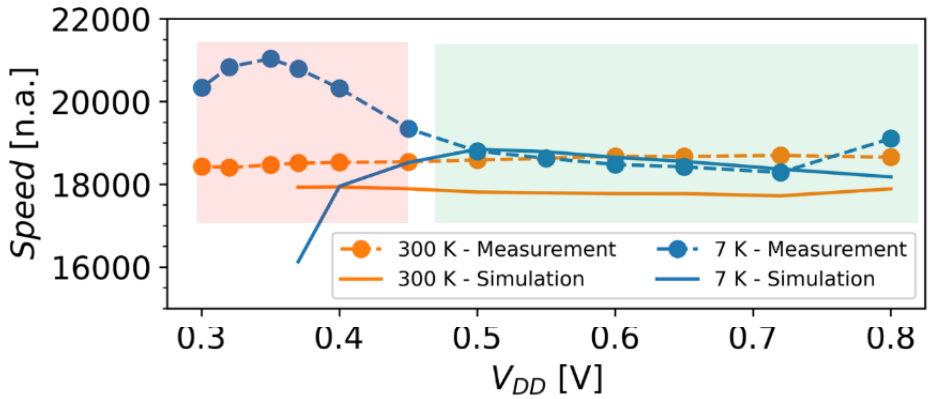


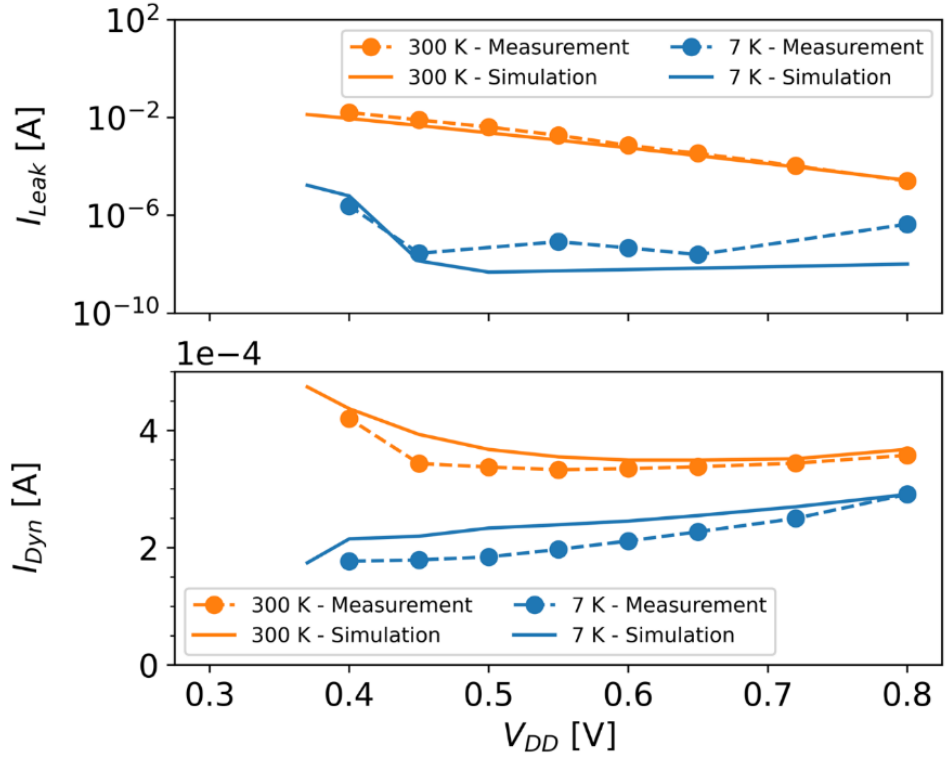
The cryogenic library captures the cryogenic speed-up with a maximum deviation of ~ 8%

- NAND3: nMOS sensitive; NOR3: pMOS sensitive
- Multiple instances measured (Median values reported)
- Both NAND3 and NOR3 show ca. 15-20% speed-up at 7K

Model Validation

INVX040: Adaptive Back-biasing





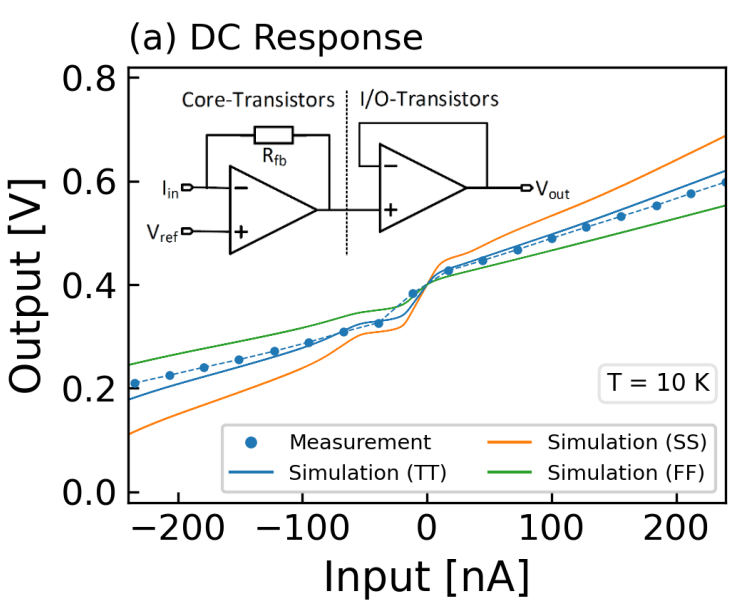
- ABB Calibration → Estimation of FBB
- Deviation < 0.5% down to 0.45 V
- Below 0.45 V → FBB approaches limits

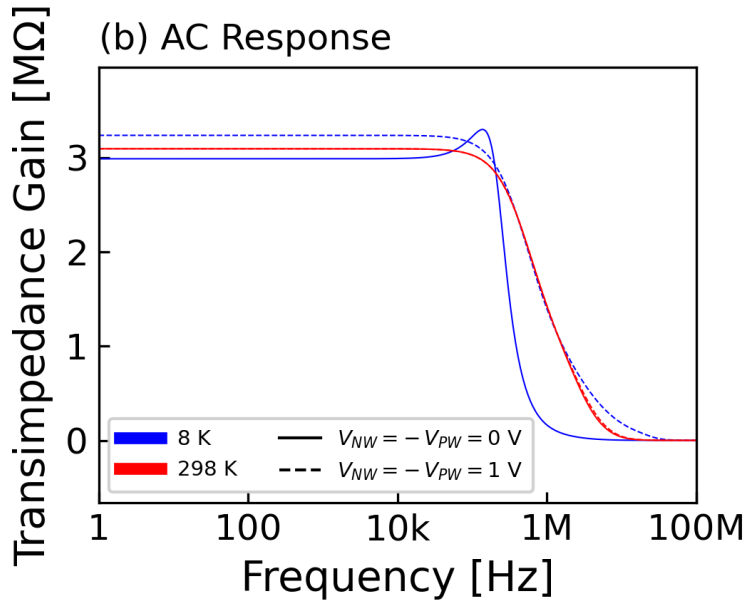
S. Höppner, *"Adaptive body bias aware implementation for ultra-low-voltage designs in 22FDX technology,"* IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 10, pp. 2159–2163, Oct. 2020.

Model Validation

Transimpedance Amplifier: DC and AC Response

- Qubit readout circuit front-end
- **TIA:** Core devices (thin-oxide);
  Buffer: I/O devices (thick-oxide)
- Feedback network: R_{ser} || TG
- DC Response at 10K within the corner simulations

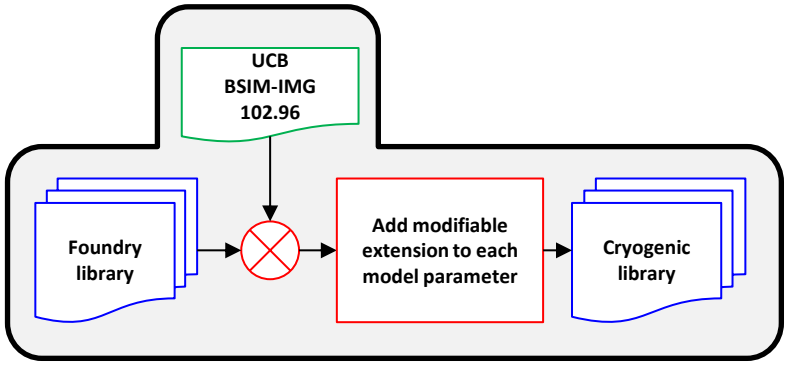


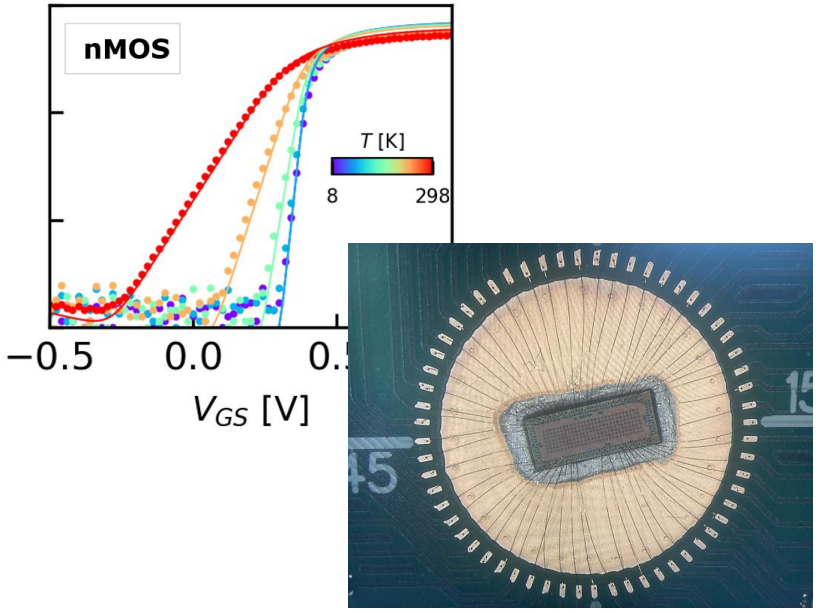


Summary

Key Takeaways:

- Cryogenic electronics → growing demand
- Lack of cryogenic models → bottleneck for designers
- Our approach:
  - Unified cryogenic library (T, W, L)
  - Validated on both device and circuit level
- Future considerations → Noise, mismatch, RF, etc.





Thank you!

With funding from the:

Federal Ministry of Research, Technology and Space

QSOLID

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Project Partners

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Racyics

Fraunhofer IPMS