Device aging simulations enabling circuit optimizations

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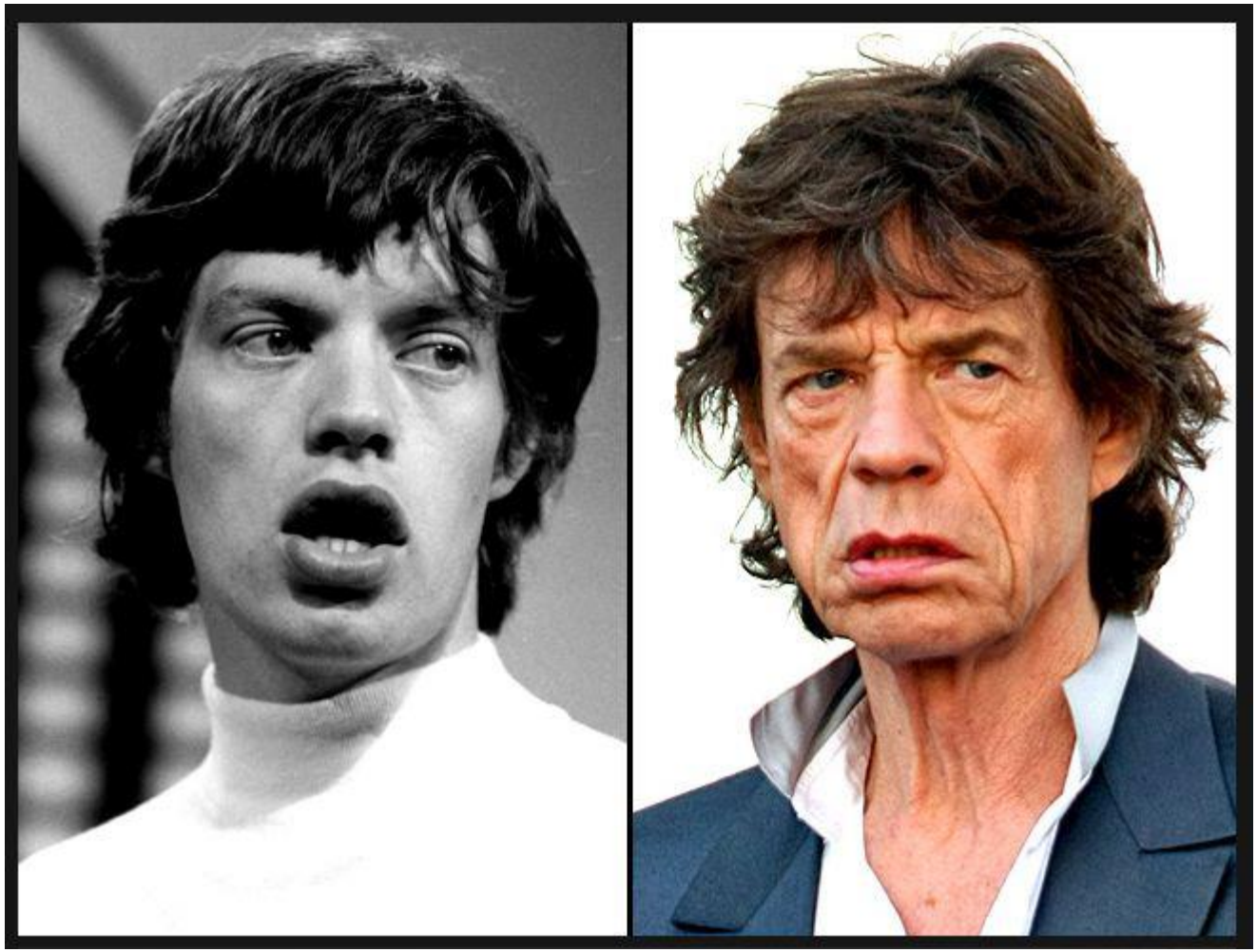
Aging – Critical Stress Conditions?



RESilient Integrated SysTems

RESilient
Integrated
SysTems

- Funded by: BMBF and European Union Catrene Program 01/2015-12/2017
- Motivation:
  - Electronic systems in cars planes require high reliability
    - New reliability aware design approaches and solutions are needed
  - Resist targets: New approaches for resilient integrated systems

Resilience:

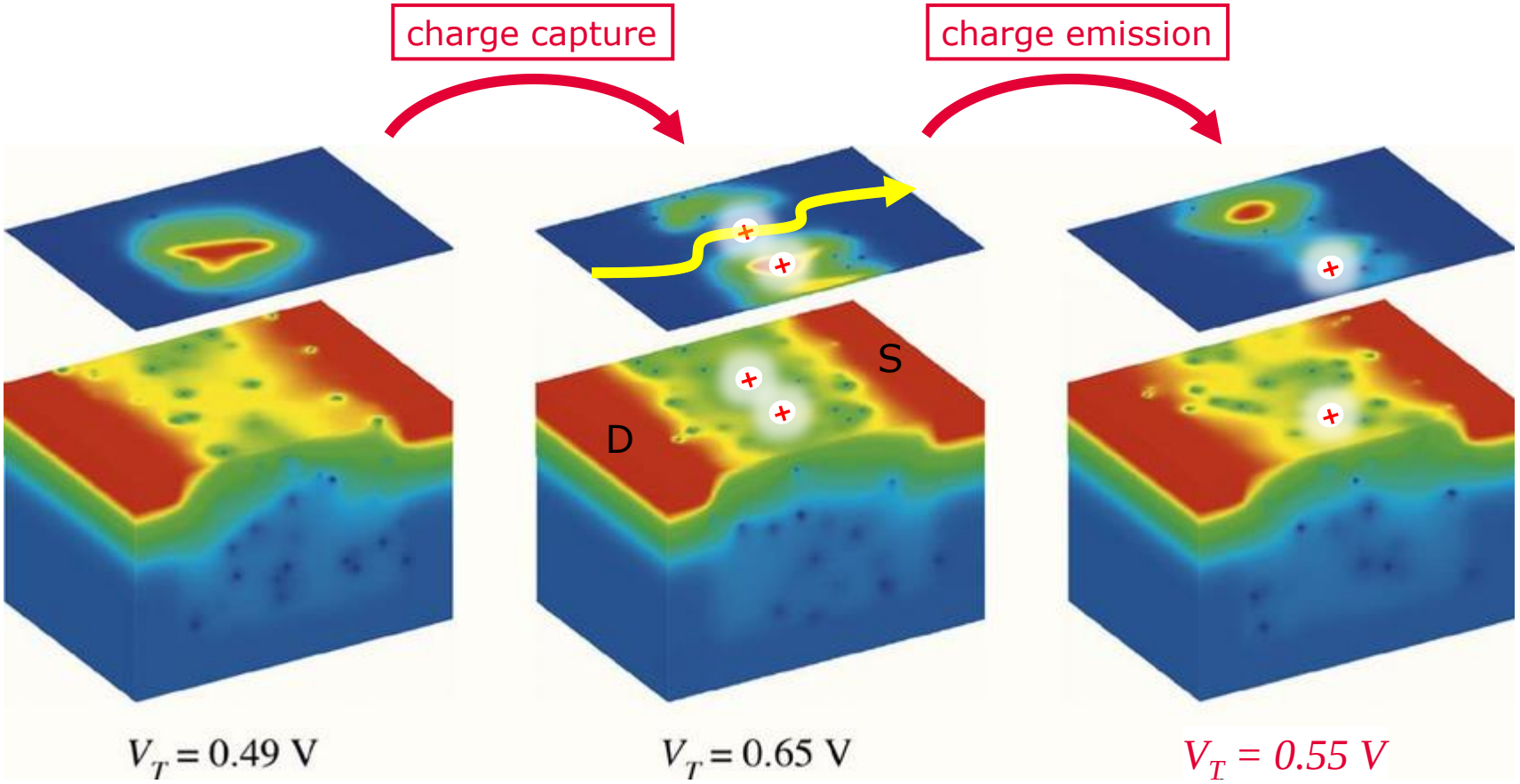
- The ability of a system or component to resist a certain load change **by adapting** its initial stable configuration to the new situation

RESIST Project Partners

Agenda

1. Worst Case Aging Models
2. Variability
3. BTI Recovery
4. Circuit Simulations
5. Outlook and Cooperation

Electrical stress generates charged traps

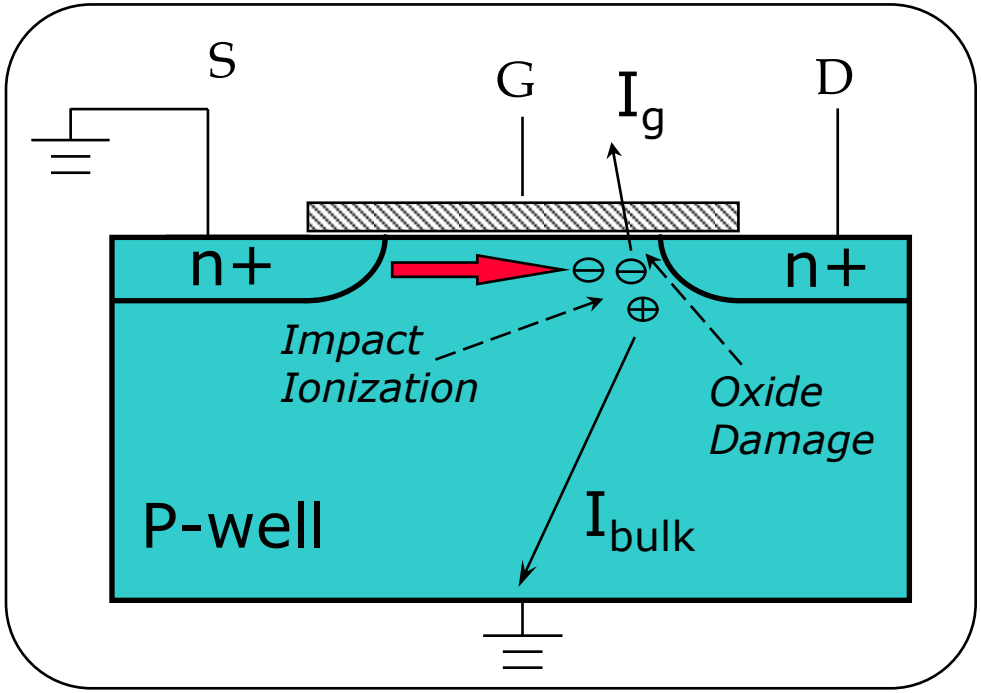


A. Asenov et. al., *Simulation of Instrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs*, IEEE Transactions on Electron Devices 50(9), 2003

BTI and HCI Impact on Device Behavior I

NMOS Hot Carrier Injection (HCI) Effect

- E_{max} at drain corner causes hot carrier generation
- Hot carriers cause I_{sub}, I_{gate} and oxide damages



Degradation f(T,V_{DS},V_{gs})
Doesn't recover

Parametric shift

› Increase of V_{th}

› Decrease of g_m

› Increase of I_{off}

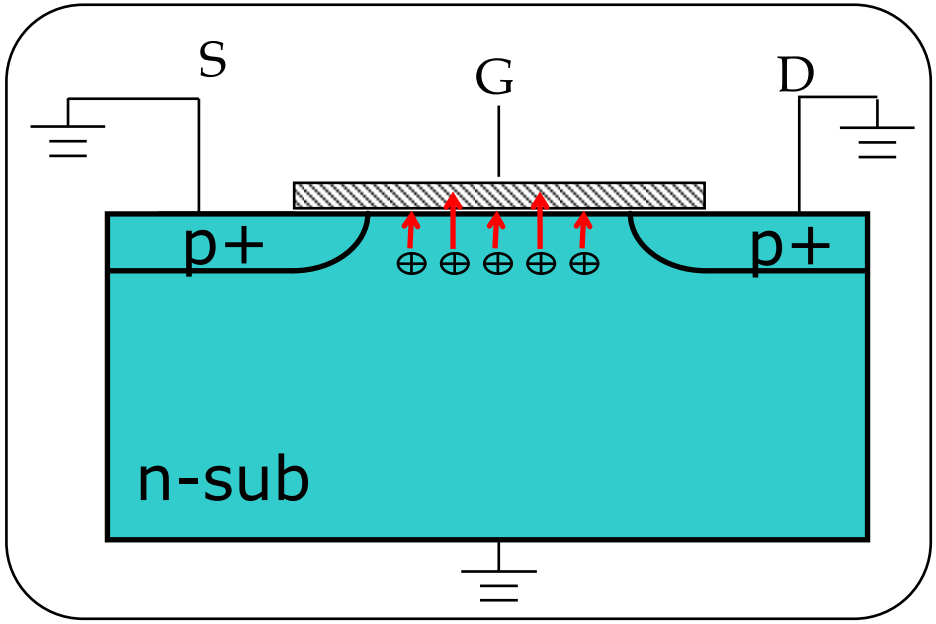
› Decrease of I_{dsat}

BTI and HCI Impact on Device Behavior II

Negative Bias Temperature Instability (NBTI) Effect

Positive Bias Temperature Instability (PBTI) Effect

- Hydrogen-silicon bond (Si-H) is broken
- Hydrogen is trapped into the oxide → interface trap



Degradation f(T,V_{GS}) Recovers

Parametric shift

› Increase of V_{th}

› Decrease of g_m

› Increase of I_{off}

› Decrease of I_{dsat}

Worst-Case Aging Models – Main Features 1

BTI - Basic Set of Generic Equations for ΔV_{th} and $\Delta I/I_o$ Contributions

$$\text{(BTI)} \quad < \mathrm{L}(V_{gs}) \cdot C \cdot e^{\left\{\frac{B_V}{\pm|V_{gs}|} + \frac{-E_a}{(k_B \cdot T_{op})} + \frac{B_L}{L_{des}}\right\}} >_t \cdot (t_{op})^n$$

HCI - Basic Set of Generic Equations for ΔV_{th} and $\Delta I/I_o$ Contributions

$$\text{(HCI)} \quad < \mathrm{L}(V_{gs}, V_{\mathrm{ds}}) \cdot C \cdot e^{\left\{\frac{B_V}{\pm|V_{ds}|} + \frac{-E_a}{(k_B \cdot T_{op})} + \frac{B_L}{L_{des}}\right\}} \cdot A(|V_{gs}|) >_t \cdot (t_{op})^n$$

- ± depends on device type: + for nmos, - for pmos
- V_{gs} and V_{ds} are time dependent transistor terminal voltages
- Boltzmann term $exp\left\{\frac{-E_a}{(k_B \cdot T_{op})}\right\}$ for temperature dependency
- $A(|V_{gs}|)$ models the V_{gs} dependency by using fit polynomial of low degree (n=6)
- $(t_{op})^n$ describes extrapolation to final long-term aging time, typically t_{op}= 10y
- $<\ldots>_t$ is the weighted summation over simulated stress time
- L(…) are limiting functions required for numerical reasons

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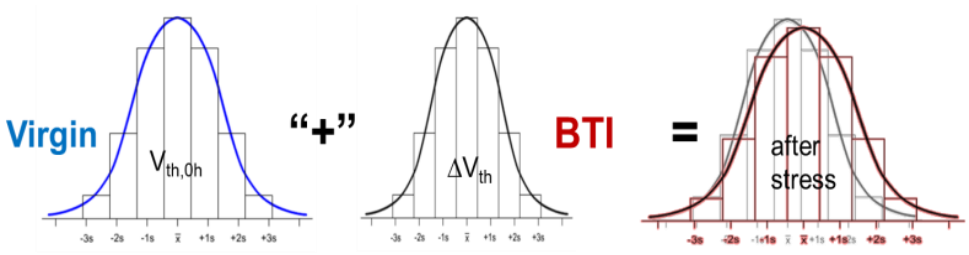
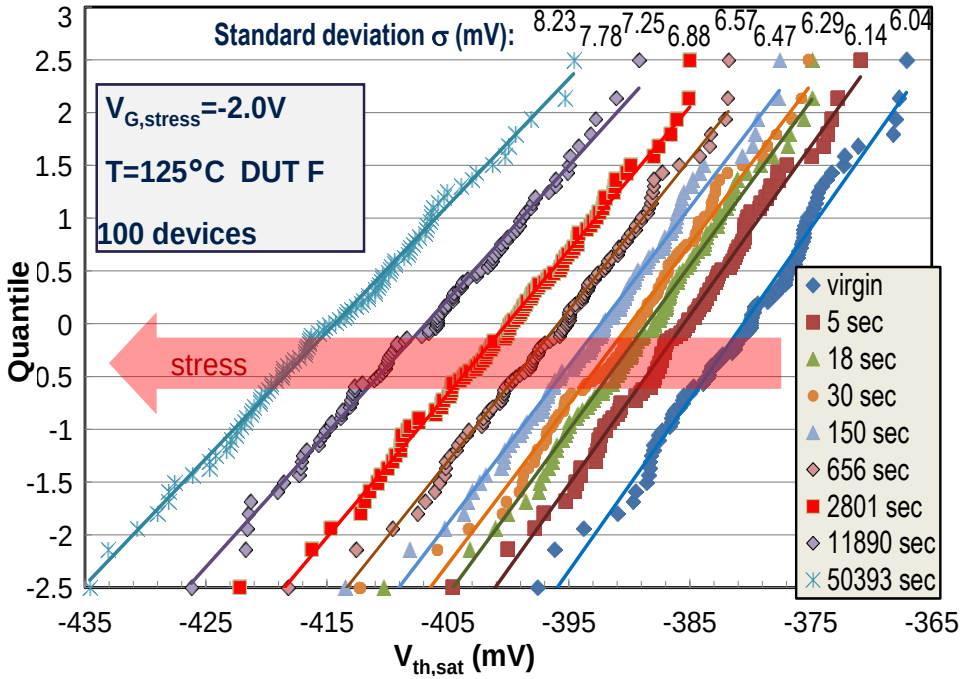
Distribution of the threshold voltage after BTI





Distribution of V_{th} after NBTI stress

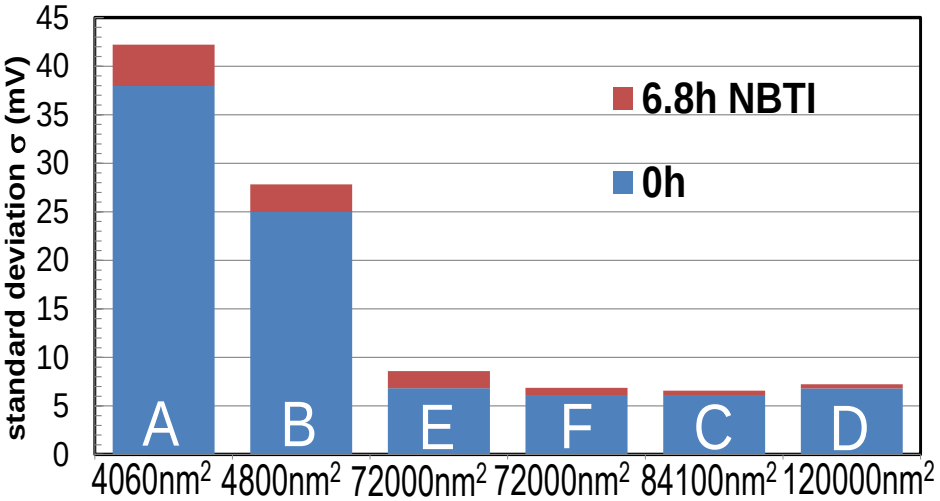
→convolution of:

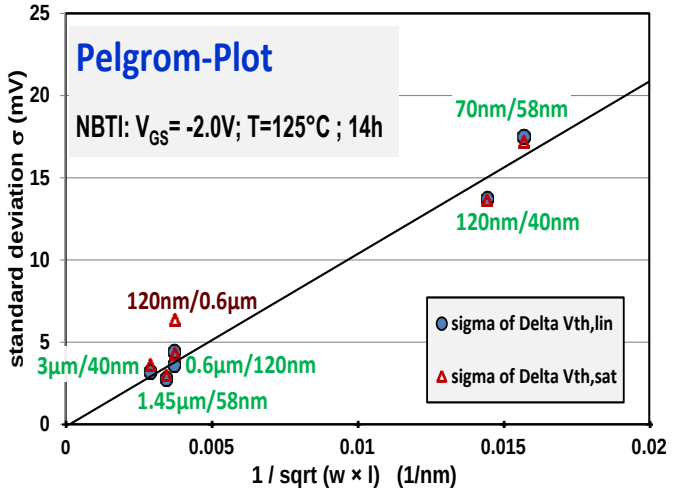
- Distribution of the virgin devices
- Distribution of the NBTI degradation

Distribution of the threshold voltage after NBTI $V_{G,stress}$=-2.0V. The variability increases with longer stress times.

Schlünder C.; Berthold J.M.; Hoffmann M.; Weigmann J-M.; Gustin W. and Reisinger H.; "A New Smart Device Array Structure for Statistical Investigations of BTI Degradation and Recovery", IEEE International Reliability Physics Symposium (IRPS), April 12-14, Monterey, California, 2011, pp. 56-60

Impact of BTI Variability



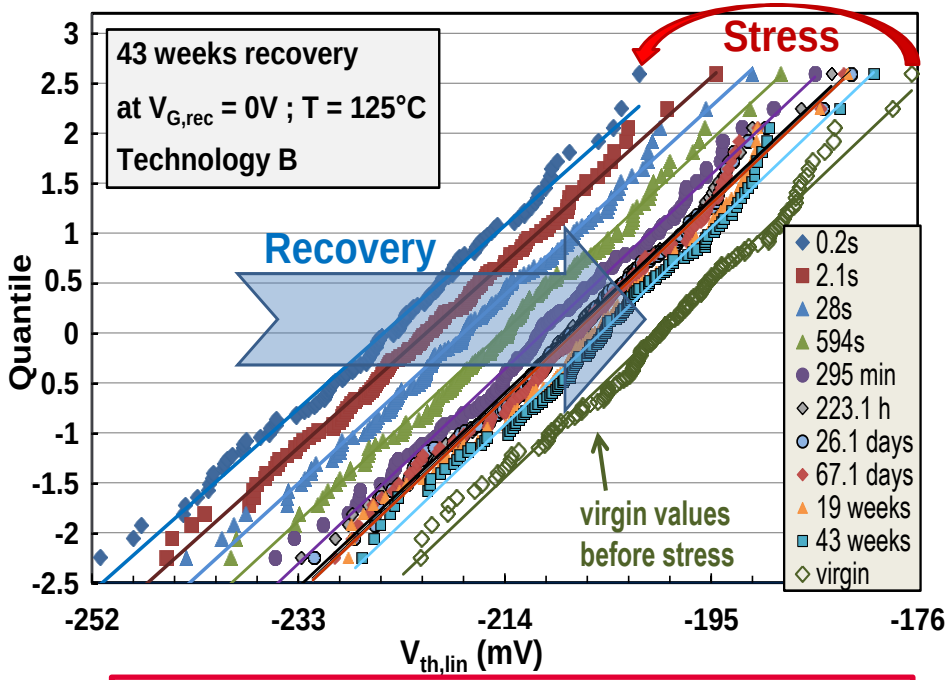


Standard deviation s of $V_{th,lin}$ of the transistors with different areas (nm²) before and after stress

Pelgrom plot of the standard deviations s of the stress induced $V_{th,lin}$ and $V_{th,sat}$ shift. Like the s of zero hour parameters also the s of the V_{th} shift is proportional to ~1/sqrt(w×l).

Schlünder C.; Proebster, F.; Berthold, J.; Gustin, W.; and Reisinger, H.; "Influence of MOSFET geometry on the statistical distribution of NBTI induced parameter degradation", Final Report IEEE International Integrated Reliability Workshop (IRW), S. Lake Tahoe, CA, Oct. 11-15, IRW, pp. 81-86, 2015

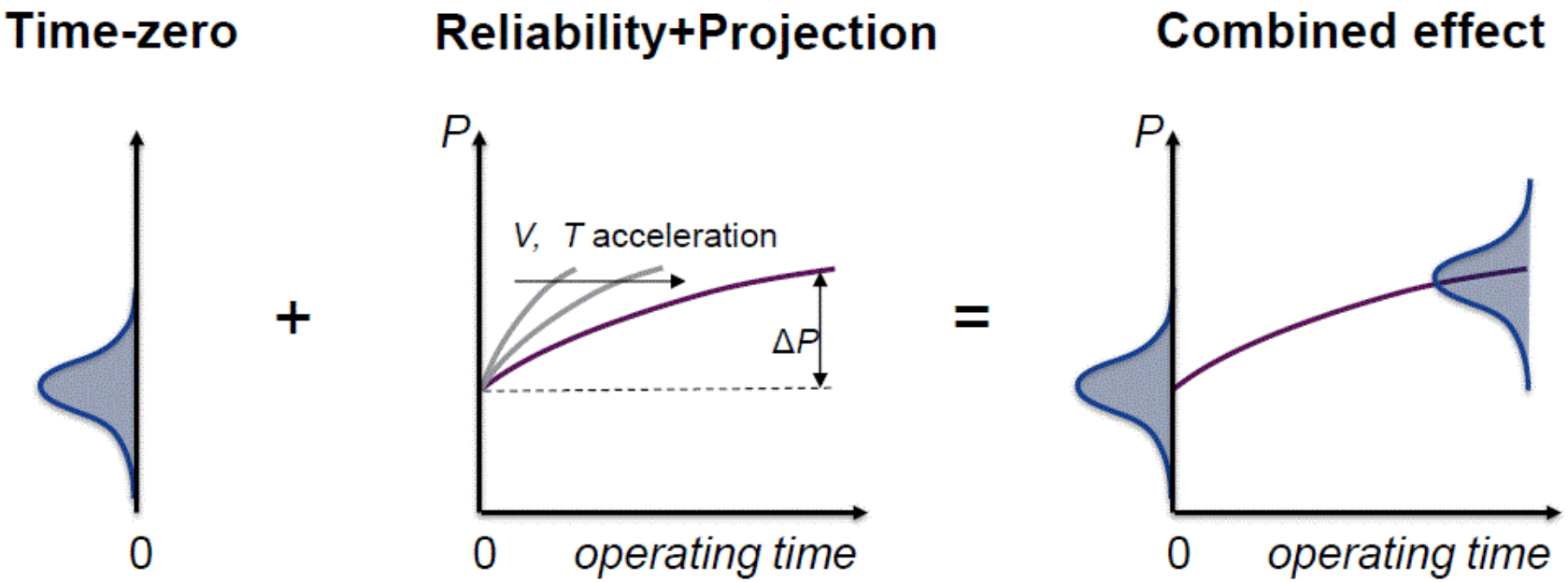
Distribution of the threshold voltage after recovery



Distributions of the threshold voltage after recovery up to 43 weeks at T=125°C. Both the V_{th} values and the variability recover in direction of the virgin values (rightmost curve).

Schlünder C., Berthold J., Proebster F., Martin A., Gustin W. and Reisinger H.; Degradation and Recovery of variability due to BTI “, ESREF 2016

Present status of circuit aging simulations



Neglection of BTI induced variability due to:

- 0h variability dominates variability
- BTI induced variability recovers together with the BTI degradation

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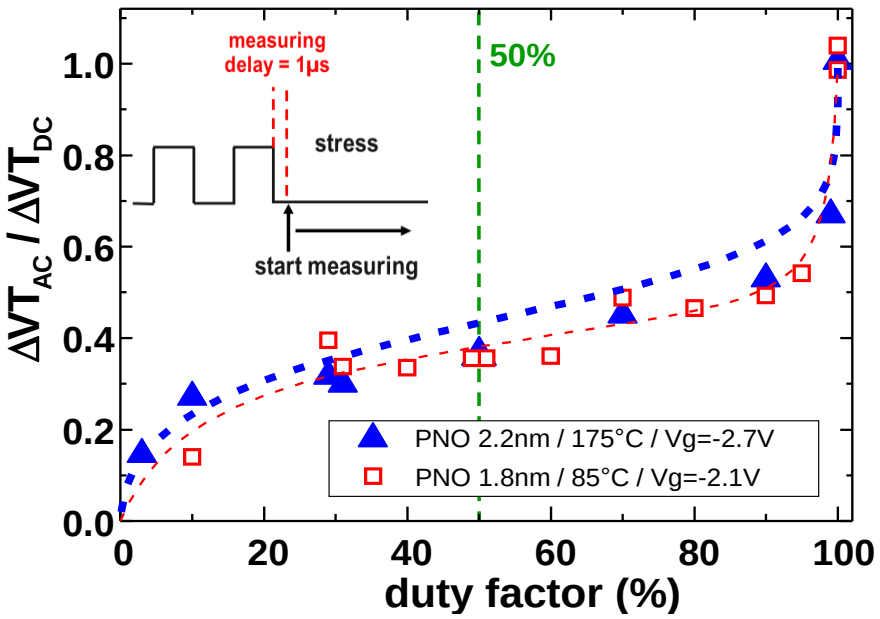
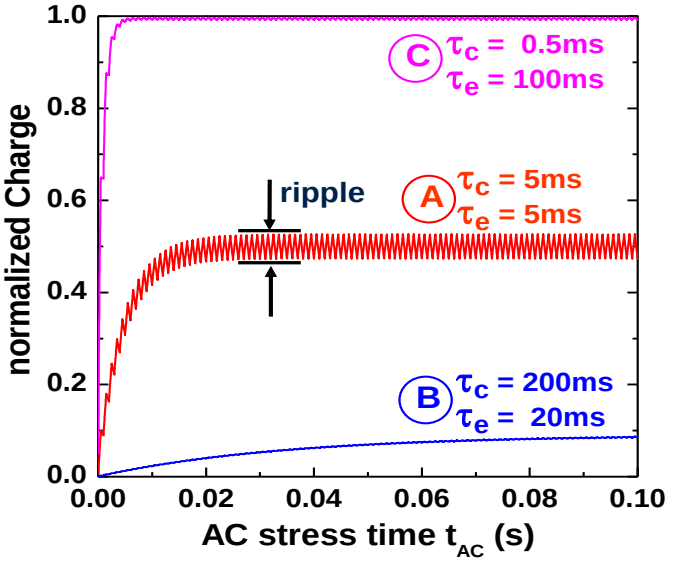
Can we just neglect Recovery of BTI?





'S-Curve': BTI degradation as a function of the duty-cycle of a rectangular signal (f=100 kHz) applied to the gate for 10ks.

Some examples of charging curves of defects with different charging time constants $\bar{\tau}$ and different ratios τ_e/τ_c

Neglecting recovery is more than 2 times over-estimating the degradation after BTI for a duty cycle of 50%

Integrating Recovery into Circuit Simulations

- Why it is so complicated to consider BTI recovery for circuit simulations?
  - Recovery depends on the full device history
    - real-time simulations necessary
    - No simple extrapolation possible
  - Physical models: Charging/discharging of every single trap
    - Very time-consuming, huge calculation effort
  - Simplifications: E.g. Fraunhofer Gesellschaft approach
    - But: Still time-consuming and high measurement effort
    - New approach developed: Publication will follow soon

Physics-based compact modeling

Physics-based Compact Modeling of NBTI for Analog and Digital Circuit Design

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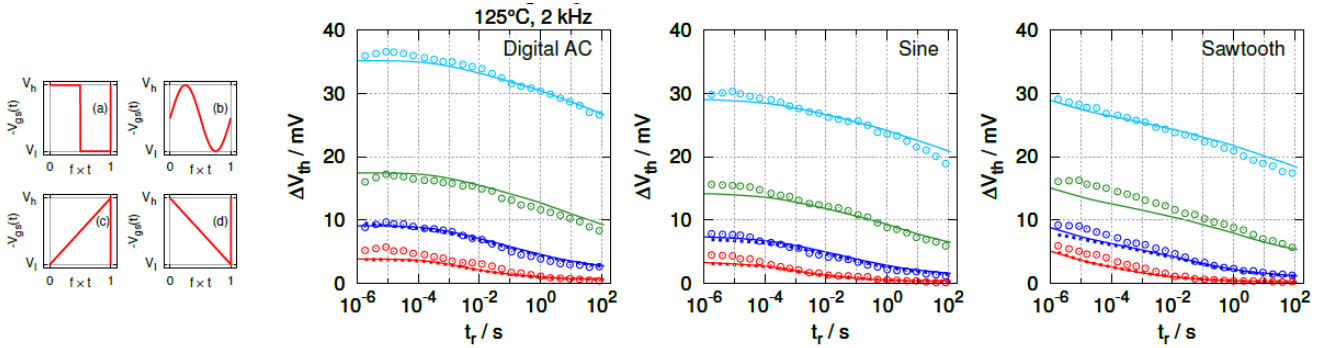

Fig. 4: MSM experiments with analog stress patterns. ***Left:*** During the MSM stress phase we periodically apply one of the four stress patterns: digital AC, sine, sawtooth, inverse sawtooth (a to d). The stress voltage oscillates between the values $V_l \leq -V_{gs}(t) \leq V_h$. ***Right (three plots):*** The MSM setup uses a sequence of four stress intervals of duration 10^{-2}s, 10^{0}s, 10^{2}s and 10^{4}s (bottom-up in the plots) and traces the respective recovery curves. We compare experimental data (symbols) to TCAD results (thick dashes) and to compact model results (solid line). Due to numerical complexity, TCAD data so far is only available for the two smaller stress times. The difference between TCAD and compact model results is often hardly noticeable. Most importantly, the theoretical predictions and experimental measurements are in good agreement. The consistency of experimental and compact model data at large stress times validates the compact model's extrapolation method to large stress times also from a practical point of view. The present setup applies a stress frequency of 2kHz, a temperature of 125°C and stress voltages between $V_l = 0.5$V and $V_h = 2.8$V.

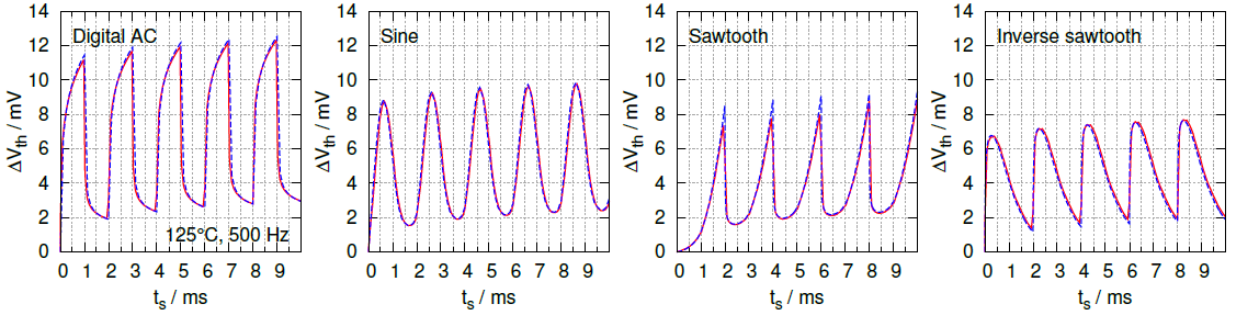

Fig. 5: Threshold voltage shift during analog stress. We compare TCAD (dashed line) to compact model (solid line) results on $\Delta V_{th}(t)$ during the first five periods of the stress phase. For all four stress patterns, both models are in excellent agreement. The simulations use a stress frequency of 500Hz, a temperature of 125°C and voltage values $V_l = 0.5$V and $V_h = 2.8$V.

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Device Aging Simulation – Design Flow Building Blocks

Multi-step Spice simulation sequence

1. Fresh Simulation
2. Stress Simulation
3. Aged Simulation

deploying

- A Spice simulation engine
- Add-on worst-case aging models
- assertions for stress integration
- alter concept for instance specific
- Avenue/ADE-XL test sequence as flow control engines

Worst-Case/Realistic Stress Conditions

Main Impact Factors

- Aging Model Dependencies (VDS, VGS, Temperature)
- Analog Circuit Modes (Circuit Duty Cycles, Sleep Modes, Start-up Phase)

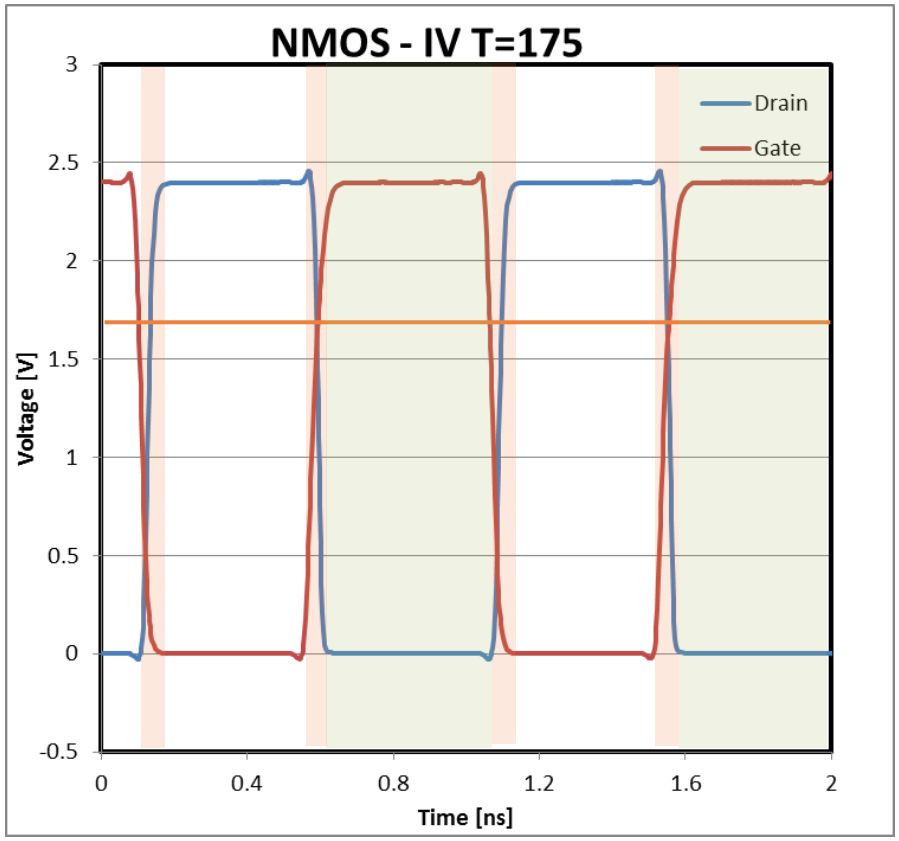
Temperature Implications

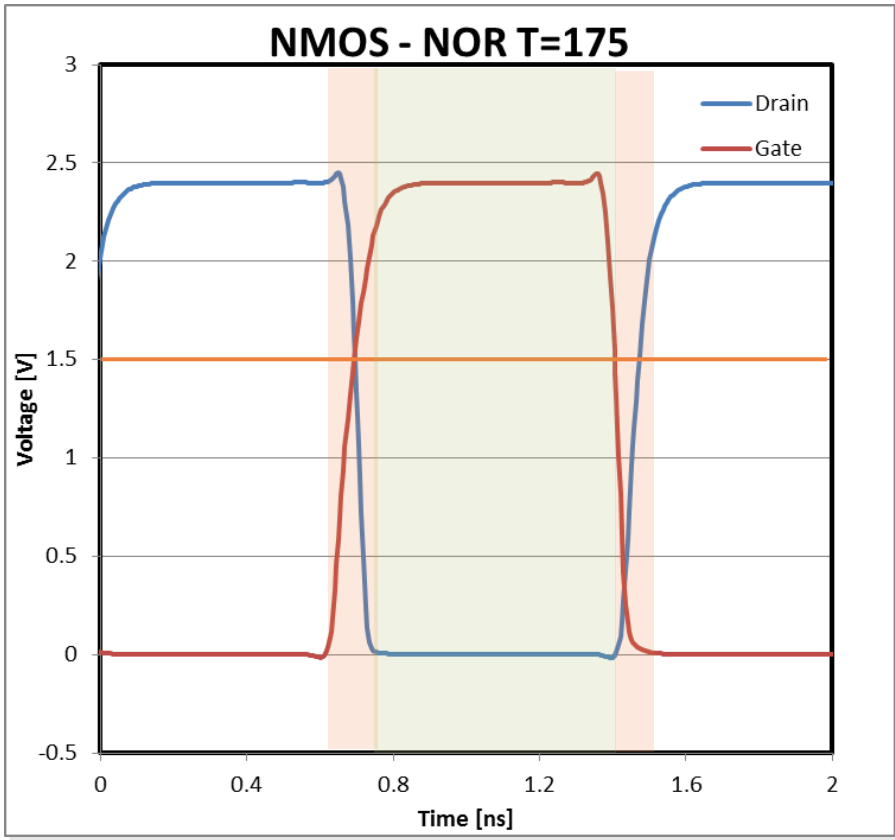
- local temperature increase
- mixed temperature stress profiles
- worst-case temperature condition for single device dependent on aging effect (BTI, HCI) and device type, but circuit contains always a mixture

Stress Scenario Discussion

- worst-case vs. realistic stress pattern
- suppression of start-up simulation phases
- handling of complex multi-circuit mode stress pattern

Comparison IV, NOR



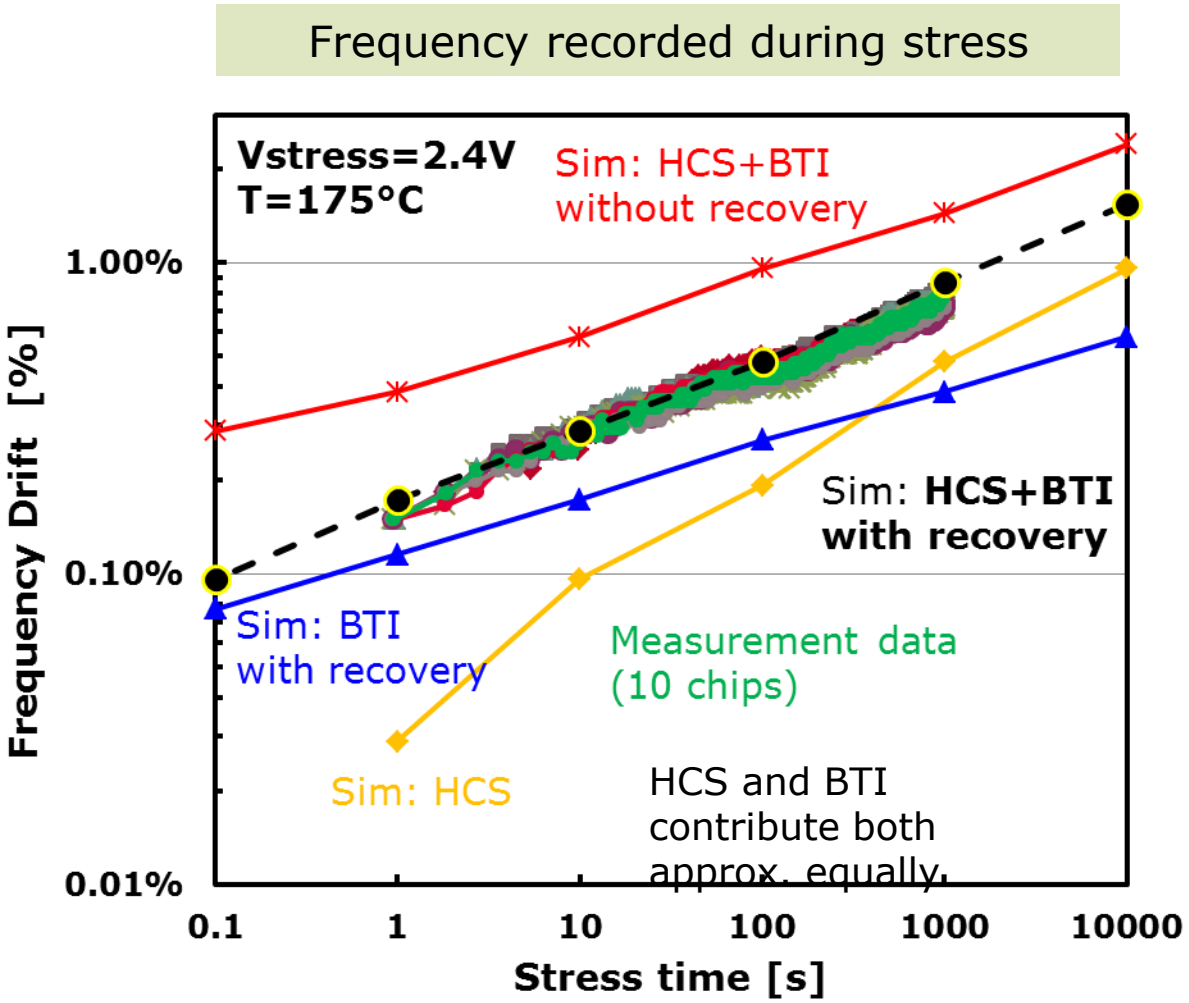


BTI

HCS

For the NOR ringo, HCS should play a less dominant role, than for the IV due to the exponential drain voltage dependence

Results: Inverter Ringo, T=175°C, Vdd=2.4V



Outlook & cooperation

- Efficient usable worst case models were developed
- Variability is currently neglected (0h hour variability has been shown to be bigger than aging-induced variability)
- Recovery is no longer neglected – Publication will follow soon
- Relevant circuit examples (Ring- and Relaxation-Oscillators) are further studied

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