Compact Modeling of Nanomagnetic Logic Devices and Circuits

Markus Becherer, Simon Mendisch, Gražvydas Žiemys

Technische Universität München, Fakultät für Elektrotechnik und Informationstechnik, (D)

Digital computation with ferromagnetic islands is one promising technology in beyond CMOS device research. In the physical implementation of the so-called perpendicular Nanomagnetic Logic (pNML), it provides intrinsically non-volatile computational states, atto-joule dissipation per bit operation and estimated data throughputs which could be competitive with state-of-the-art high performance CMOS CPUs. In this work, both a 2D planar implementation of pNML and the path to monolithically 3D integrated systems is discussed. Rather than CMOS substitution, additional functionality is added by a co-processor architecture as a prospective back-end-of-line (BEOL) process. [1] [2] [3]

For modeling of Boolean gates and circuits, a three-step approach is found to be well suited. First, micro-magnetic finite element simulations provide insight in the physics of magnetization reversal dynamics and domain-wall propagation of single pNML islands and devices. Second, switching distributions of magnets are extracted and simplified behavioral models are formulated. Third, the parameterized compact models form the basis of Verilog-A simulations, utilizing the well-known strength of abstraction in system level simulation. [4] [5]

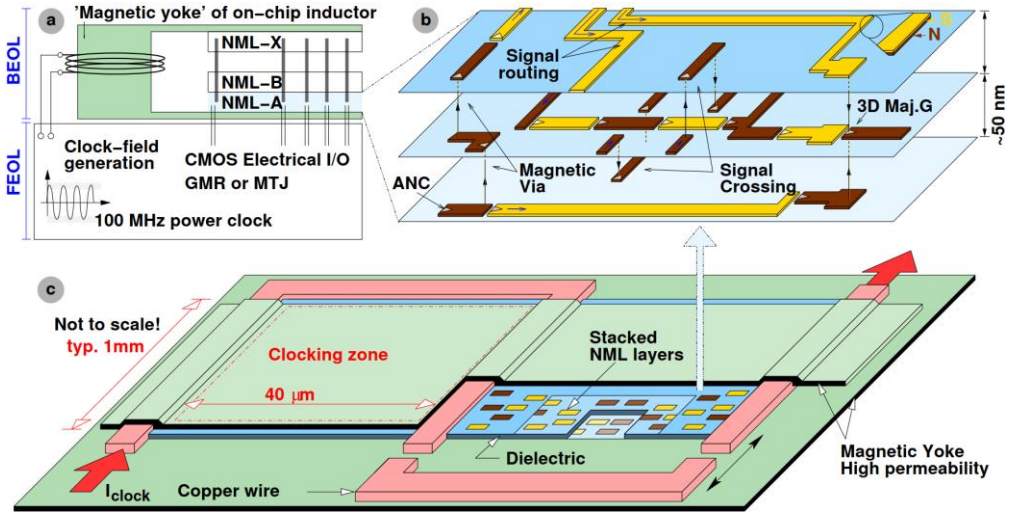

Fig. 1 a) The vision of a Co-Processing unit fabricated in the Back-end of-line. b) Exploded view a monolithically 3D integrated layers of Nanomagnetic logic devices. c) On-chip inductor forming zones for a global magnetic field-clock. Graph adapted and reprinted with permission from [3].

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[4] G. Žiemys, A. Giebfried, M. Becherer, I. Eichwald, D. Schmitt-Landsiedel, and S. Breitkreutz v. Gamm. Modeling and simulation of nanomagnetic logic with cadence virtuoso using verilog-a. *Solid-State Electronics*, 125: 247–253, 2016. doi: 10.1016/j.sse.2016.05.013. Extended papers selected from ESSDERC 2015.

[5] G. Žiemys, A. Giebfried, I. Eichwald, D. Schmitt-Landsiedel, M. Becherer, and S. Breitkreutz-v. Gamm. Modelling and Simulation of Nanomagnetic Logic with Cadence Virtuoso using Verilog-a. In *45th IEEE European Solid-State Device Research Conference (ESSDERC)*, pages 97–100, September 2015. doi: 10.1109/essderc.2015.7324722.