Compact Modeling at Infineon

MOS-AK in Munich
2018-03-13

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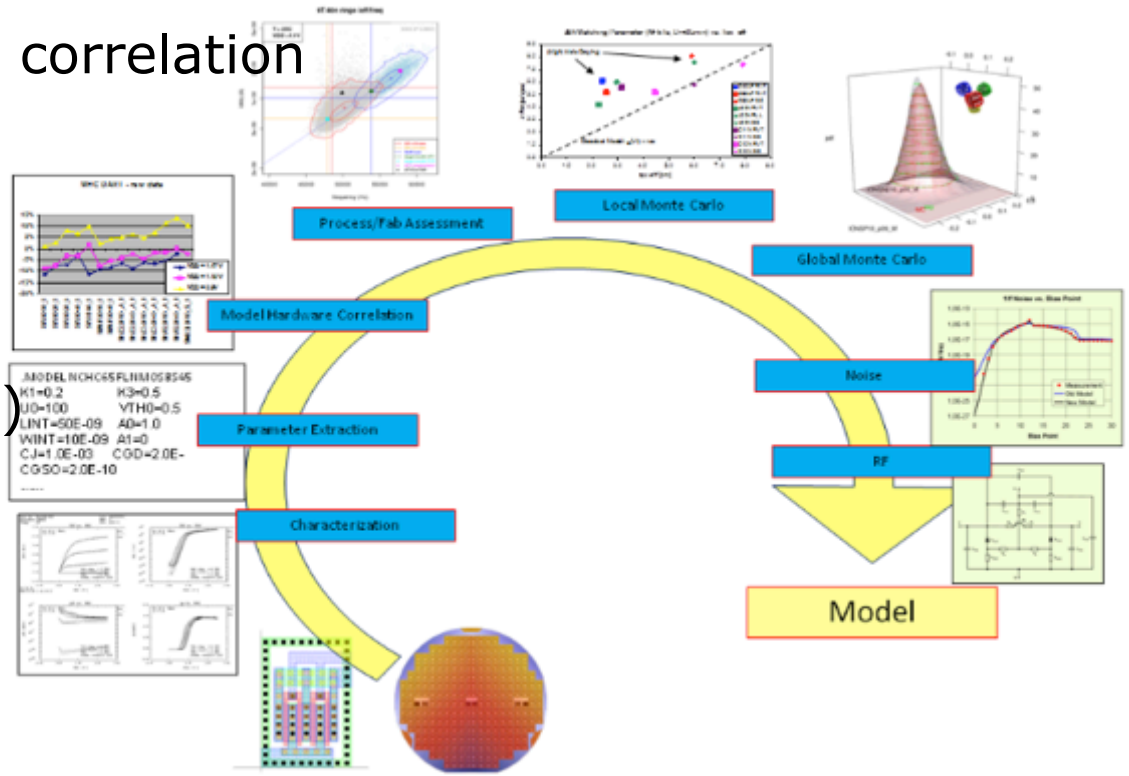
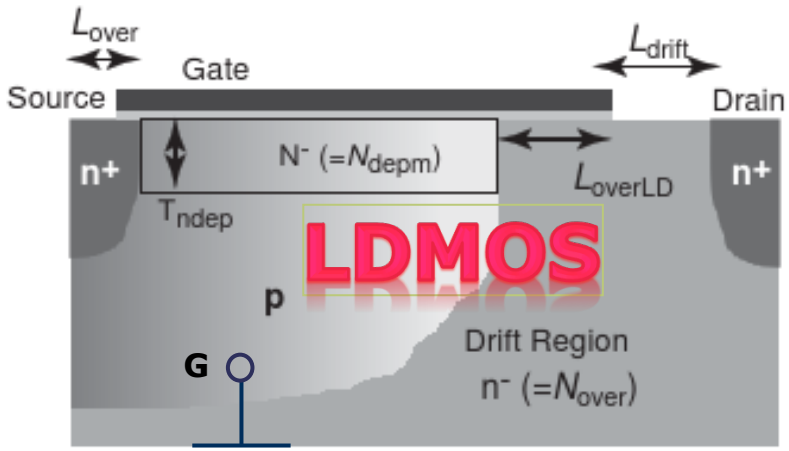
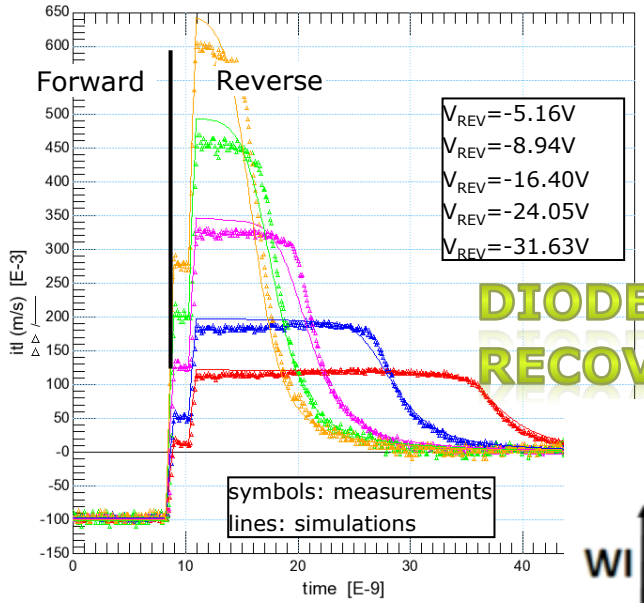
Modeling in Central Department
MDL: **Mo**d**e**l**l**ing

- ✓ Responsible for CMOS incl. embedded flash and RF technologies
- ✓ Technology assessment (together with other departments)
- ✓ Technology target setting (together with other departments)
- ✓ Modeling (nom / variations (MonteCarlo) / corner)
- ✓ MHC = model hardware correlation
- ✓ RF-modeling
- ✓ Noise-parameter
- ✓ BEOL-extraction (metallization parasitics)
- ✓ Preparation for design flow usage

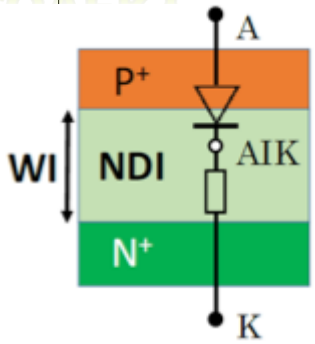


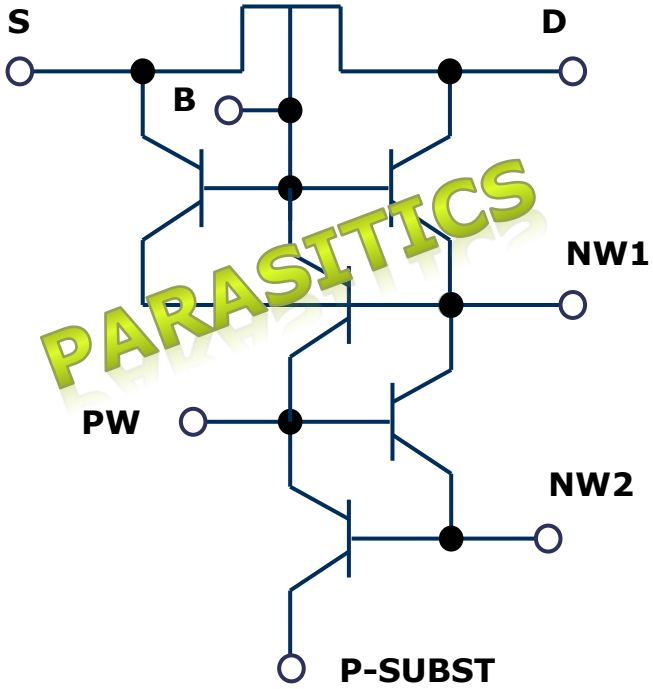
Automotive Power Modeling Group





DIODE REVERSE RECOVERY

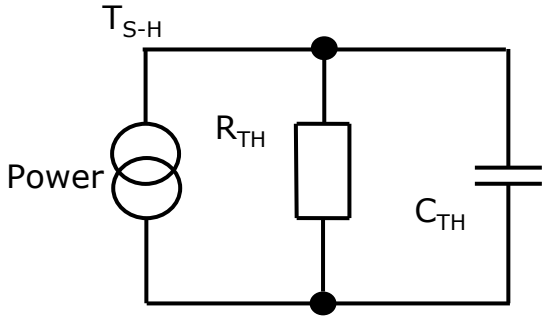




PARASITICS

Compact Models

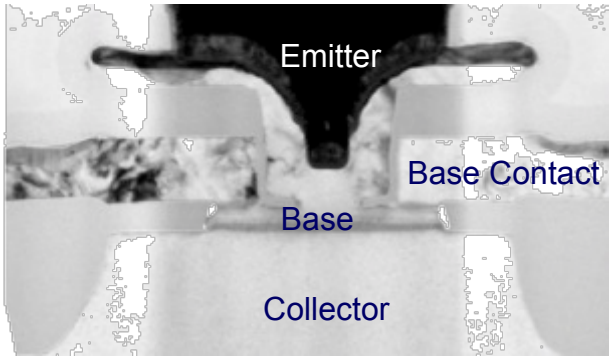
- HiSIM-HV
- BSIM3/4/SOI
- VBIC, BJT
- JFET
- Sub-circuits
- VerilogA Models

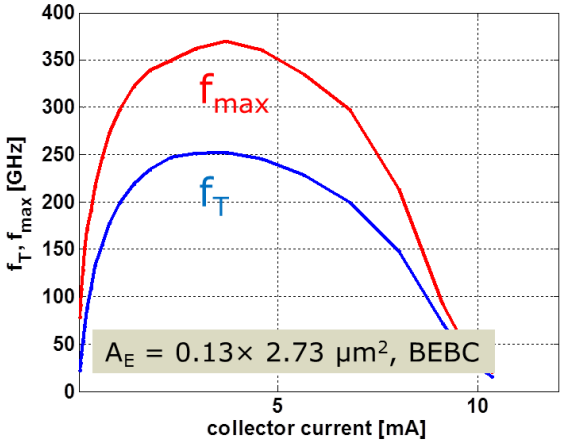


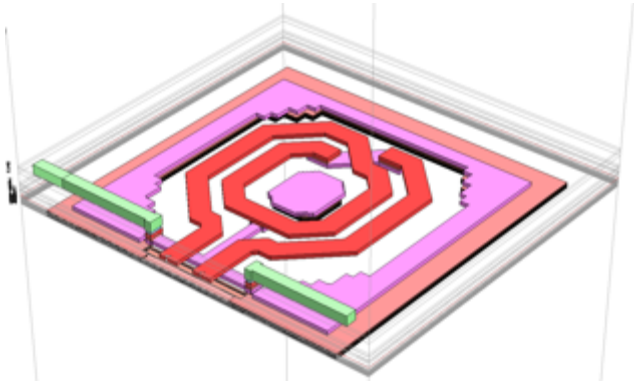
Self-Heating

Autom. S&C Radar Tech. Modeling Group

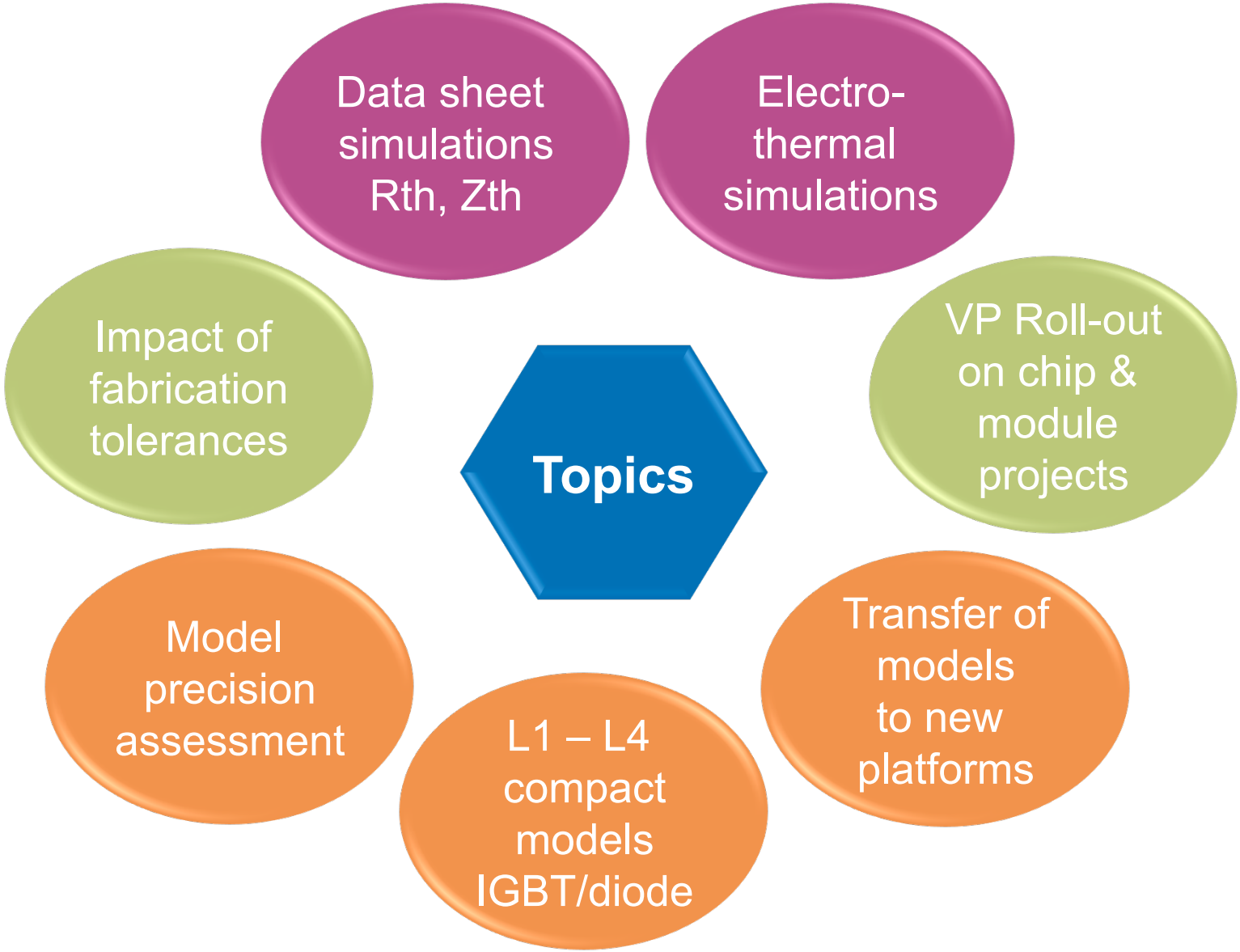
- In radar technology group, together with technology and RF circuit design experts
- Topics:
  - Active devices (SiGe HBTs: HICUM, BJT)
  - Passive devices: inductors, transformers, transmission Lines
  - Crosstalk mitigation, RF design methodology



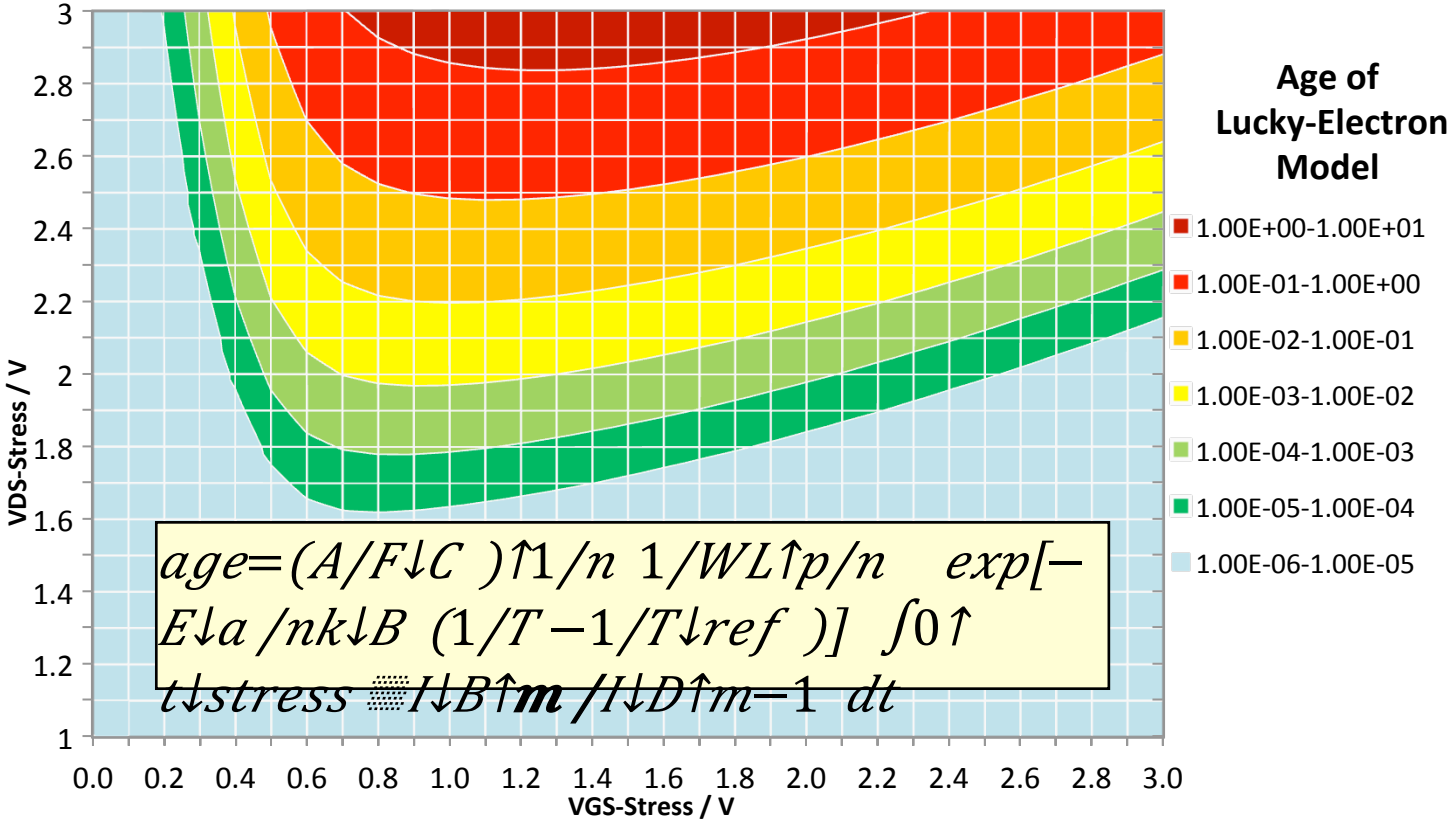




Virtual Prototyping Group (IGBT)



Special Topic: Aging Simulation



CMC workgroup **Reliability Equations** is looking for candidates of aging equations for MOS, LDMOS and Bipolar. Effects like Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), etc.

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Infineon