

Spring MOS-AK Workshop March 13, 2018 Munich

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Over two decades of MOS-AK in brief

MOS-AK R&D Association

- 17 subsequent MOS-AK Compact Modeling Workshops
at ESSDERC/ESSCIRC Conferences
- 29 International MOS-AK Compact Modeling Workshops
in Europe, USA, China and India (plans for Brazil)
- 17 special Compact Modeling Sessions
at MIXDES Conference
- 50+ active sponsors and technical program promoters
- 350+ MOS-AK technical CM papers and posters
(available on line www.mos-ak.org)
- 4 modeling MOS-AK modeling books
<http://www.mos-ak.org/books/>



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MOS-AK: Munich Compact Modeling Events

- ❑ MOS-AK Munich **2018**
 - ❑ organized by Klaus-Willi Pieper, Infineon
 - ❑ http://www.mos-ak.org/munich_2018/

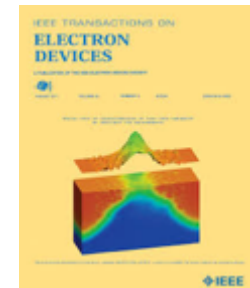
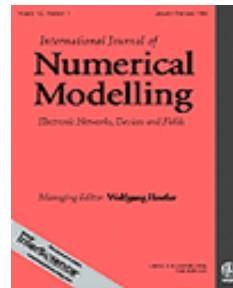
- ❑ MOS-AK Munich **2013**
 - ❑ At TUM with the technical program cosponsorship by the IEEE EDS Chapter Germany
 - ❑ http://www.mos-ak.org/munich_2013/

- ❑ MOS-AK/ESSDERC/ESSCIRC Workshop **2007**
 - ❑ <http://www.mos-ak.org/munich/>

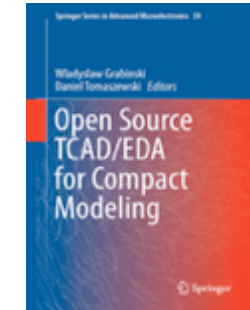
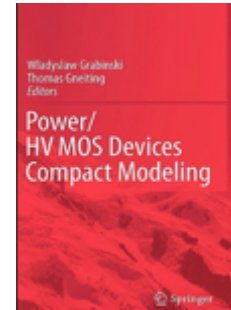
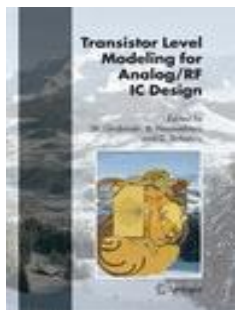
- ❑ MOS-AK Munich **2001**
 - ❑ organized by B. Lemaitre, Infineon
 - ❑ http://www.mos-ak.org/munich_2001

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MOS-AK: Recent Publications



Special Compact Modeling Issues



Special Compact Modeling Books



TRACK4: Compact Modeling of Devices and Circuits

www.mos-ak.org

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MOS-AK: Call for Papers



International Journal of High Speed Electronics and Systems (IJHSES)
MOS-AK Advances in the Compact/SPICE Modeling and its Verilog-A Standardization
<https://www.worldscientific.com/page/ijhses/callforpapers01>
Submission deadline: April 30, 2018 Publication date: January 2019
Co-Editors-in-Chiefs: Wladek Grabinski (MOS-AK) Benjamin Iñiguez (URV (SP))
Guest Editors: Jean-Michel Sallese (EPFL (CH)) Daniel Tomaszewski (ITE (PL))



Call for papers for a Special Issue of **IEEE TED** on **Compact Modeling for Circuit Design**
<http://sedemos.blogspot.ch/2017/12/special-issue-ted-on-compact-modeling.html>
Submission deadline: April 30, 2018 Publication date: June 2018
The main objective of this dedicated special issue is to engage Electron Devices Community in a serious discussion with their scholarly contributions specifically focused on solving major challenges in the broad area of compact device modeling for circuit design.



TRACK4: Compact Modeling of Devices and Circuits
<https://www.esscirc-essderc2018.org/esscirc-call-for-papers>
All submissions must be received by 3 April, 2018

www.mos-ak.org

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MOS-AK Technical Presentations

MOS-AK Morning Session

T_0 MOS-AK Workshop Opening

Klaus-Willi Pieper; Infineon Technologies AG, Neubiberg, (D)

Wladek Grabinski; MOS-AK (EU)

T_1 Overview of the Compact Modeling at Infineon

Klaus-Willi Pieper

Infineon Technologies AG, Neubiberg, (D);

T_2 Advanced Fast on-wafer Low-frequency Noise

Measurement with High Resolution, Wide Bandwidth and Large Biasing Current Range

James Ma, Lianfeng Yang and Zhihong Liu

ProPlus Design Solutions Inc. (US)

T_3 Advances in Statistical Compact Modeling

Dr. Volker Gloeckel* and Dr. Elmar Gondro**

*MunEDA; **Infineon Technologies

T_4 Compact Modeling of Nanomagnetic Logic Devices and Circuits

Markus Becherer, Simon Mendisch and Grazvydas Ziemys

Technische Universität München (D)

P_1 Devices for Nanomagnetic Logic

Gražvydas Žiemys

Technische Universität München (D)

T_5 Modelling Emerging Devices through EU ASCENT Network

Paul Roseingrave

Tyndall National Institute (IE)

MOS-AK Panel: Compact Model Licensing

Peter Lee; CMC Chair

MOS-AK Afternoon Session

T_6 How Is CMC Standard Model Implemented and Verified In Simulator?

Jushan Xie

Cadence (US)

T_7 Virtual Prototyping for Power Diode and IGBT Development

Maria Cotorogea*, Peter Türkes*, Andreas Groove**

*Infineon Technologies AG, Neubiberg, (D); **Infineon

Technologies AG, Warstein-Belecke (D)

T_8 Modeling of Device Aging - Example: Diode

Franz Sischka*, Bertrand Ardouin**

*SisConsult (D), **XMOD Technologies (F)

T_9 Device Aging Simulations Enabling Circuit Optimizations

Katja Puschkarsky

Infineon Technologies AG, Neubiberg, (D)

T_10 Integration of Aging Models Across Different EDA Environments

A case study implementing HCI and NBTI models for X-FAB XU035 CMOS technology

Fabio A. Velarde Gonzalez*, André Lange*, Sonja Crocoll**, Roland Jancke*

*Fraunhofer IIS/EAS (D), **X-FAB (D)

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MOS-AK Panel Discussion

- ❑ Open Compact Modeling Directory <http://www.mos-ak.org/open_dir/>
 - ❑ FOSS EKV2.6 Compact Model (Verilog-A Code)
 - ❑ Europractice 180nm CMOS Testchip
- ❑ NEEDS Compact Models Library (NanoHub.org)
 - ❑ Licensed under NEEDS Modified CMC License according to these terms
 - ❑ <https://nanohub.org/publications/173/license/2>
- ❑ i-MOS Library (Uni. Hong Kong)
 - ❑ <https://i-mos.org/imos/model>

❑ QA Tests and Compact Model Licensing

"I do not know for the other models, but for HICUM, both HICUM/L2 and HICUM/L0 (a form have to be filled to have access) are available for everybody on the HICUM website..."

"Same for QA Test routines written in perl. It is forbidden by CMC that developing teams providing the code..."

"Clarification of the GPL status of CMC Verilog-A compact models is also needed as a matter of some urgency..."

"Sorry - I am now more then 35 years in modeling. But if this process will go further then any open source model integration will be stopped..."



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MOS-AK: Upcoming Compact Modeling Events

- ❑ Spring **MOS-AK** Workshop
 - ❑ March 13, 2018, Munich (D)
- ❑ EuroSOI-ULIS
 - ❑ March 18-21, 2018, Granada (SP)
- ❑ International EDSSC Conference
 - ❑ June 6-8, 2018, Shenzhen (CN)
- ❑ 3rd Sino **MOS-AK** Workshop
 - ❑ June 2018 Beijing (CN)
- ❑ MIXDES & Special CM Session
 - ❑ June 21-23, 2018 Gdynia (PL)
- ❑ 16th **MOS-AK** at ESSDERC/ESSCIRC
 - ❑ ESSDERC TPC Track 4: Compact Modeling
 - ❑ September 3-6, 2018 in Dresden (D)