

# Speeding Concept to Silicon

High Performance EDA Tools for Analog/Mixed  
Signal ICs, ASICs and MEMS

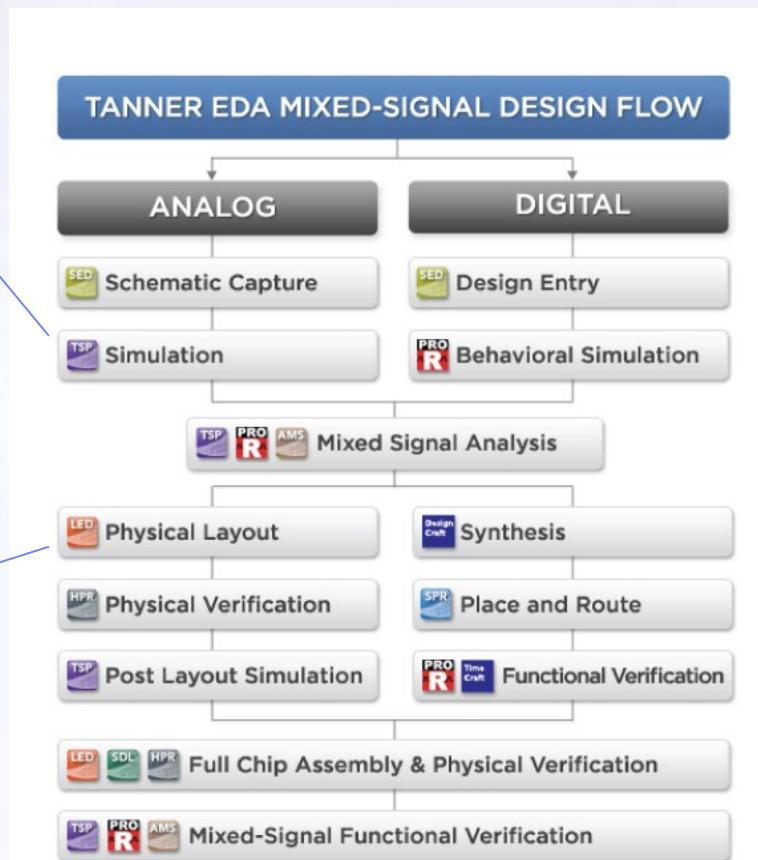
# Driving Innovation: Analog & Mixed-Signal



- Optional add-in to bolster T-Spice
- Industry-leading performance
  - Transient Noise Analysis
  - S-Parameter support



- Industry standard database format
  - Multi-user functionality



foundry-certified PDKs





# T-Spice – Analog Simulation

- Runs on Windows and Linux
- HSPICE® and PSPICE® Compatible
- Verilog-A Behavioral Modeling
- Advanced Numerical Techniques for Superior Convergence

The screenshot displays the T-Spice simulation environment. The main window shows a circuit diagram with various components and nodes. A code editor window on the right contains the following Verilog-A code:

```

Main circuit: d1atch
.include n76w.md
Minv1n a3 a1 Gnd Gnd CMOSN L=5u W=8u
Minv1p a3 a1 Vdd Vdd CMOSN L=5u W=12u
Minv2n Gnd a3 a2 Gnd CMOSN L=5u W=8u
Minv2p Vdd a3 a2 Vdd CMOSN L=5u W=12u
Minv3n Q a5 Gnd Gnd CMOSN L=5u W=8u
Minv3p Q a5 Vdd Vdd CMOSN L=5u W=12u
Minv4n Gnd Q a4 Gnd CMOSN L=5u W=8u
Minv4p Vdd Q a4 Vdd CMOSN L=5u W=12u
vphi2 phi2 Gnd bit({1100} pw=10n on=3.0 off=0.0 rt=1.25n ft=1
vphi1 phi1 Gnd bit({0011} pw=10n on=3.0 off=0.0 rt=1.25n ft=1
vdata data Gnd bit({1000} pw=20n on=3.0 off=0.0 rt=1.25n ft=1
Mtg1n a1 phi2 data Gnd CMOSN L=5u W=8u
Mtg1p a1 phi1 data Vdd CMOSN L=5u W=8u
Mtg2n a2 phi1 a1 Gnd CMOSN L=5u W=8u
Mtg2p a2 phi2 a1 Vdd CMOSN L=5u W=8u
    
```

The simulation window at the bottom provides the following statistics:

Simulation input:	d1atch.sp	Simulation output:	d1atch.out
Simulation progress:	Simulation completed		
	Time = 200.000000ns	100%	
Total nodes	11	Active devices	16
Total devices	20	Passive devices	0
		Independent sources	4
		Controlled sources	0
Parsing	0.21 seconds		
Setup	0.05 seconds		
DC operating point	0.04 seconds		
Transient Analysis	3.01 seconds		
Total	3.31 seconds		

The waveform plot shows the output of the mixer circuit, and the FFT plot shows the frequency spectrum of the output signal.

# T-Spice – Build in Models (extract)

- PSP
- BSIM3 v3.3
- BSIM4 v4.7
- EKV v2.6,
- HiSIM260
- HiSIM\_HV2
- VBIC
- BSIM SOI v4.4
- MOS 9, 11, 20
- MOS 30, 31, 40
- Philips Mextram
- Philips Modella
- Poly-Si TFT
- RPI a-Si

**In total there are more than 80 compact models  
Verilog A support for all new developments**

# Tanner Tools for Universities and Students

- **Almost free licenses through Europractice**
- **Easy to install, just klick on „setup.exe“**
- **Ideal for class rooms because of short learning curve**

**For more information goto:**

**[www.tannereda.com](http://www.tannereda.com)**

**Or ask me in the coffee break.**