Modeling of very low doped and pinched resistors

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Customized 3D jfet model

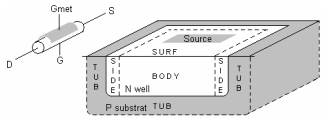
Shichman and Hodges Spice model, with 2 model parameters customized to enable the modeling of 3D pinching effect:

- Transconductance: Beta=-1/(2*Vto*R)
- Threshold voltage: Vto=Vto_inf/(1+2*xj/w)

Direct link to series resistance: R=Rsh*(l+delta_L)/(w+delta_W)
Additional parasitic diodes for capacitance, leakage and BV modeling

Limitations: poor fit for too lightly doped layers
predefined number of terminals

Verilog-A model for very lightly doped resistors with metal/poly flap [1]

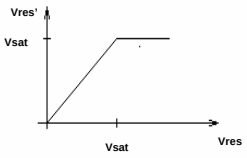


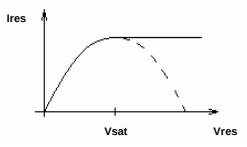
DC model is voltage controlled current source containing 3D pinching effects

$$I_{res}=\frac{V_{res'}}{rh0\cdot(l+dl)}\left((w+dw)-2\cdot\alpha_p\sqrt{\psi_p+V_{10}}\right)\left(xo-\alpha\sqrt{\psi+V_{10}}-\alpha_o\sqrt{\psi_o+V_{11}}\right)\left(1+\lambda\cdot|V_{res}|\right)$$

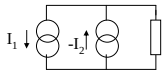
Lateral pinching — Vertical pinching (Bottom, Top)

Ψ .....built-in potential
V_{10}….pinch-off voltage caused by substrate-nwell potential V_{10}=f(Vres)
V_{11}….pinch-off voltage caused by metal plate potential V_{11}=f(Vres)
α……pinching factor
Vres'…..auxiliary voltage used instead of Vres to keep the current constant in the saturation (finally adjusted by parameter λ)





- **VSAT CALCULATION**:
  Vsat=peak of parabola (the first derivative of Ires = 0)
- **PROBLEM**:
  Too complicated equation - the solution of 1st derivative can't be explicitly expressed
- **SOLUTION**:
  The first derivative can be calculated by Spice iterations during simulation execution.
- **HOW TO DO IT?**
  The 1st derivative can be split into 2 parts – let's call them I1 and I2:
  I1+I2=0 ➔ I1=-I2
  I1 and I2 can be represented by 2 current sources in one loop (Kirchhoff low).



BASIC MODEL PARAMETERS:
- Concentrations (body, tub, side, surface)
- Diffusion depth (Xj)
- Series resistance
- Geometry factors (dW, dL)
- Field oxide thickness
- Correction and temperature parameters

Mainly Physically Based Parameters

Limitations: long simulation time
poor convergence
bad symmetry

Model convergence improvements

1) Made model fully symmetrical (I@V=-(I@-V)
2) Used Verilog-A capability to prevent extreme solutions of Vdsat evaluation
3) Linearized model for very low voltages (explicitly expressed equation)

- Advantages of improved model:
  Model is universal and applicable in various HV macromodels
- Disadvantages of improved model:
  although the convergence was significantly improved (no crash any more) the simulation time is still relatively long due to implicitly expressed equation in nonlinear area

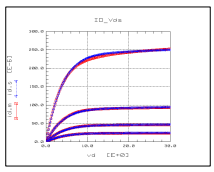
Model improvement for Fast and precise pinch resistor

Pinch resistors don't have top vertical pinching caused by the metal/poly flap. Top and bottom pinching has the same physical fundament, the only difference is "tub" and "surface" concentration.
These 2 concentrations were connected to one parameter and surface top pinching was removed from the equation..

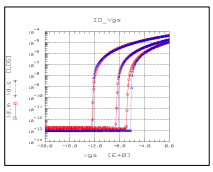
$$I_{res}=\frac{V_{ext}}{rh0\cdot(l+dl)}\left((w+dw)-2\cdot\alpha_p\sqrt{\psi_p+V_{10}}\right)\left(xo-\alpha\sqrt{\psi+V_{10}}-\alpha_o\sqrt{\psi_o+V_{11}}\right)\left(1+\lambda\cdot|V_{res}|\right)$$

This allows for explicit solution of Vsat.

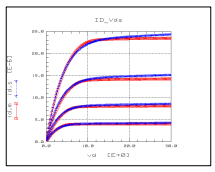
The simulation time was significantly decreased to be comparable with built-in spice models and the preciseness is still very good.



IdVd for various l and w



IdVg – pinch-off voltage for various widths



IdVd for various Vs-Vsub

Model improvement for Fast and precise part of HV device macromodels

HV devices are often wide, or don't contain side edges.
The side pinching is then negligible, so it was removed from the equation.

$$I_{res}=\frac{V_{ext}}{rh0\cdot(l+dl)}\left((w+dw)-2\cdot\alpha_p\sqrt{\psi_p+V_{10}}\right)\left(xo-\alpha\sqrt{\psi+V_{10}}-\alpha_o\sqrt{\psi_o+V_{11}}\right)\left(1+\lambda\cdot|V_{res}|\right)$$

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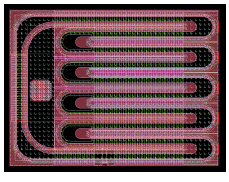
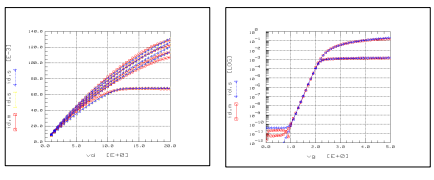


Scalable 700V HV LDMOS layout with drain bonding pad



700V HV LDMOS with quazisaturation modeled by Verilog-A model of lightly doped resistor

Conclusions

The universal Verilog-A model for very lightly doped resistor was introduced.
The model can be used in macromodel of different HV devices (LDMOS, HV schottky diode, level shifter, pinch resistors, metal-poly flapped lightly doped resistors, etc…)
In most cases the simulation time is comparable with standard complex Spice models
The model is cleaned from convergence issues and is able to simulate up to extremes (temperature, bias, size)

REFERENCES
[1] James Victory, Colin C. McAndrew, Jeff Hall and Mike Zunino, A 4-Terminal Compact Model for High Voltage Diffused Resistors with Field Plates, IEEE Journal of Solid State Circuits, VOL 33, No. 9, 1998, p1453