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Comparison of MOS Model EKV3 with BSIM3 and BSIM4

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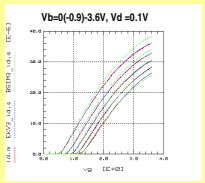
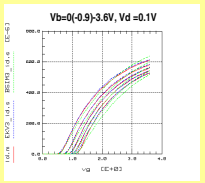
Outline

- Comparison of a new charge based model, EKV3 with the BSIM3 and BSIM4 for MOSFETs
- Extraction of model parameters in 0.35um CMOS technology for the EKV3 and BSIM3 and 0.18um CMOS technology for the EKV3 and BSIM4
- Implementation of model parameter extraction strategy in ICCAP
- Geometry scalability of EKV3 is verified for both technologies
- Worst case corner modeling is also investigated and the result is presented
- Finally, model benchmark test has been performed for the EKV3 model

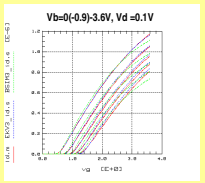
EKV3 vs. BSIM3



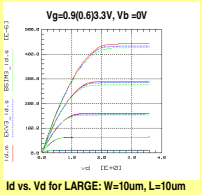
Id vs. Vg for LARGE: W=10um, L=10um



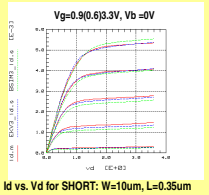
Id vs. Vg for SHORT: W=10um, L=0.35um



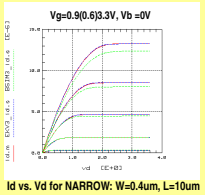
Id vs. Vg for NARROW: W=0.4um, L=10um



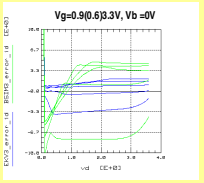
Id vs. Vd for LARGE: W=10um, L=10um



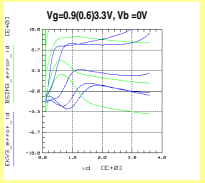
Id vs. Vd for SHORT: W=10um, L=0.35um



Id vs. Vd for NARROW: W=0.4um, L=10um



Error of Id for LARGE: W=10um, L=10um



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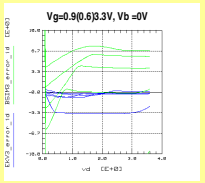
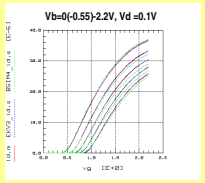


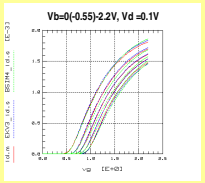
Error of Id for NARROW: W=0.4um, L=10um

- EKV3 is more accurate physical model for CMOS
- Better fitting of EKV3 model with measurements compared to BSIM3
- Comparison of the simulation results for different geometries clearly illustrates the advantage of geometry scalability in the EKV3 model

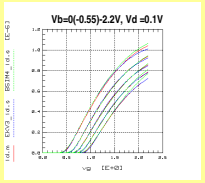
EKV3 vs. BSIM4



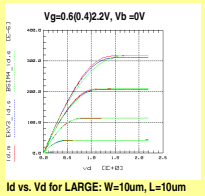
Id vs. Vg for LARGE: W=10um, L=10um



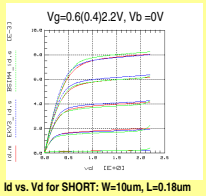
Id vs. Vg for SHORT: W=10um, L=0.18um



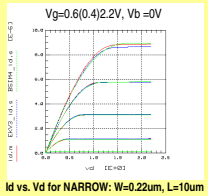
Id vs. Vg for NARROW: W=0.22um, L=10um



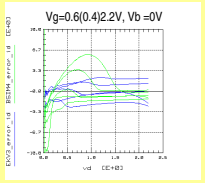
Id vs. Vd for LARGE: W=10um, L=10um



Id vs. Vd for SHORT: W=10um, L=0.18um



Id vs. Vd for NARROW: W=0.22um, L=10um



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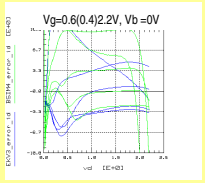

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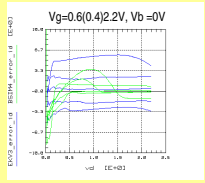

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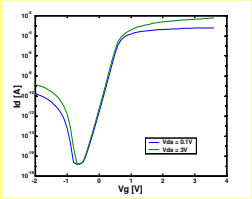
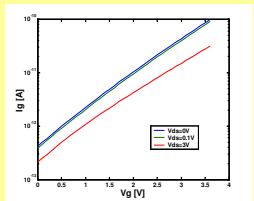


Id vs. Vg for W=10um, L=0.35um due to gate-induced drain leakage effect in EKV3 model



Id vs. Vg for W=10um, L=0.35um due to gate leakage current in EKV3 model

- Similar fitting quality for both the EKV3 and BSIM4 with measurements
- Less number of model parameters in EKV3 compared to BSIM4
- EKV3 model includes short channel effects, narrow channel effects, drain induced barrier lowering, mobility reduction due to vertical field, carrier velocity saturation, channel length modulation, polysilicon-gate depletion effects, quantum mechanical effective on gate oxide thickness, gate-induced drain leakage, gate leakage current, and overlap capacitance

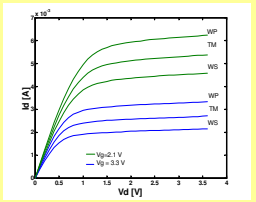
Worst Case Model

- Determination of the worst case parameters is performed using typical parameters of the MAP parameters
- Minimum and maximum value of model parameters are calculated as follows:

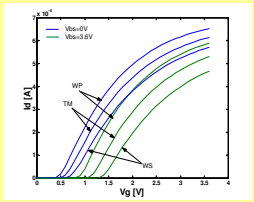
$$model\_par\_min = model\_par\_typ\left[1-\left(\frac{par\_typ - par\_min}{par\_typ}\right)\right]$$

$$model\_par\_max = model\_par\_typ\left[1+\left(\frac{par\_max - par\_typ}{par\_typ}\right)\right]$$

- Extracted model parameters for different worst cases (WP, TM, WS) are applied to EKV3 parameters LOV, CJ, CJSW, COX, DL, DW, VTO, KP, GAMMA

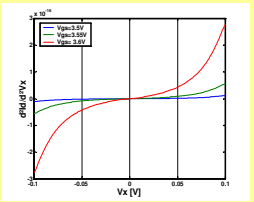


Id vs. Vd for SHORT: W=10um, L=0.35um

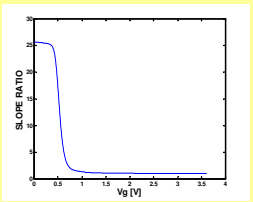


Id vs. Vg for SHORT: W=10um, L=0.35uu

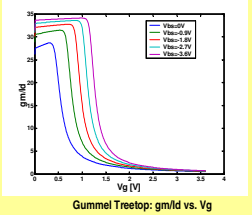
Benchmark Test



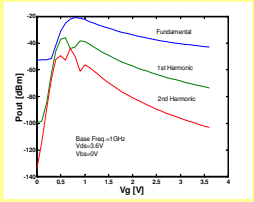
Gummel Symmetry : d²Id/d²Vx vs. Vx



Gummel Slope Ratio vs. Vg



Gummel Treetop: gm/Id vs. Vg



Harmonic distortion: Pout vs. Vg

Conclusion

- EKV3 is a self-consistent and charged based physical model for new generation MOSFETs
- Most of the model parameters are directly linked to the process control monitoring and thus parameter extraction is much simpler
- EKV3 has less number of parameter set while offering similar scaling ability as BSIM3/4
- Also, symmetrical test has been passed successfully for both DC and CV characteristics

Acknowledgment: We would like to thank Dr. Matthias Bucher, Technical University of Crete (TUC), Greece for the Verilog-A EKV3 code and valuable discussion.