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Unified charge-based Transistor Model including Degradation Mechanisms

MOS-AK Workshop

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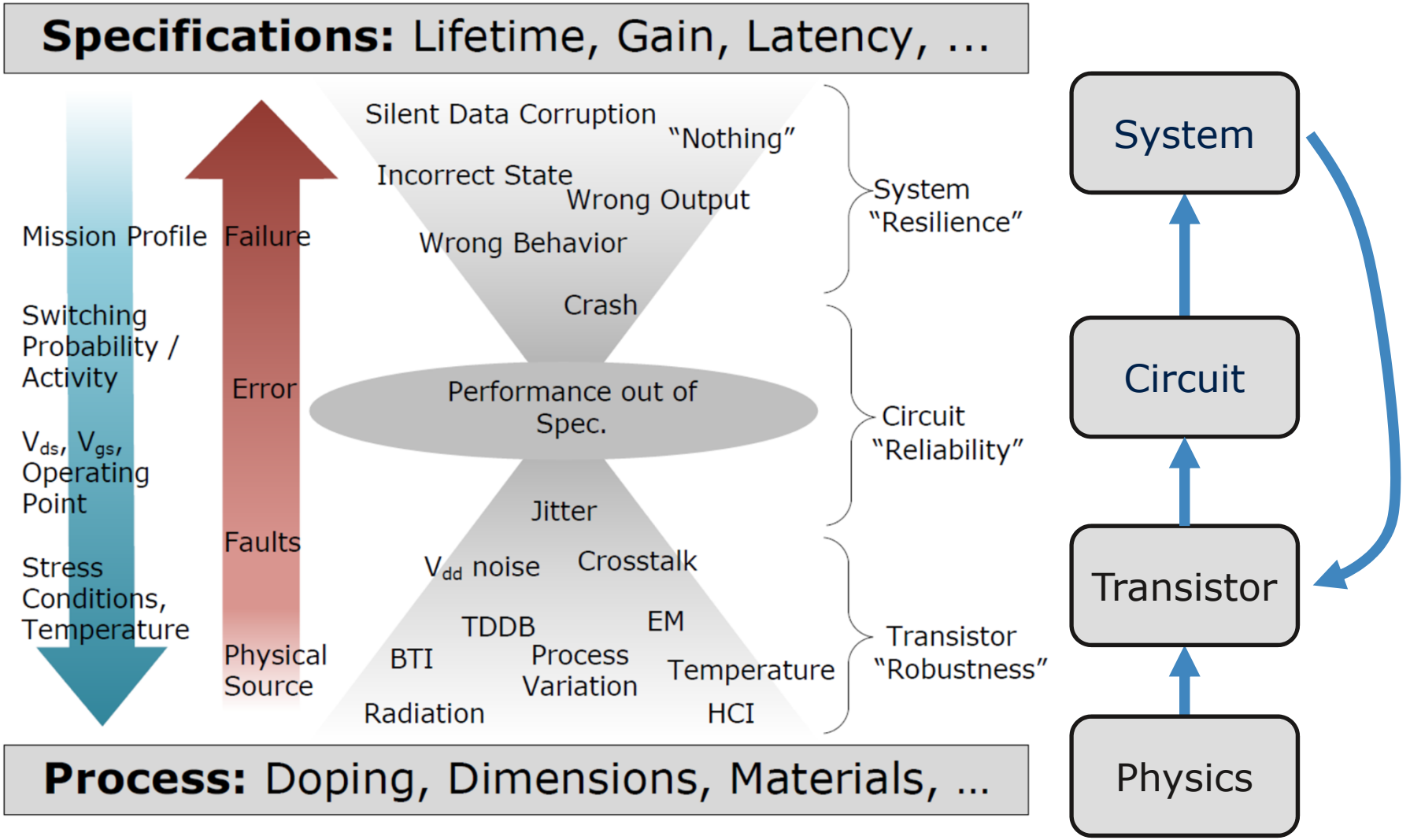
Lausanne - March 2017

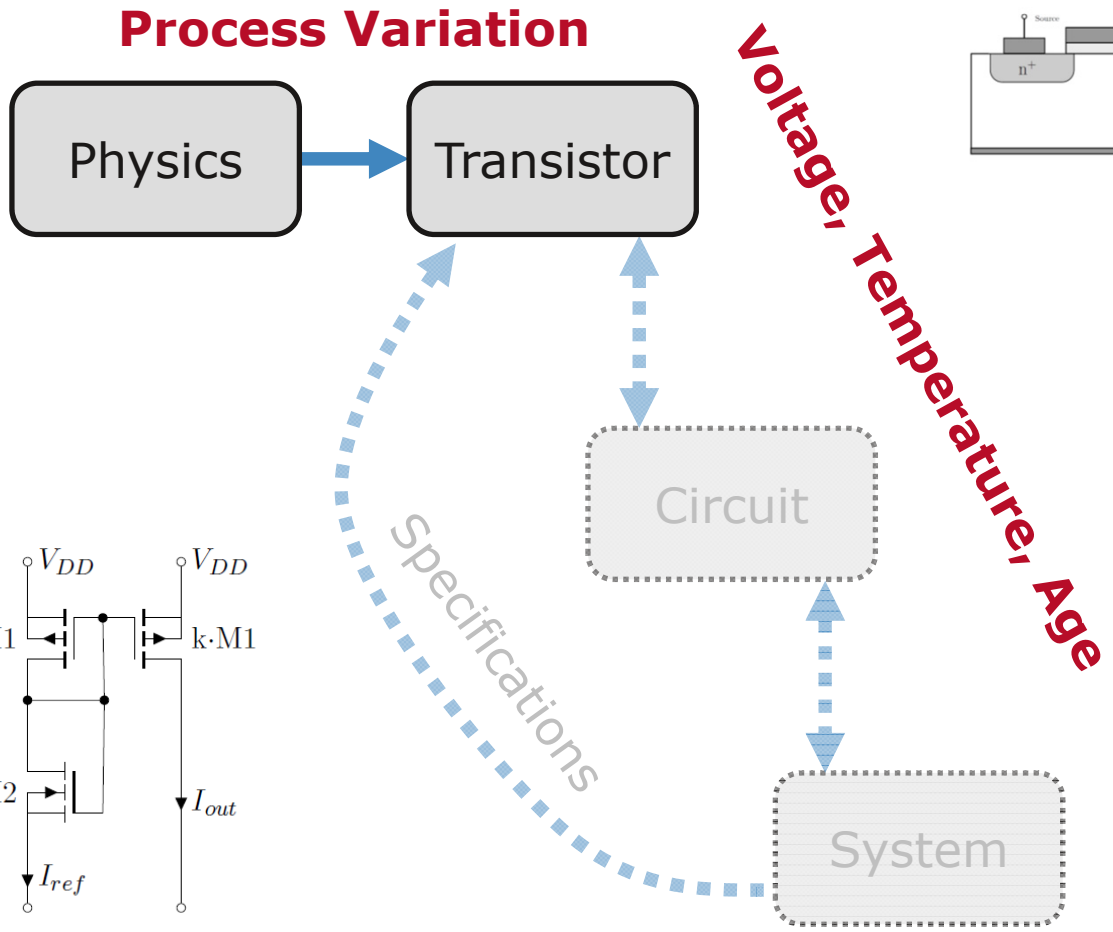
Universität Bremen

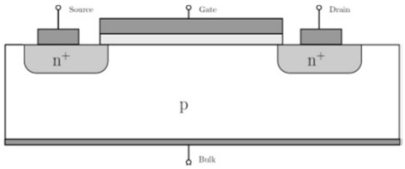
Motivation

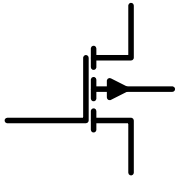


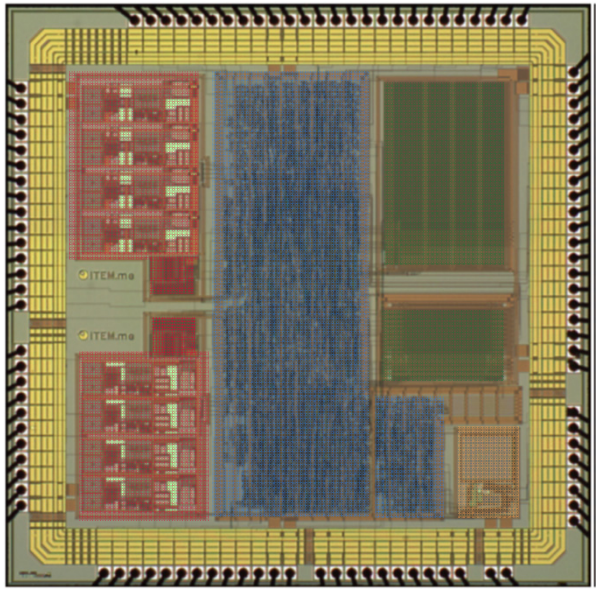
Inspired by Herkersdorf, Schlichtmann, Teich, et.al: Resilience Articulation Point (RAP): Cross-layer dependability modeling for nanometer system-on-chip resilience. Microelectronics Reliability 2014

Overview

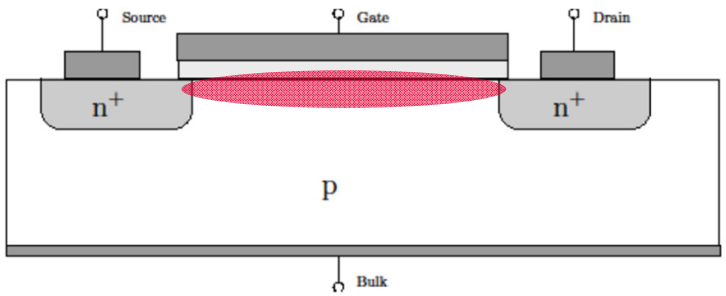

Process Variation
Physics
Transistor
Voltage, Temperature, Age
Circuit
Specifications
System
V_{DD}
V_{DD}
M1
k·M1
M2
I_{out}
I_{ref}


Source
Gate
Drain
n+
n+
p
Bulk

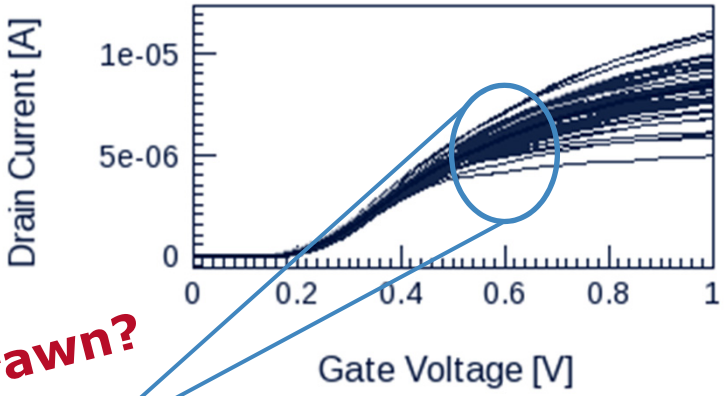




Transistor Degradation



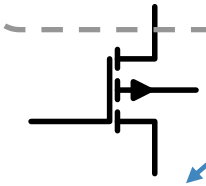
Threshold Voltage



Process variations

Conclusions drawn?

$\frac{W}{L}, V_{dd}, V_B, V_G, \ldots$



1. V_{th}
2. Q_i
3. Φ_s

Transistor Model

- Process → Monte Carlo
- Temperature → SPICE
- Voltage → SPICE
- Age → RelXpert

Influences

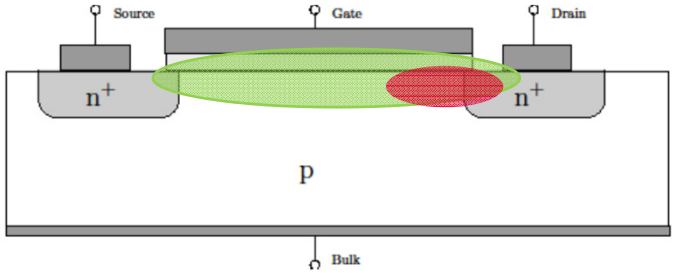
Consideration

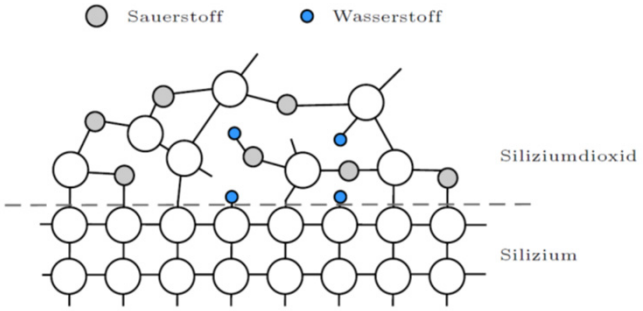
g_m, g_{ds}, V_{th}, I_{DS}

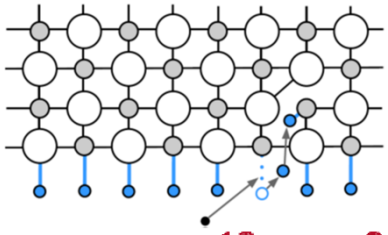
No propagation of interdependencies within modeling

FEOL Aging Mechanisms

Hot Carrier Injection

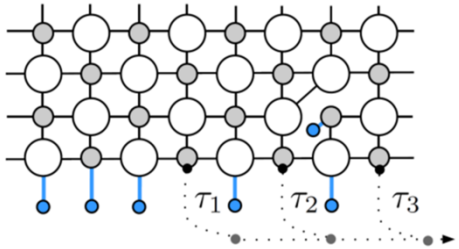




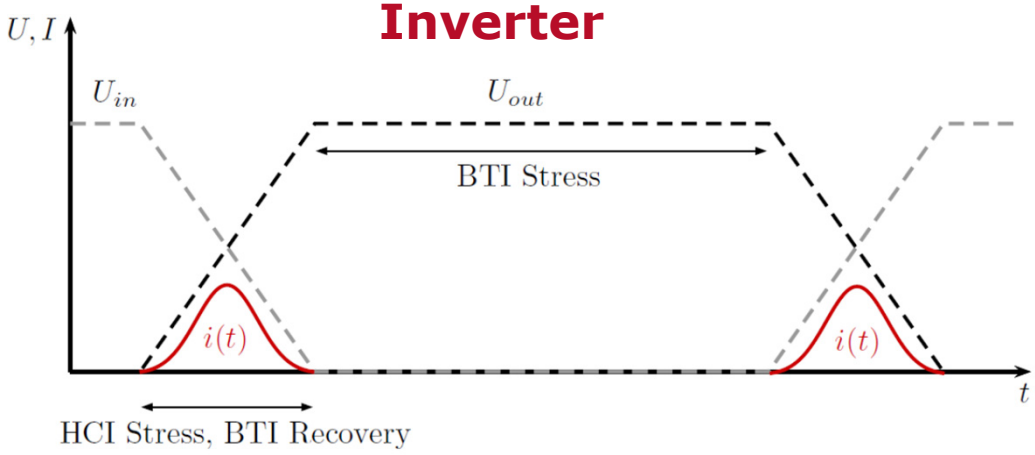


$\tau = 10^{-12} \ldots 10^{8}\ \mathrm{s}$

Bias Temperature Instability



Different Stress Conditions Inverter



Additional Gate Charge

$$Q_i = Q_0(P,V,T) + Q_{age}(t)$$

Transistor Aging Models

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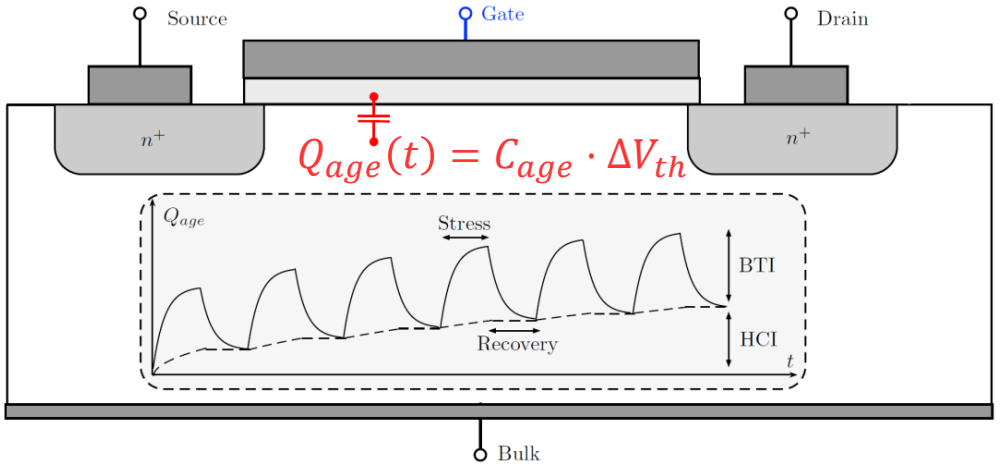
V_{th} BSIM4:

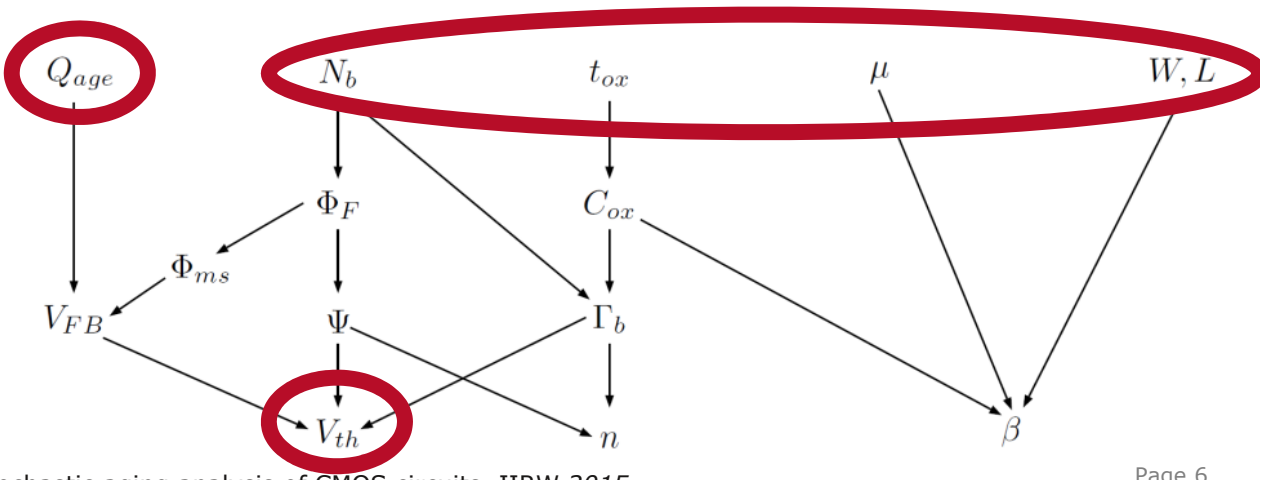
$$V_{th} = VTH0 + \left(K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K1\cdot\sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K_{2ox}V_{bseff}$$
$$+K_{1ox}\left(\sqrt{1+\frac{LPE0}{L_{eff}}}-1\right)\sqrt{\Phi_s} + \left(K3+K3B\cdot V_{bseff}\right)\frac{TOXE}{W_{eff}'+W0}\Phi_s$$
$$-0.5\cdot\left[\frac{DVT0W}{\cosh\left(DVT1W\frac{L_{eff}W_{eff}'}{l_{tw}}\right)-1}+\frac{DVT0}{\cosh\left(DVT1\frac{L_{eff}}{l_t}\right)-1}\right]\left(V_{bi}-\Phi_s\right)$$
$$-\frac{0.5}{\cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right)-1}\left(ETA0+ETAB\cdot V_{bseff}\right)\cdot V_{ds} - nv_t\cdot\ln\left(\frac{L_{eff}}{L_{eff}+DVTP0\cdot\left(1+e^{-DVTP1\cdot V_{DS}}\right)}\right)$$
$$-\left(DVTP5+\frac{DVTP2}{L_{eff}^{DVTP3}}\right)\cdot\tanh\left(DVTP4\cdot V_{ds}\right)$$

- Standard
- Non-Uniform Doping
- Pocket Implant
- SCE
- DIBL
- DITS
- Narrow Width

$$V_{GS} \geq V_{th} + \Delta V_{th}(t)$$



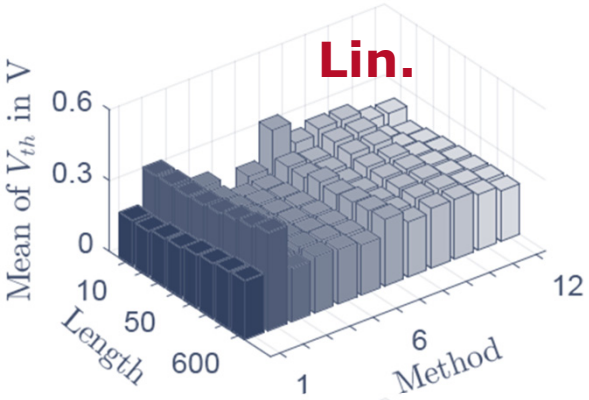
- Unclear age-dependencies
- Unwanted interferences

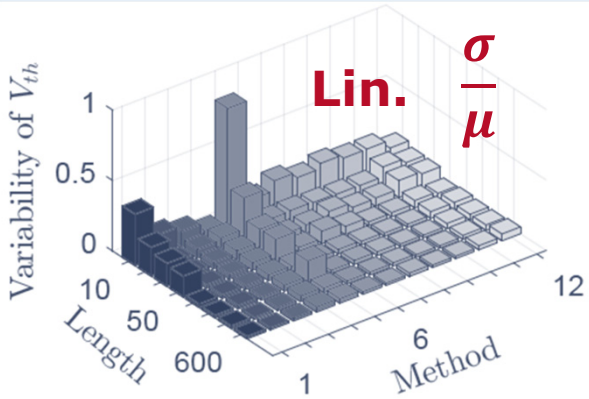


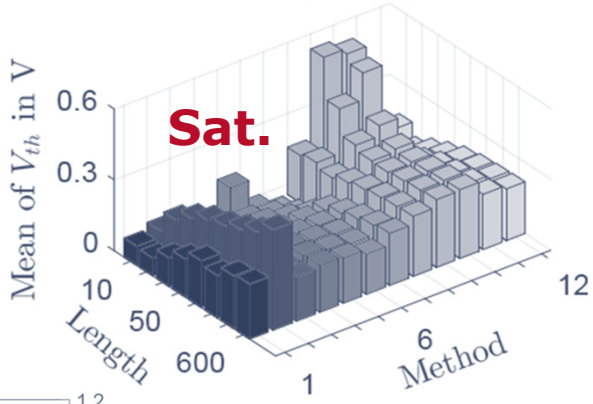
Hillebrand et al. Charge-based stochastic aging analysis of CMOS circuits. IIRW *2015*

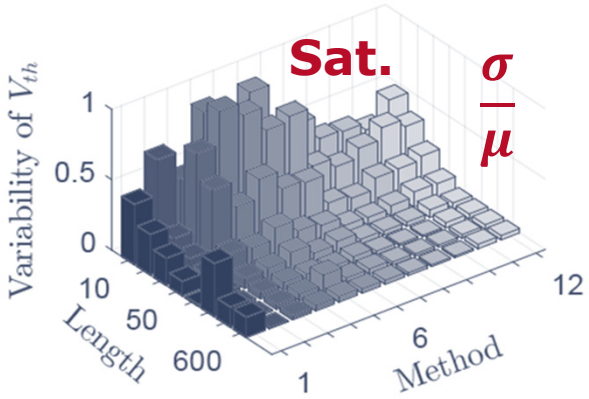
Threshold Voltage Measurement

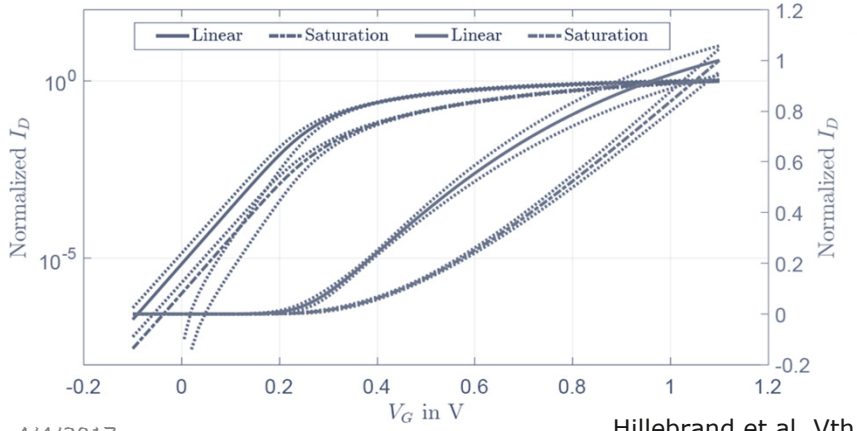
Number	Name
1	Maximum g_m
2	Linear Extraction
3	Adjusted Constant Current
4	Second Derivative
5	Third Derivative
6	Current-to-square-root-of-the-Transconductance
7	Current-to-square-root-of-the-Transconductance (modified fitting)
8	Transition Method
9	Normalized Mutual Integral Difference
10	Normalized Reciprocal H function
11	Transconductance-to-Current-Ratio
12	Reciprocal H function





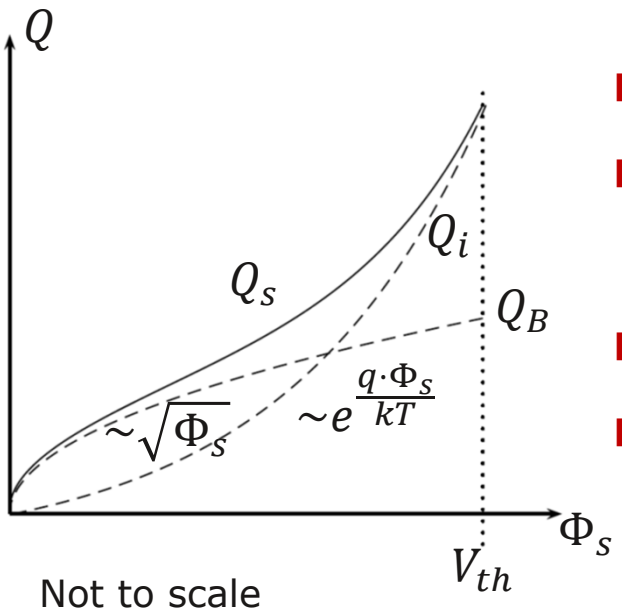






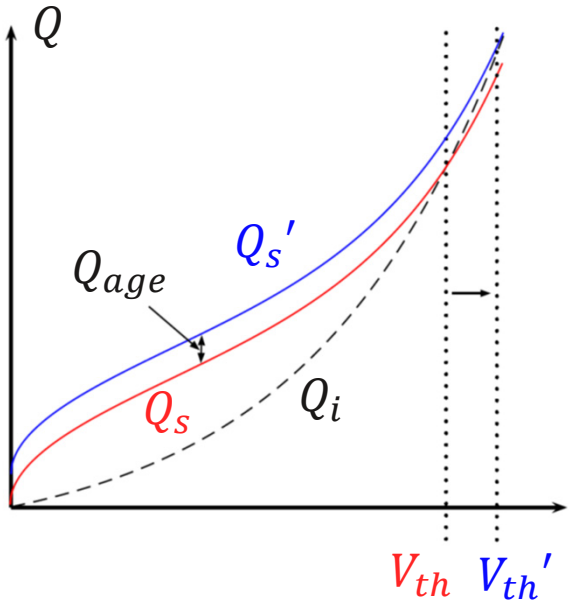
w/o knowledge of method and region ΔV_{th} can be misleading

Charge Based Aging Model



Not to scale

- Charge based model
- EKV, BSIM6
- PVTA within Model
- Verilog-A



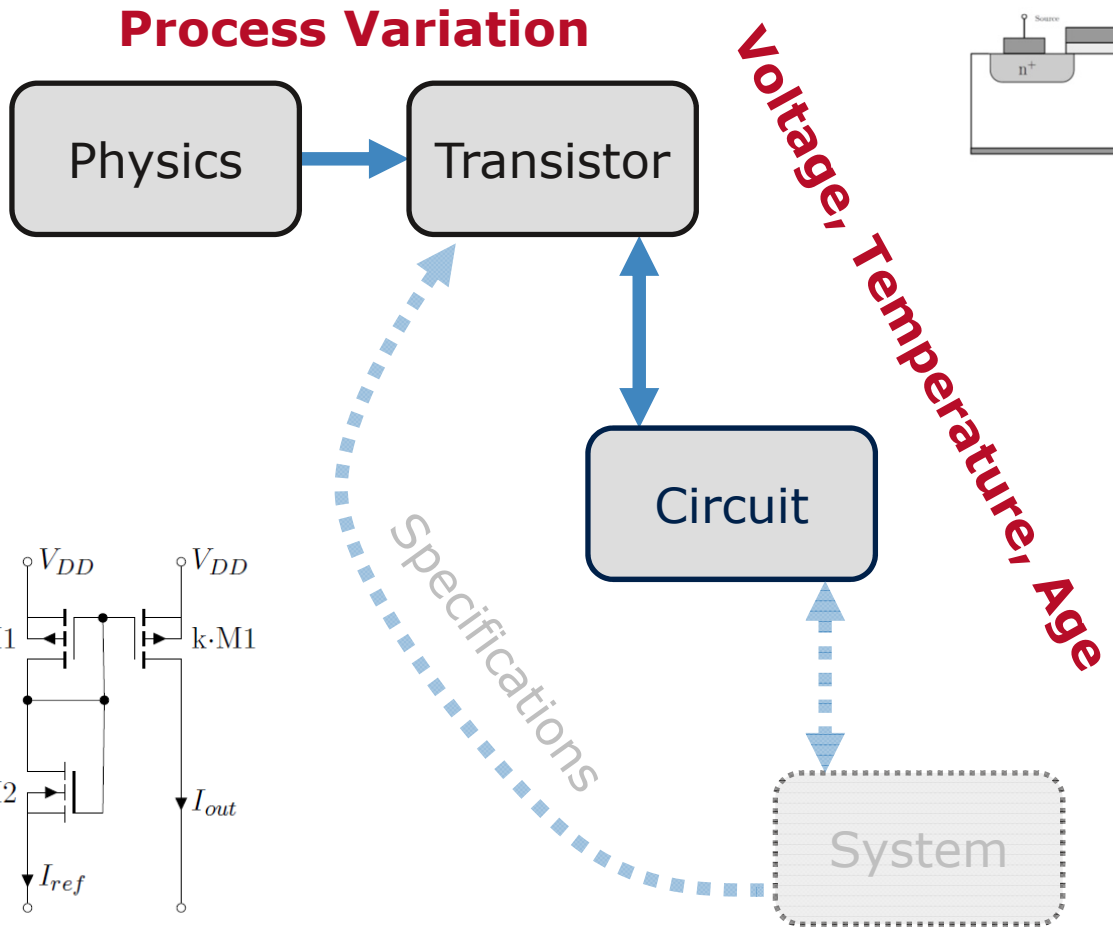
Shift of V_{th}: Consequence not Cause

$$Q_i = -\gamma' . C_{ox} \cdot \sqrt{V_t} \left[\sqrt{\frac{\psi_S}{V_t} + e^{\frac{\psi_S - 2.\phi_F - V_{ch}}{V_t}}} - \sqrt{\frac{\psi_S}{V_t}} \right] - Q_{age}(t)$$

➔ Shift of parameters are calculated within the transistor model

➔ No need for additional simulation environment

Overview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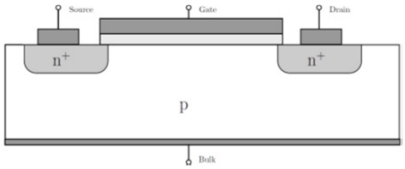
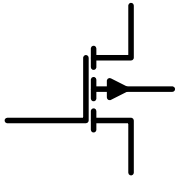
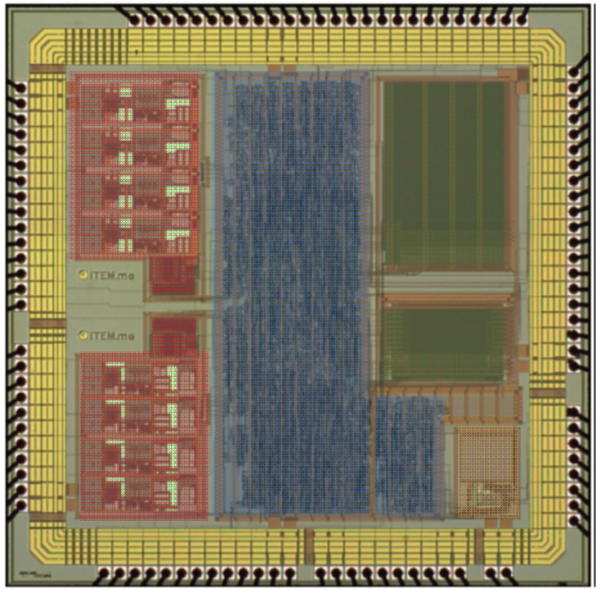

Source
Gate
Drain
n+
n+
p
Bulk



V_{DD}
V_{DD}
M1
k·M1
M2
I_{out}
I_{ref}



Circuit Design Method

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g_m/I_D - Method

- Operation Mode

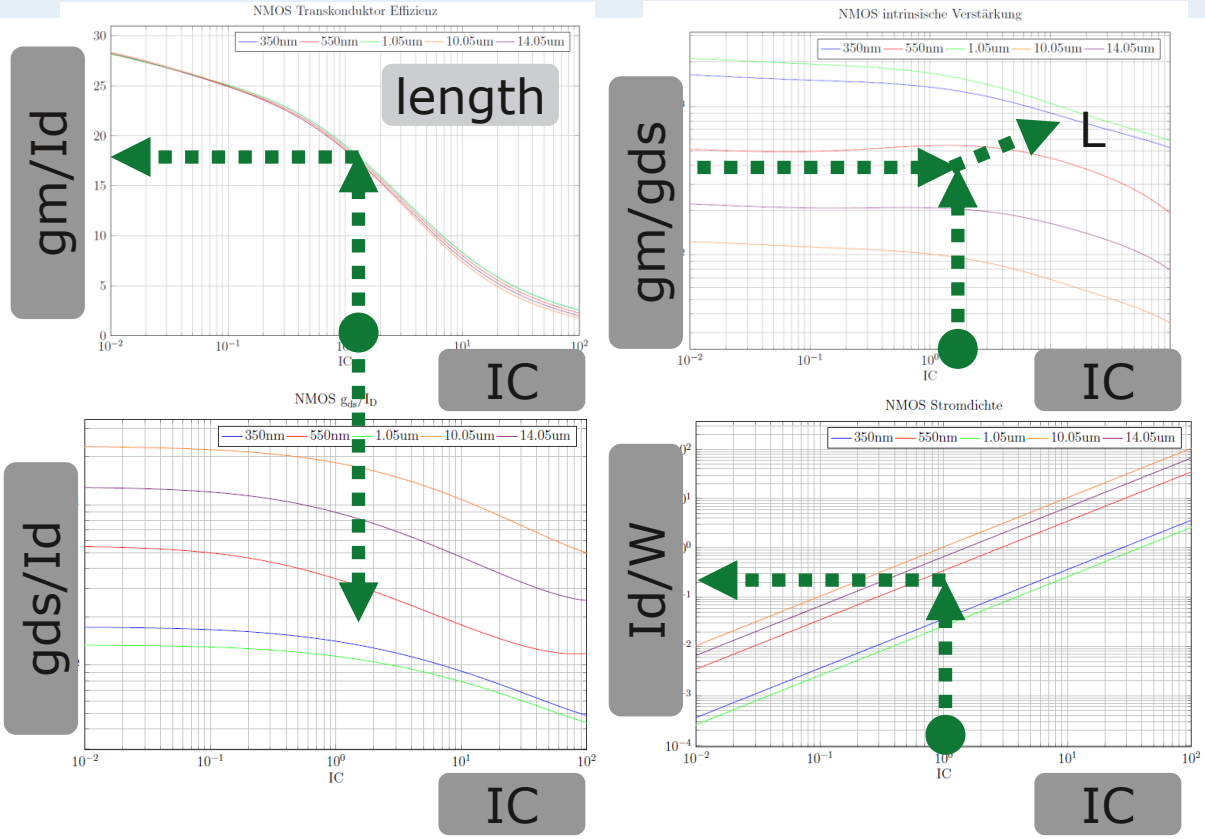
$$IC = \frac{I_D}{I_0 \, W/L}$$

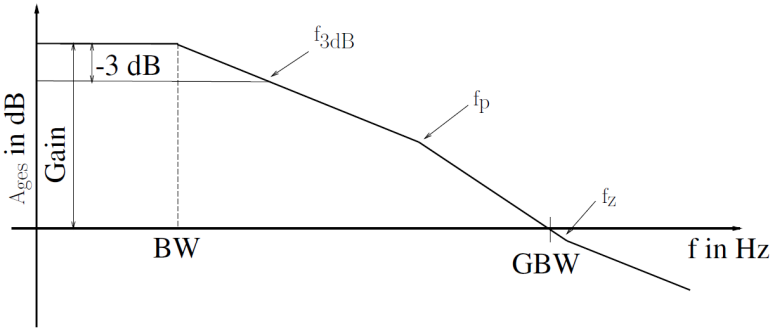
- Speed / Area

  L

- Power/Speed

  I_D



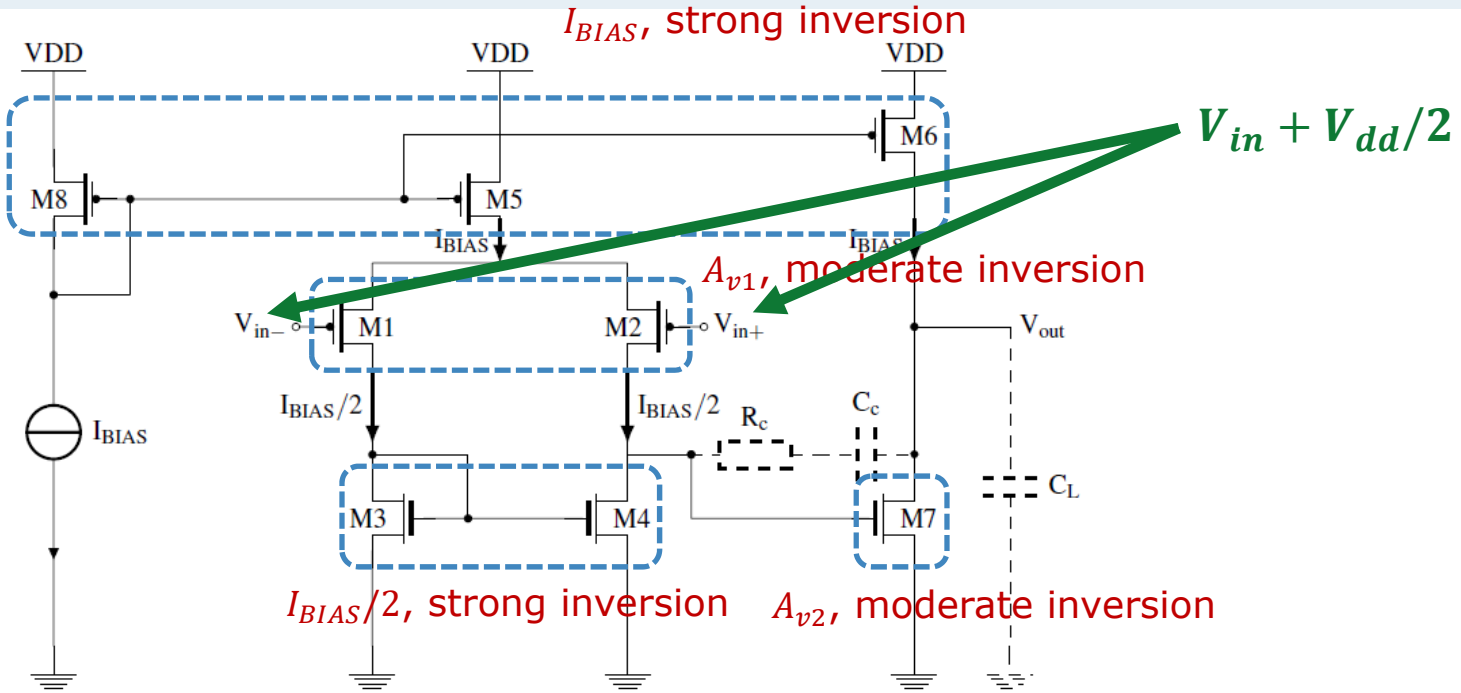


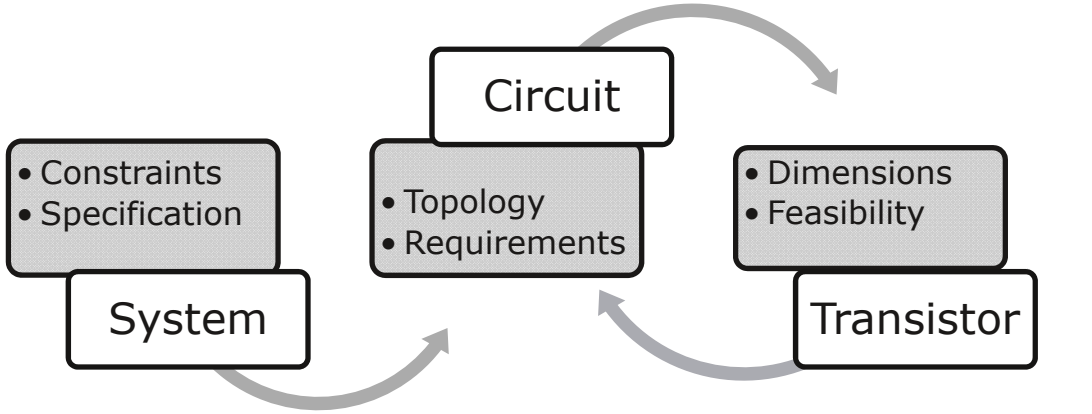
FOM	Equation	GMID-Tool notation
Gain_{lin}	$g_{m4}/g_{ds4}+g_{ds2}$	$M4.gm/\text{M4.gds}+\text{M2.gds}$
Gain_{dB}	$20\log(\text{Gain}_{\text{lin}})$	$\text{mag2db}(\text{Gain}_{\text{lin}})$
GBW	$g_{m1}/C_{GD1}+C_L$	$M1.gm/\text{M1.cgd}+C_L$
f_{3dB}	$g_0/2\pi(C_{DS4}+C_{GD4}+C_L)$	$M4.gds/2*\text{pi}*(\text{M4.cds}+\text{M4.cgd}+C_L)$
f_z	$g_{m4}/2\pi \cdot C_{GD4}$	$M4.gm/2*\text{pi}*\text{M4.cgd}$
SR	I_{BIAS}/C_L	$M2.\%ids/C_L$

Hillebrand et.al. Design and Verification of Analog CMOS Circuits Using the gm/ID-Method with Age-Dependent Degradation Effects, VARI 2016

Miller OTA

- A_{ges}
- f_{3dB}
- GBW
- SR





Expensive Redesign

- Input needs bias
- Biasing circuit must be taken into account for PVTA investigation

Beta Multiplier: Reference Voltage

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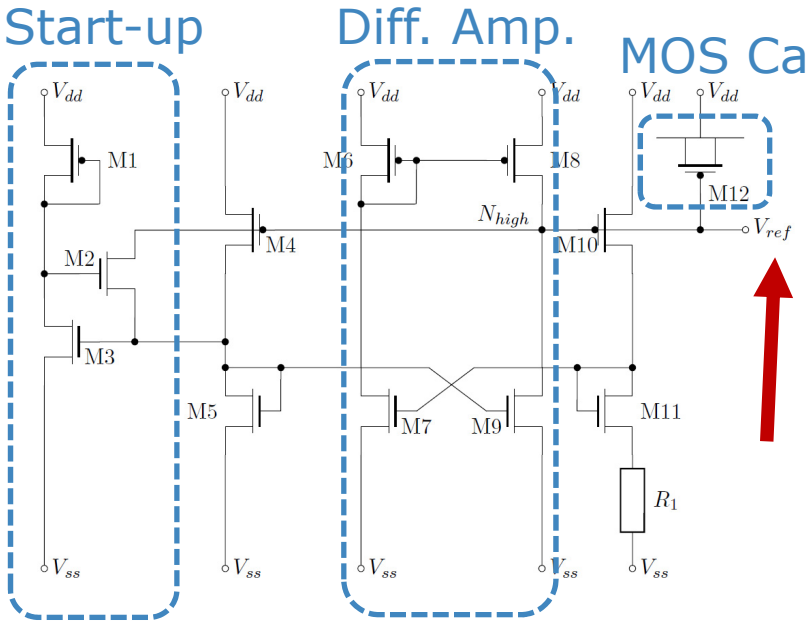
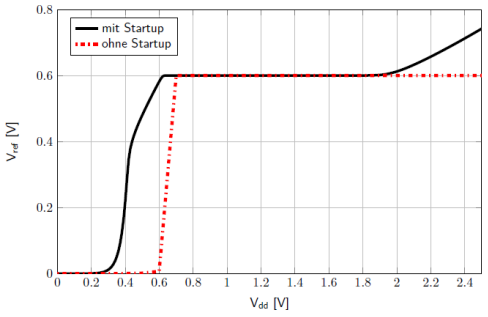


PTA influences on circuit level resulting in voltage change on system level.

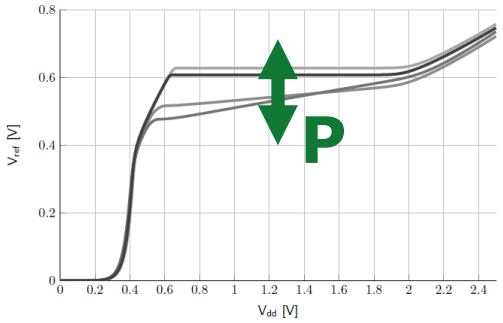
Circuit ↔ System

No Divide and Conquer for PVTA

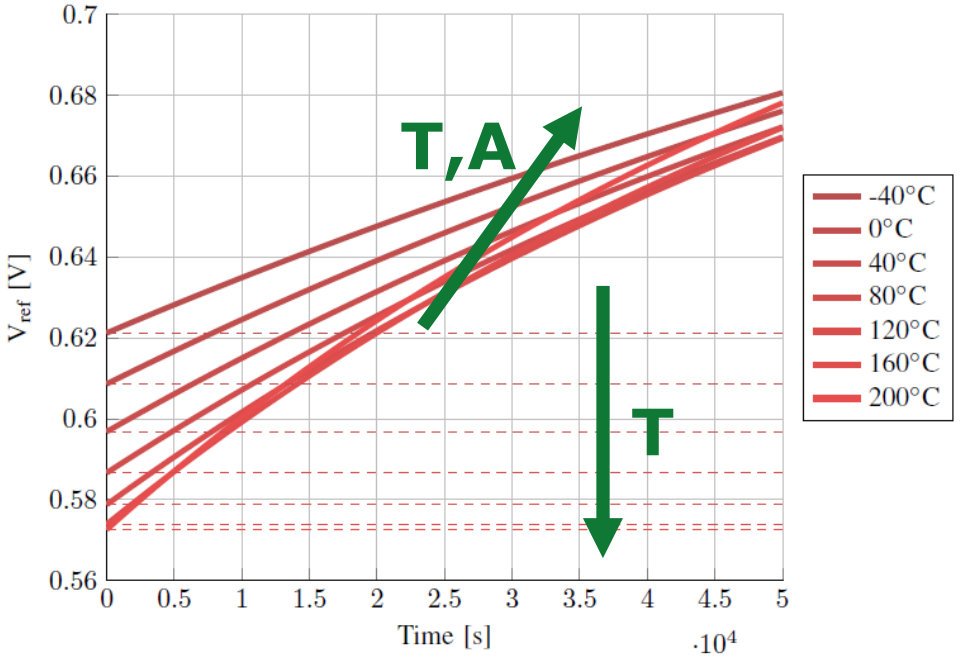
Circuit Design



Process

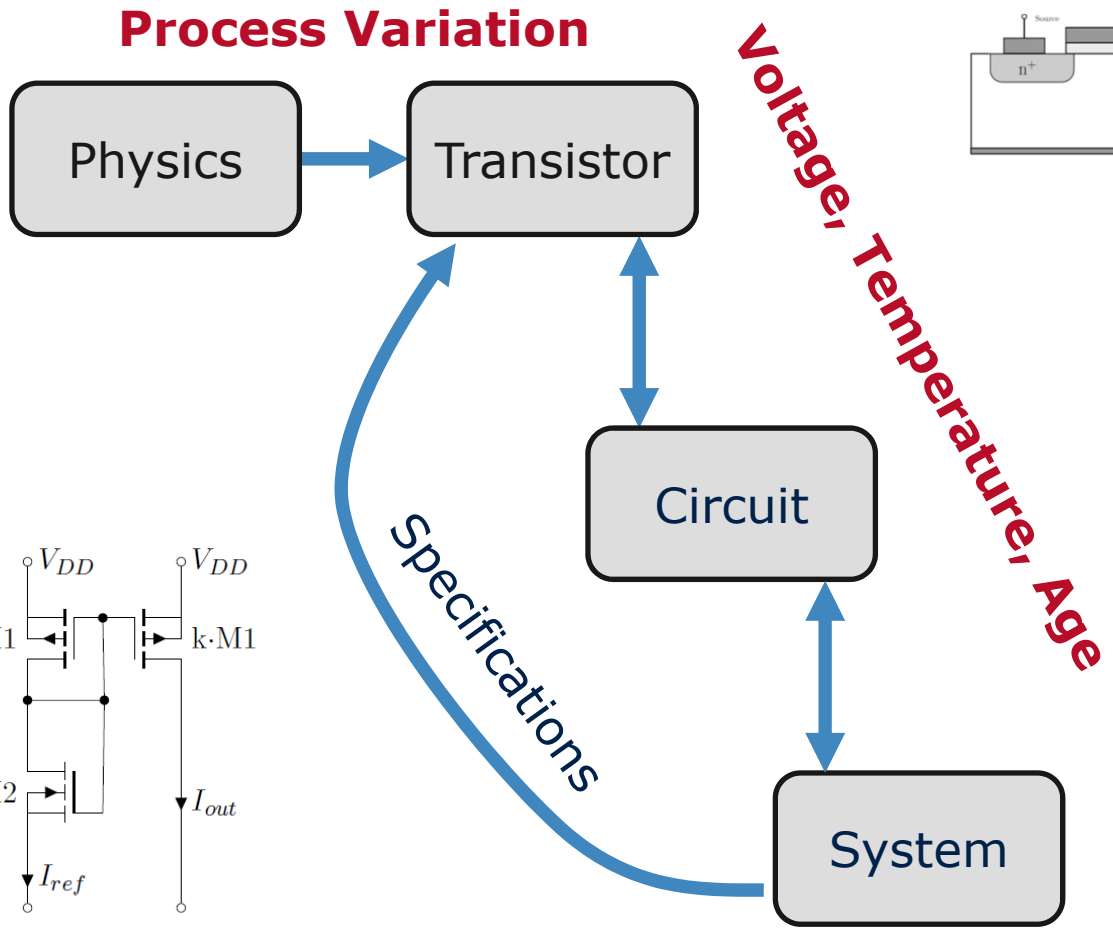


Temperature , Age



Hillebrand et.al. Online Monitoring of NBTI and HCD in Beta-Multiplier Circuits, IOLTS 2016

Overview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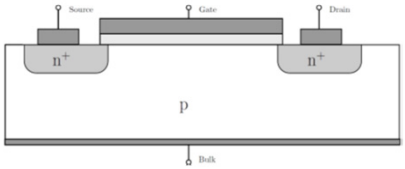
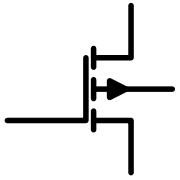
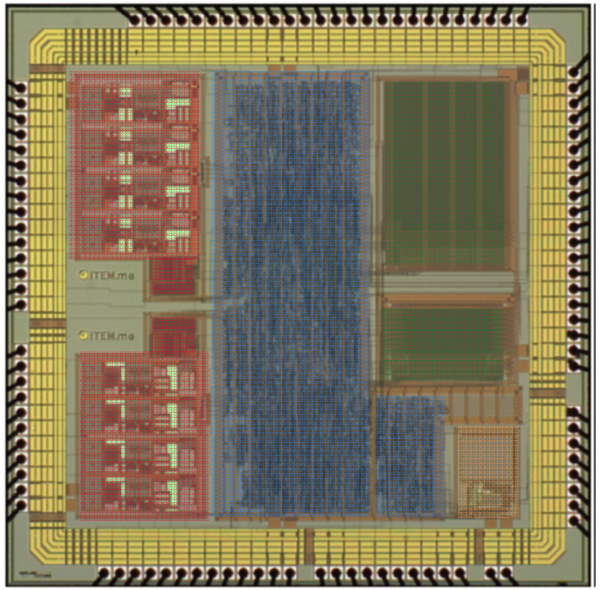
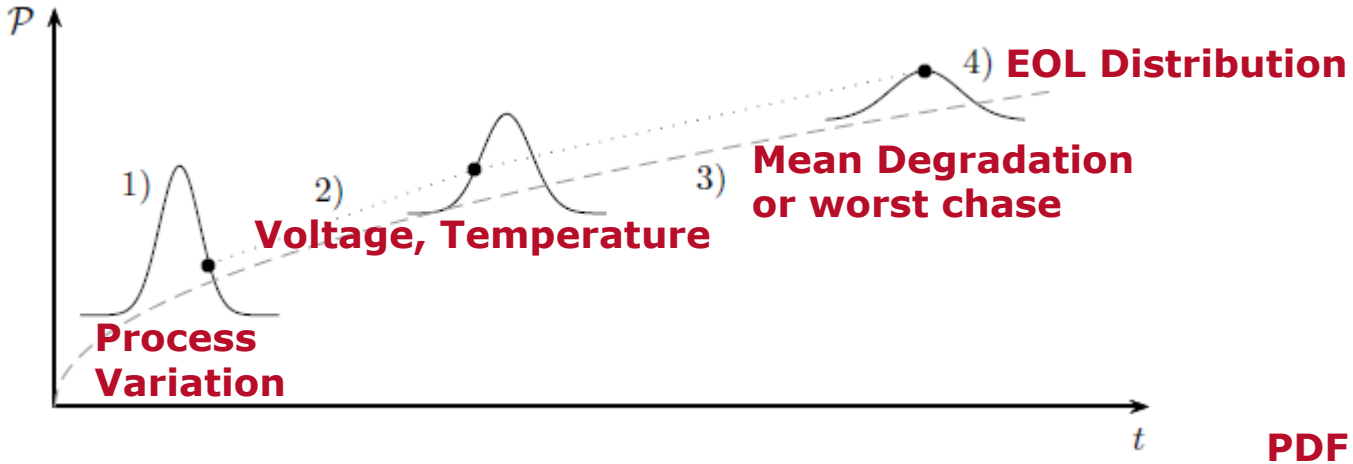

Source
Gate
Drain
n+
n+
p
Bulk

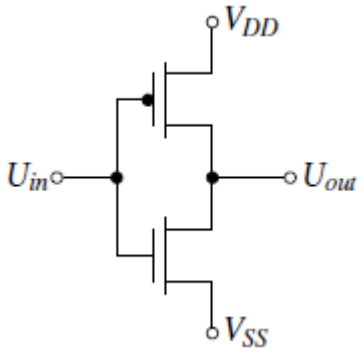


V_{DD}
V_{DD}
M1
k·M1
M2
I_{out}
I_{ref}

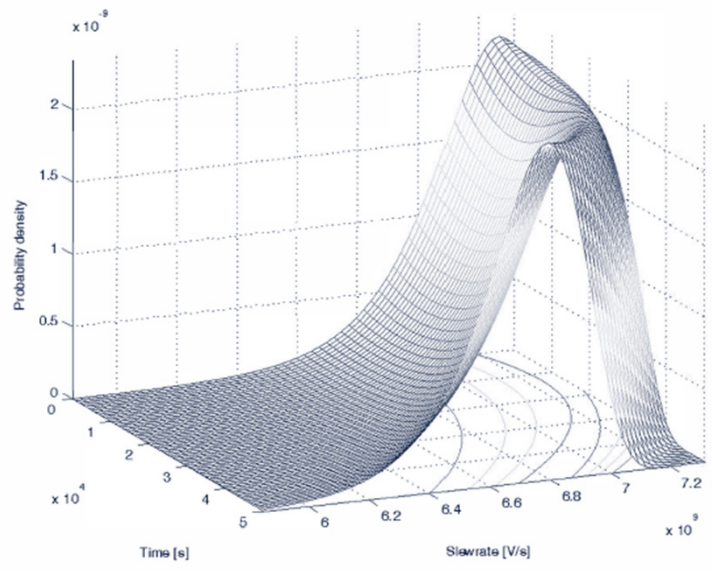


PVTA Interdependencies





PDF of Slew Rate



- Time dependent distribution function
  - transistor-, circuit and/or system performances
- Full PVTA at once
- Enables sophisticated system analysis

Time dependent distribution function

$$\mathcal{B}(t,x) = \frac{\frac{(\beta_k t^{\tau_k}+\gamma_k)(\beta_c t^{\tau_c}+\gamma_c)}{\beta_\alpha t^{\tau_\alpha}+\gamma_\alpha}\left(\frac{x}{\beta_\alpha t^{\tau_\alpha}+\gamma_\alpha}\right)^{\beta_c t^{\tau_c}+\gamma_c-1}}{\left(1+\left(\frac{x}{\beta_\alpha t^{\tau_\alpha}+\gamma_\alpha}\right)^{\beta_c t^{\tau_c}+\gamma_c}\right)^{\beta_k t^{\tau_k}+\gamma_k+1}}$$

Hillebrand et.al. Stochastic analysis of degradation and variations in CMOS-Transistors, ZUE 2015

Charge Based Stochastic CMOS Design

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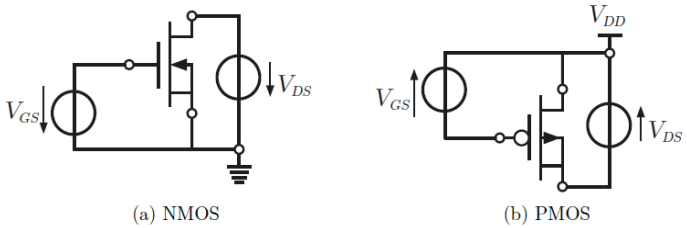
Test Bench for N-, PMOS

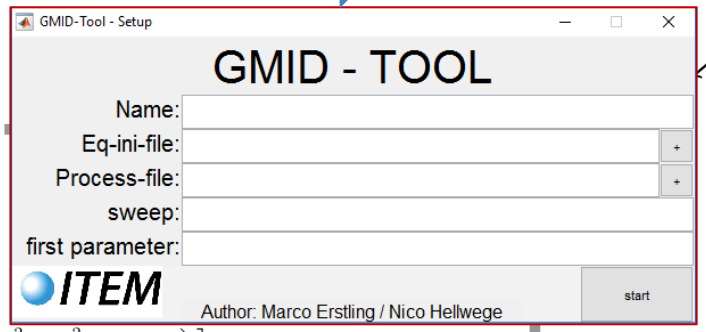
- W, L
- Temp. Vdd, Vgs, Vds
- Process degradation



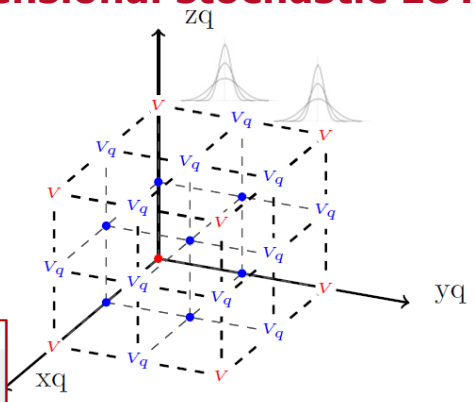
(a) NMOS (b) PMOS

$$f_n(\mathbf{x},t) = \frac{1}{\sqrt{2\pi}\sigma(t)} \exp\left(-\frac{1}{2}\left(\frac{\mathbf{x}-\mu(t)}{\sigma(t)}\right)^2\right)$$

$$f_{ln}(\mathbf{x},t) = \begin{cases} \frac{1}{\sqrt{2\pi}\sigma(t)\mathbf{x}} \exp\left(-\frac{1}{2}\left(\frac{\ln(\mathbf{x})-\mu(t)}{\sigma(t)}\right)^2\right) \\ 0 \end{cases}$$



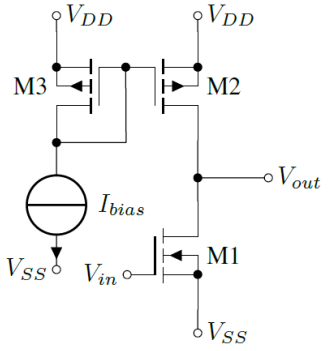
N-dimensional stochastic LUT



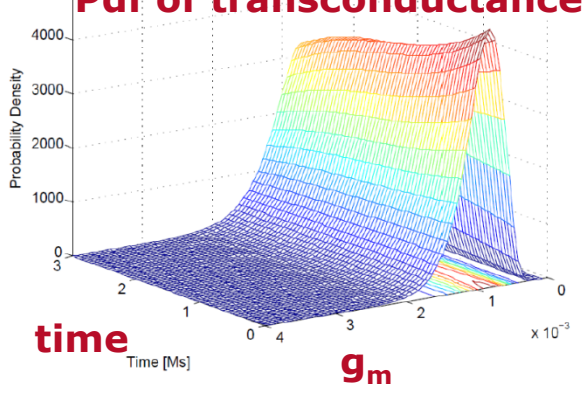
Equations for Circuit Performance

$$\mathbf{z} = \frac{\mathbf{x}}{\mathbf{y}} \quad \Leftrightarrow \quad g_m/I_D = \frac{g_m}{I_D}$$

$$f_z(\mathbf{z}) = \int_0^\infty \frac{\mathbf{y}}{2\pi\sigma_x\sigma_y\sqrt{1-r^2}} \exp\left[-\frac{1}{2(1-r^2)} \cdot \left(\frac{(\mathbf{yz})^2}{\sigma_x^2} - \frac{2r\mathbf{zy}^2}{\sigma_x\sigma_y} + \frac{\mathbf{y}^2}{\sigma_y^2} + h(\mathbf{y},\mathbf{z})\right)\right] \mathrm{d}\mathbf{y}$$



Pdf of transconductance



Sampled distribution functions, e.g.

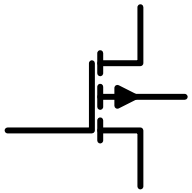
$$IC = \frac{I_D}{I_0 \, W/L} \qquad \frac{g_m}{I_D}$$

Hillebrand et.al. Stochastic LUT-based Reliability-Aware Design Method for Operation Point Dependent CMOS Circuits MIXDES 2016
Hellwege et.al. An Aging-Aware Transistor Sizing Tool Regarding BTI and HCD Degradation Modes, MIXDES 2015

Summary

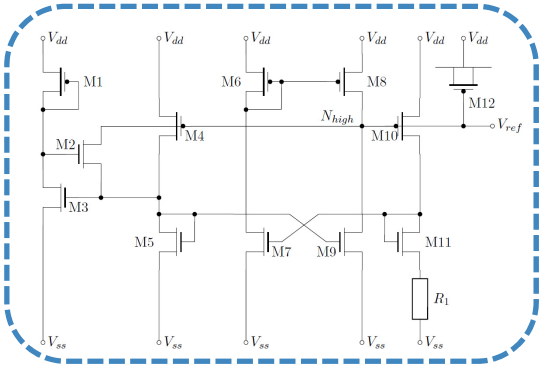
Unified Transistormodel

- Charge-based
- No V_{th}
- PVTA



Metrics

Circuit



- Consistent Environment
- Combination of analyses
- No extrapolation
- Arbitrary mission profile