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European Nanoelectronics Access

ASCENT

European Nanoelectronics Infrastructure Access

Nicolás Cordero

Funded by the European Union

Tyndall National Institute
Institiúid Náisiúnta

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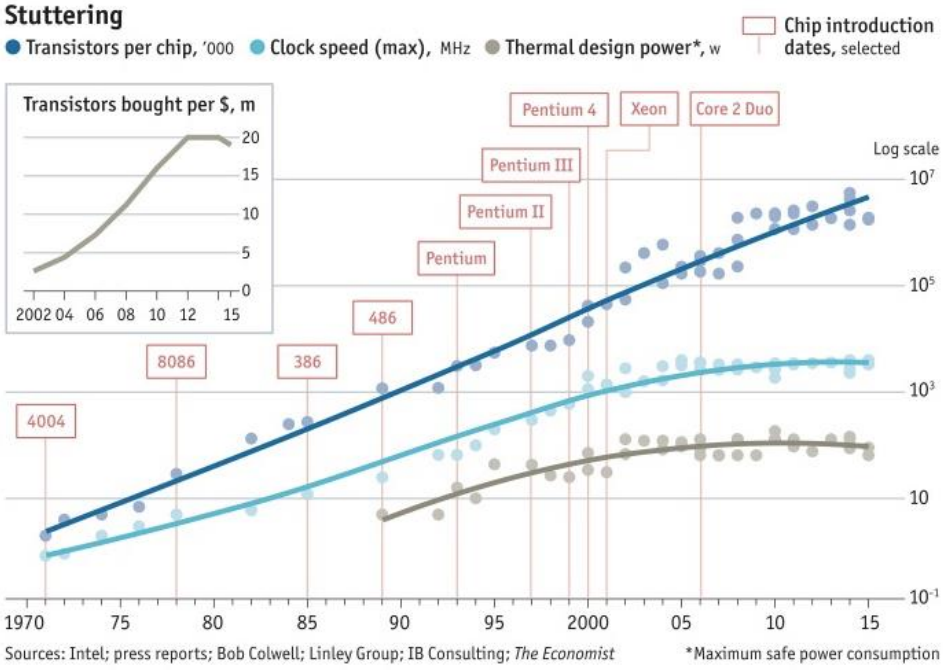
cea tech

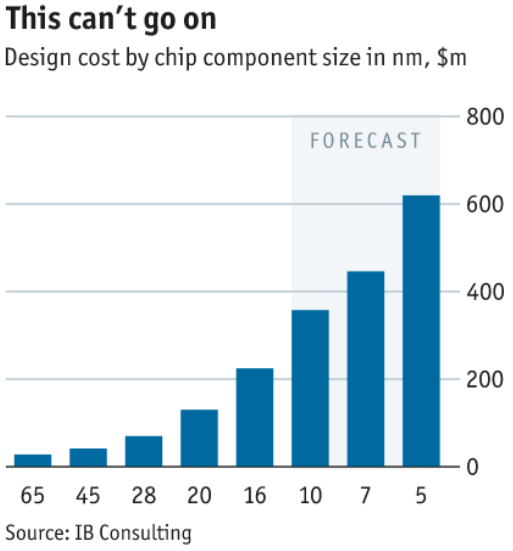
The Challenge

- Cost/performance returns by scaling are diminishing
- Cost to achieve tape out on new nodes is increasing

The Economist

Technology Quarterly
March 12, 2016





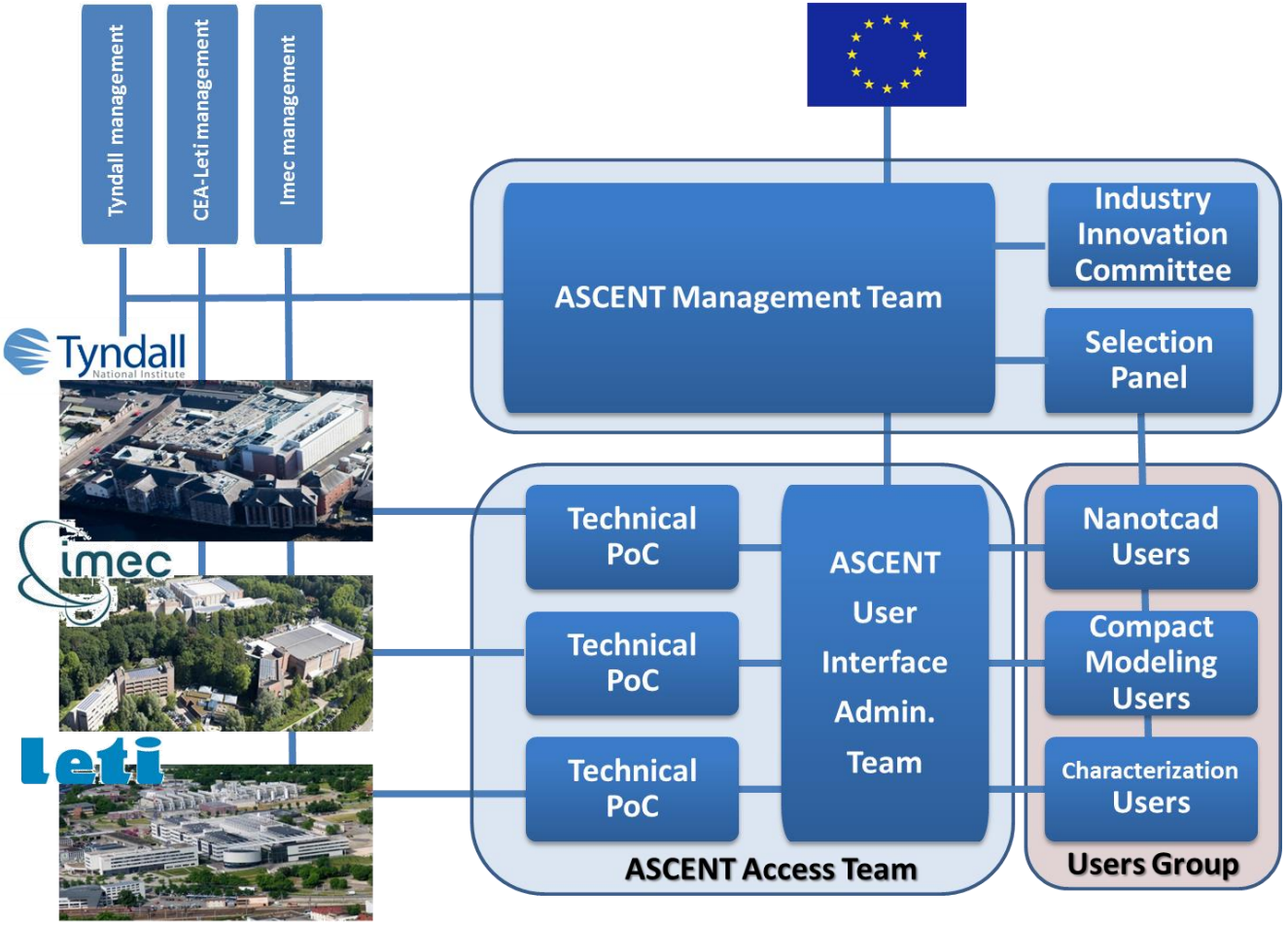
The infrastructure

A truly unique opportunity:

ASCENT combines Tyndall, imec and CEA-Leti's nanofabrication & electrical characterisation capabilities

into a single research infrastructure

and makes it accessible to all



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Objectives

ASCENT will:

- Leverage Europe's Unique advantage in nanofabrication to strengthen modeling and characterisation research community
- Accelerate development of advanced models at scales of 14nm and below
- Provide characterisation community with access to advanced test chips, flexible fabrication and advanced test and characterisation equipment
- Make project outputs available and easily accessible to nanoelectronics research community

ASCENT offers simplified access
to
advanced technology and research infrastructure

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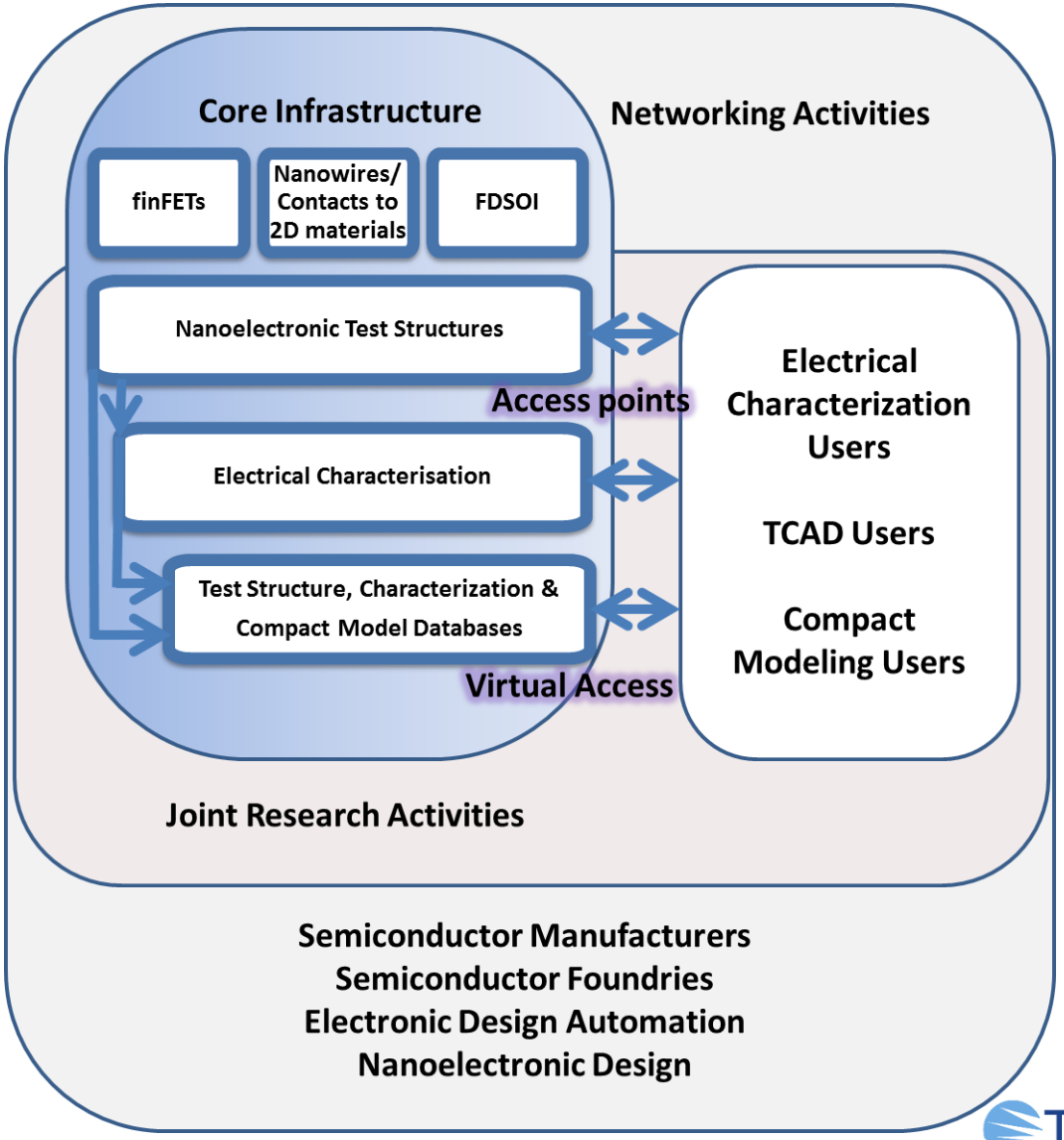
leti cea tech

ASCENT Network



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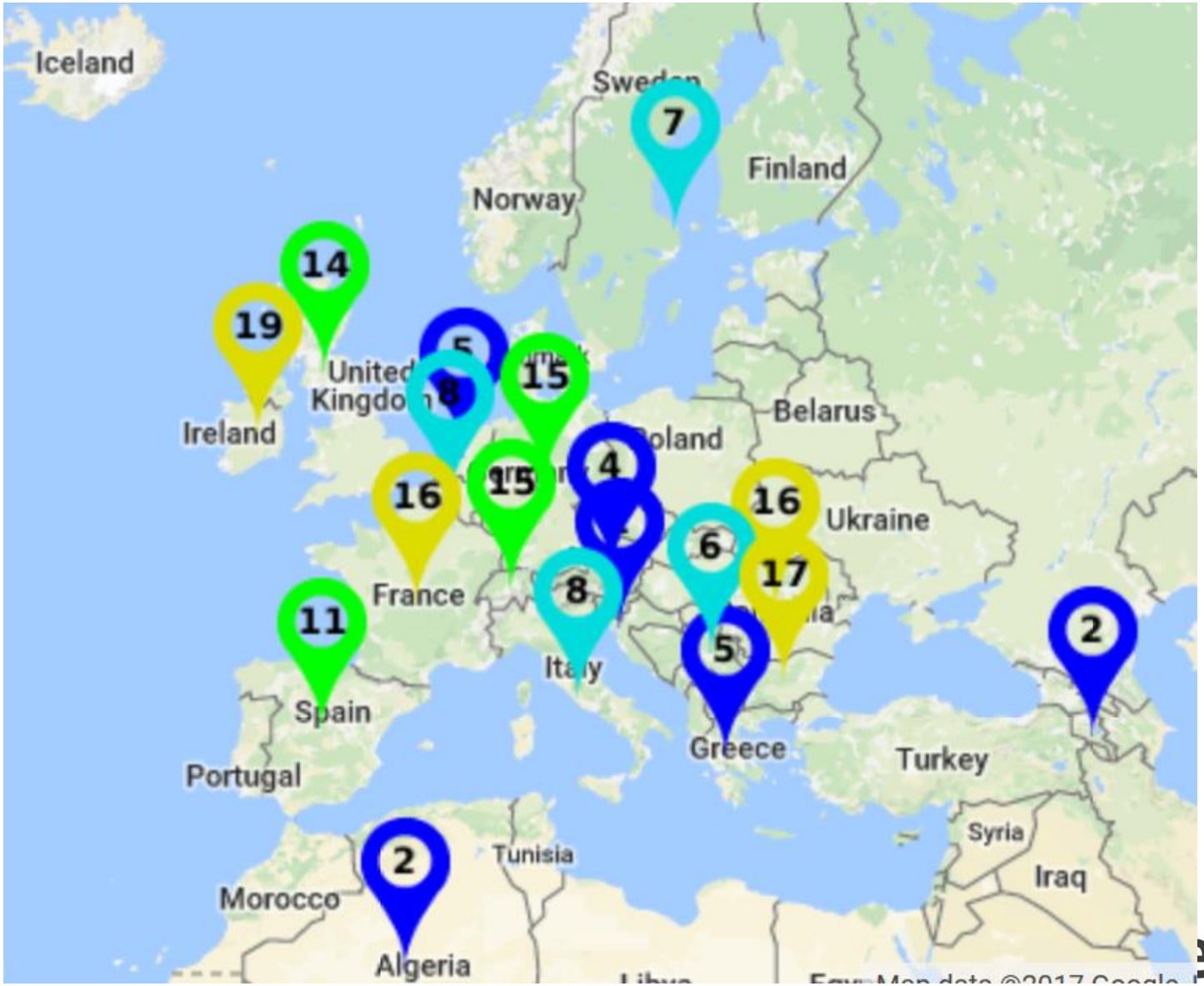
>220 members of ASCENT Network



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Committee Membership

Industry Innovation Committee

- Bernie Capraro
  - Intel
- Patrick Drennan
  - Qualcomm
- Ronald Gull
  - Synopsys
- Dominique Thomas
  - ST Microelectronics

Users Committee

- George Angelov
  - TU Sofia
- Asen Asenov
  - Uni Glasgow
- Francisco Gamiz
  - Uni Granada
- Benjamin Iñiguez
  - Uni Rovira i Virgili
- Andreas Schenk
  - ETH

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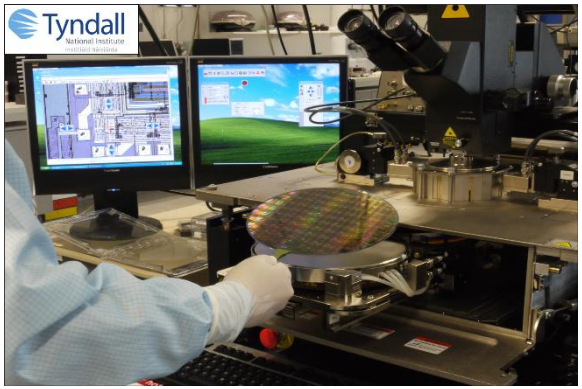
Access Provided

State-of-the-art **14 nm** bulk **FDSOI CMOS**

Advanced transistor and interconnect test structures

Electrical & nano-characterization platforms



Fabrication facilities for nanowires & 2D materials

Advanced nanowire and nano- electrode test structures

Electrical & nano-characterization platforms

State-of-the-art **14 nm FinFET CMOS**

Advanced transistor and interconnect test structures

Electrical & nano-characterisation platforms

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Access Provided

- Test wafer/chips
- Electrical Characterisation
- Physical Characterisation
- Nanoscale non-standard fabrication
- 14nm technology data (Virtual Access)

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FinFET 14/28nm Material for Device Analysis

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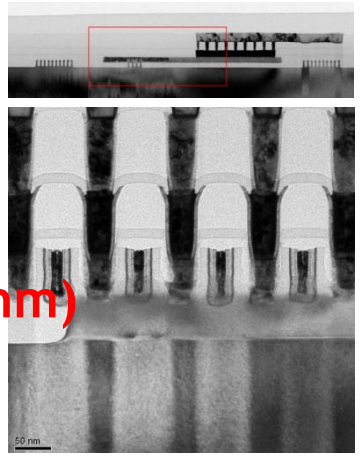
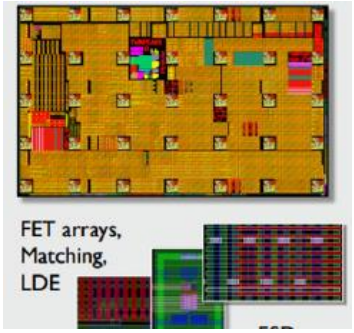
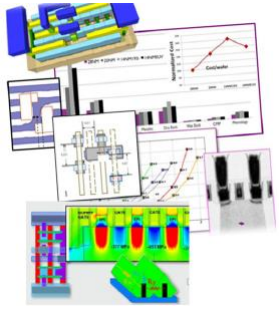
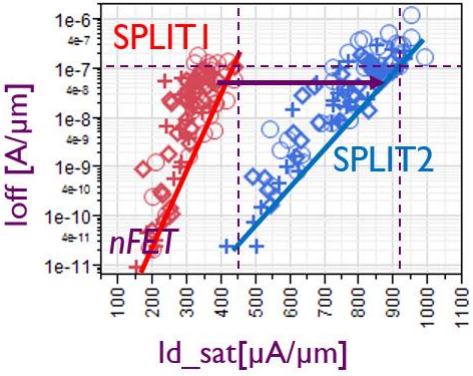
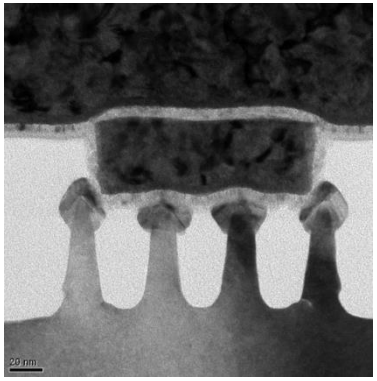


- Test chips/wafers
  - **300mm wafers with Bulk FinFET devices (14nm)**
  - **300mm wafers with Planar Metal Gate devices (28nm)**
- Digital and Analog/RF existing test chips
- Complete suite of test structures for Reliability/ESD/Matching/Local Layout effects/…
- Standard devices up to circuit level [Ring-Oscillators, …]
- State-of-the-art bulk FinFET device baseline









- Fin & STI module
- NFET wells I/I
- PFET wells I/I
- Well RTA
- Dummy gate
- NFET extension I/I
- PFET extension I/I
- Extension RTA
- NFET SiN dep & etch
- NFET recess
- NFET epi
- PFET SiN dep & etch
- PFET recess
- PFET epi
- Laser anneal
- ILD0
- RMG
- LI and BEOL

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FDSOI 14/28nm Material for Device Analysis

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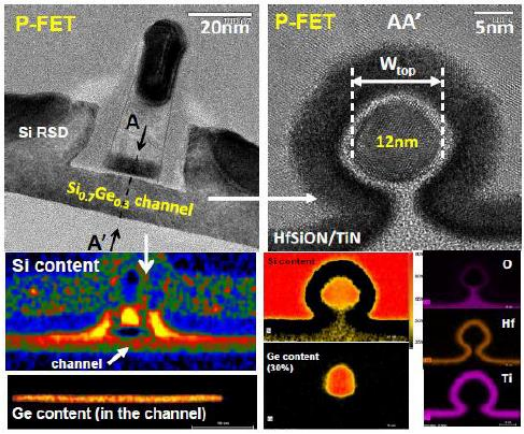
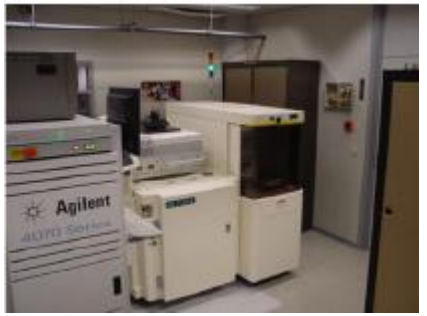
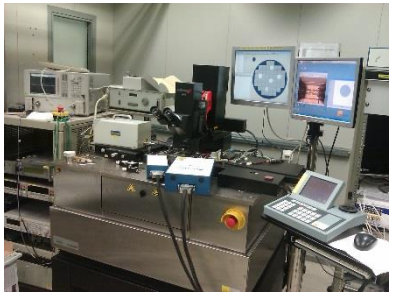
- **300mm wafers with planar FDSOI and Nanowire devices**
- SPICE models and model cards for digital: target and preliminary
  - 14nm FDSOI
  - 10nm FDSOI
  - 10nm FFSOI
- TCAD decks
  - FDSOI MOSFET
  - Trigate SOI Nanowire
  - GAA Nanowire MOSFET (mainly electrostatics)
- To come in the near future:
  - Spice model for Stacked NWs (7nm tech. node)

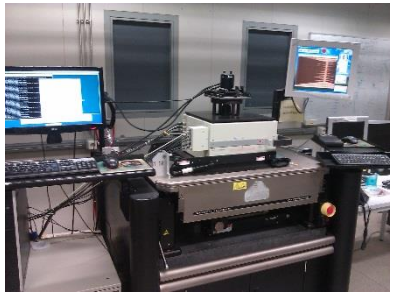


Electrical Characterisation

- >500 m^2 of test labs, ~ 25 semiauto/manual 300mm probers
- Statistical data treatment in JMP
- Fully and Semi-automatic 300mm parametric testers
- Temperature range for test on wafers 77/10K ➔ high T
- Fast Pulse testing, Self-Heating characterization
- HF tests up to 50 GHz
- Noise measurements
- Reliability tests: hot carriers, TDDB, charge pumping, …
- High power tests (10kV, > 100A) on 300mm prober
- Electrostatic discharge LAB

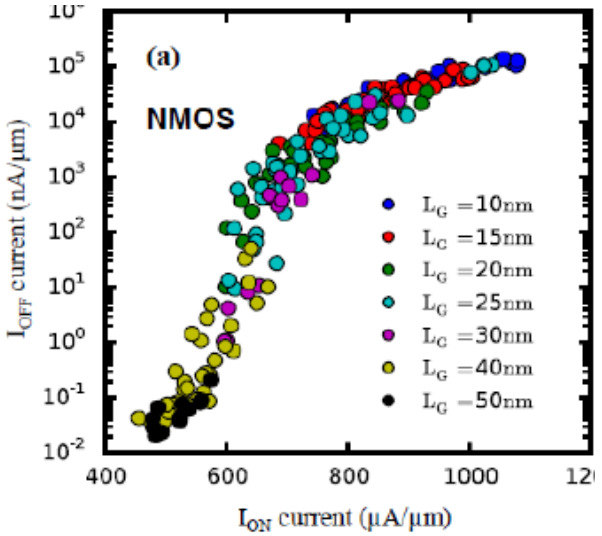


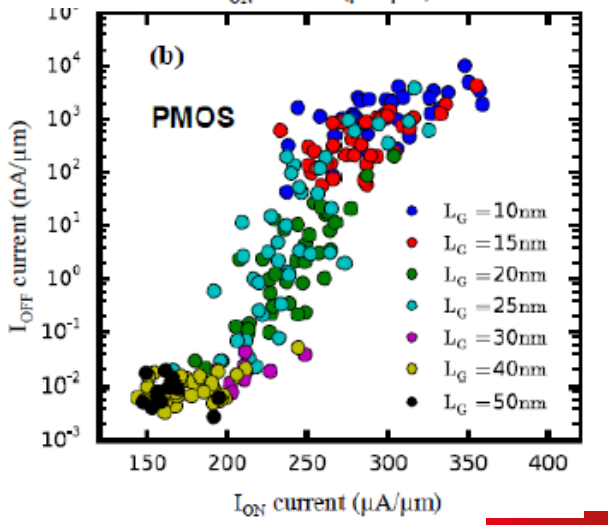




Electrical Characterisation

- Parametric testers with 300mm full auto probers
- Probe cards and new membrane cards
- Statistical data treatment
- Functional tests
- General purpose I(V)-C(V) 200/300mm testers
- Temperature range for test on wafers: 2K ⇒ 600°C
- Test systems for memories
- HF tests up to 40 MHz
- Noise measurements
- Reliability tests: hot carriers, TDDB, charge pumping, …
- Internal Photo Emission
- Emission microscopy (visible & infrared)
- Electrical test under calibrated strain
- High power tests (10kV, > 100A) on 300mm prober
- Deep Level Transient Spectroscopy
- Electrostatic discharges
- Electromigration
- Oven and climatic environments





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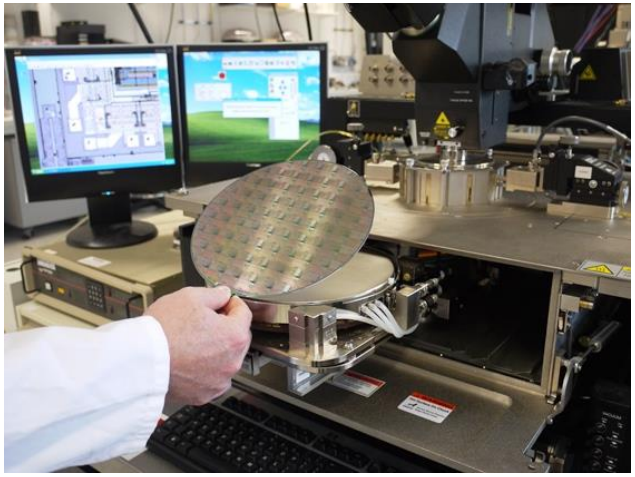
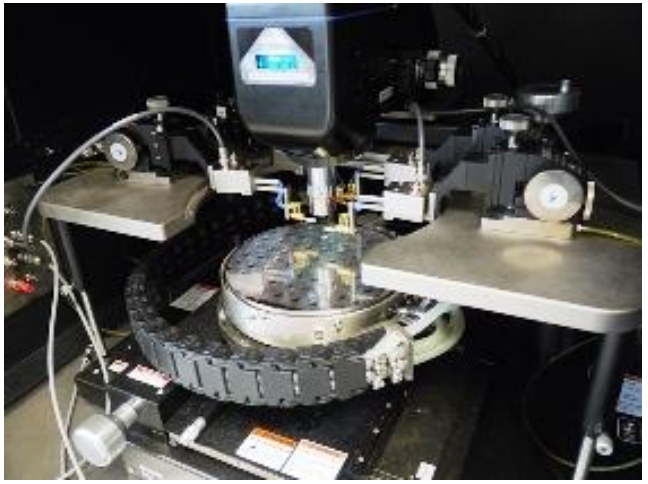
Electrical Characterisation Labs

Open Access Test Lab	Wide range of test equipment for device and wafer testing e.g.: impedance, capacitance, voltage, current, spectrum analysers, …
Nanoscale Test Lab	Variable Temperature, Micromanipulator Probe Stations
Reliability Test Lab	Wide range of test equipment for packaged devices





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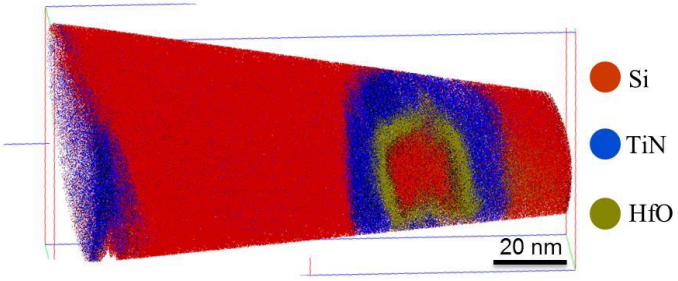
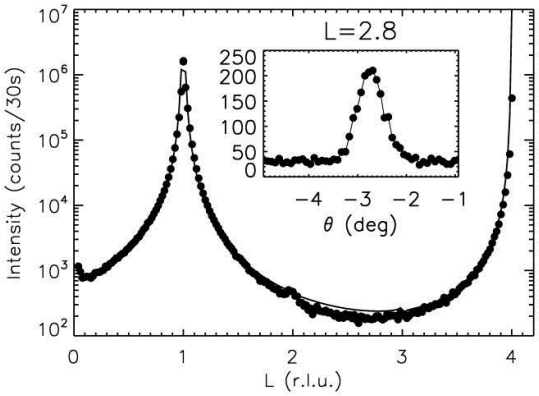
Physical Characterisation

- Atomic Force Microscopy
  - *Dimension AFM Icon/Fast Scan Bruker working under glovebox (O2, H2O < 1 ppm)*
- High Resolution Transmission Electron Microscopy
  - *FEI TECNAI G2 F 20*
  - *FEI TITAN THEMIS 80-200 kV*
- ToF-SIMS
  - *ION TOF ToF SIMS 5*
- Atom Probe Tomography
  - *CAMECA FlexTAP Atom probe*
- XRD (X-ray Diffraction)
  - *Diffractometer - Smartlab RIGAKU - 5 circles*
- XPS (X-ray Photoelectron Spectroscopy)
  - *Spectrometer/microscope - PHI VERSA PROBE II*
- Ellipsometer
  - *Ultraviolet-visible ellipsometer - HORIBA JOBIN YVON UVISEL*





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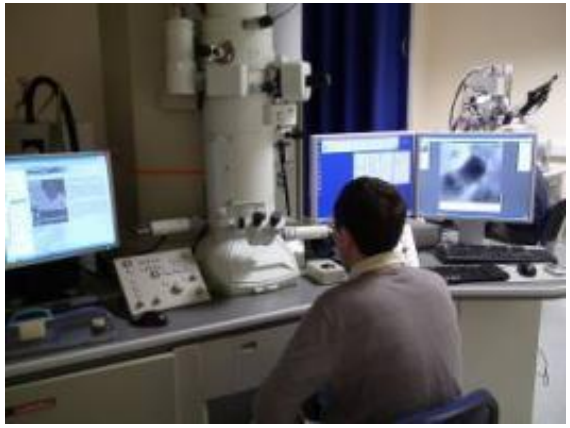
Physical Characterisation Labs

Electron Microscopy Facility	High Resolution TEM, SEM and FIB, EDAX capability
Nanoscale Characterisation	AFM, SEM and electrical characterisation
Optical Spectroscopy Labs	Raman & Optical Spectroscopy, fluorescence microscopy
Magnetic Characterisation	SQUID magnetometer for nano magnetic materials
Package Characterisation	Scanning Acoustic microscope, X-ray analysis



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Nanoscale fabrication

Range of cleanrooms designed for flexible process & product development

- Silicon MOS Fabrication
- MEMS Fabrication
- Compound Semiconductor Fabrication
- Photonics Fab Training Facility
- e-beam Lithography
- Non-standard nano-processing

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Focussed Ion Beam (FIB)

Complete nanotechnology lab in one tool

- High resolution pole piece – point-to-point resolution of 0.21 nm
- EDS, Oxford instruments, INCA 250, site-lock drift correction system for high resolution elemental mapping
- In-situ STM-TEM holders, high temperature TEM holders
- STEM mode with BF and HAADF detectors (0.8 nm resolution)
- Oxford Instruments X-MAX 80 for high productivity EDS analysis
- Cryo preparation for liquid and gel-like materials

JEOL 2100 HR-(S)TEM / FEI Helios NanoLab DB-FIB

Nanoscale Technology Data (Virtual Access)

- FinFET and GAA test chip documentation and DATA (14nm)
  - Documentation of process assumptions for the test chips
  - Inventory of test structure types available on the test chips
  - Access to test structures data
- III/V InGaAs GAA test chip documentation and DATA
  - Documentation of process assumptions for the test chips
  - Inventory of test structure types available on the test chips
  - Access to test structures data
- PLANAR test chip documentation and DATA (28nm)
  - Documentation of process assumptions for the test chips
  - Inventory of test structure types available on the test chips
  - Access to test structures data
- FDSOI: PDK for Full custom IC design
  - 14nm planar FDSOI technology
  - 10nm planar FDSOI technology (preliminary)

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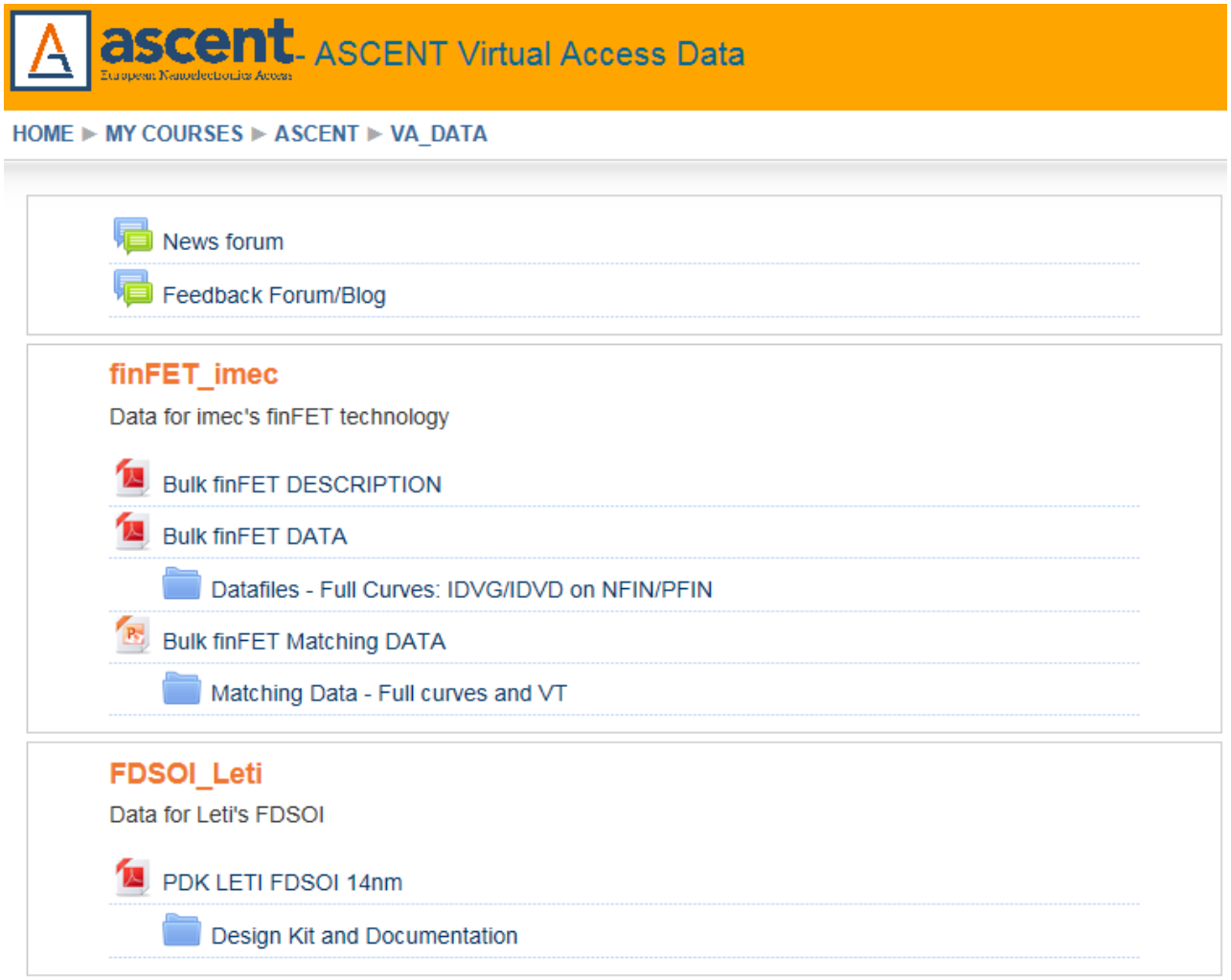
Virtual Access Data available



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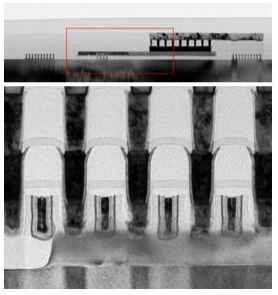
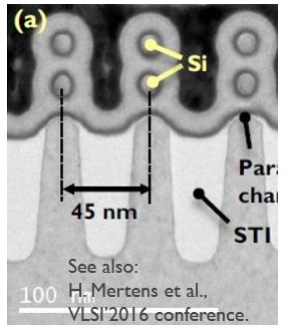
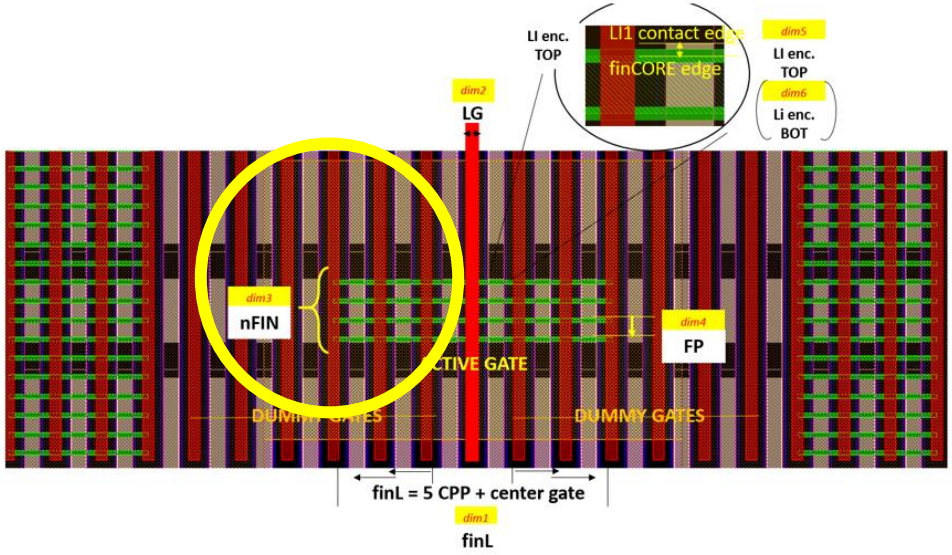
imec bulK FinFET data





- Access to bulk finFET and GAA_SiNW data
  - Integrated dual WFM CMOS
  - LG range 24nm → 90nm within pitch and long channel devices
  - nFIN from 2 to 22
- Room T available
  - 50°C or higher T next
  - Low T can be considered
- DOE for contact, layout effects,...



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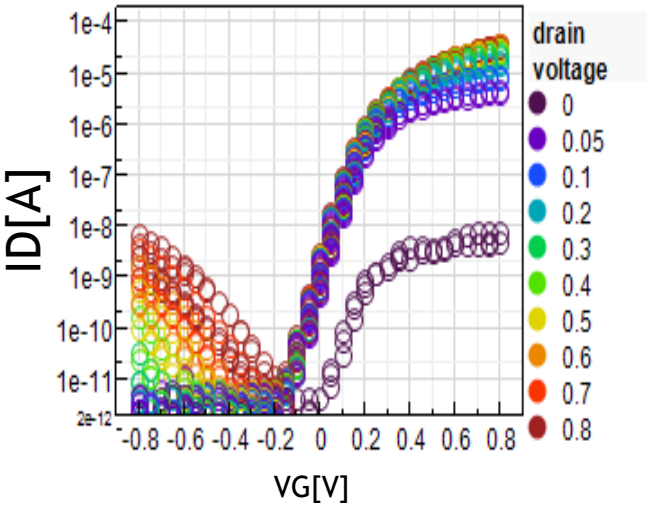
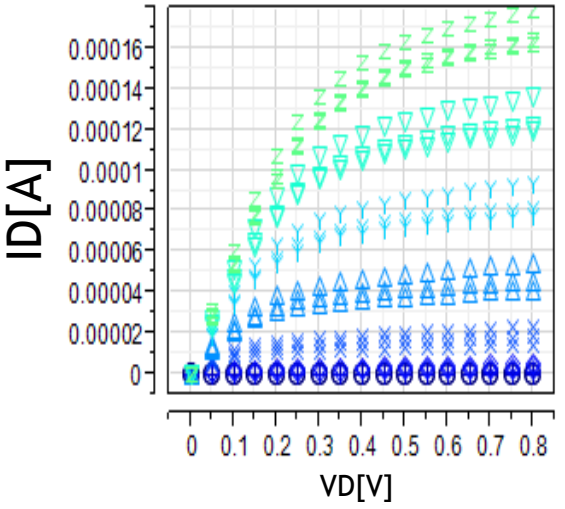
imec bulK FinFET data

- Access to raw data and extracted FoM's
  - Threshold Voltage, Mismatch
  - DC metrics and ID-VD, ID-VG characteristics
  - FEOL/BEOL R/C and Ring-Oscillator circuits
- Full sweep data in VA
  - Covers range of VG/VD and LG/nFin
- Analog FoM, Reliability testing, ESD,...
- Available for subsequent model validation





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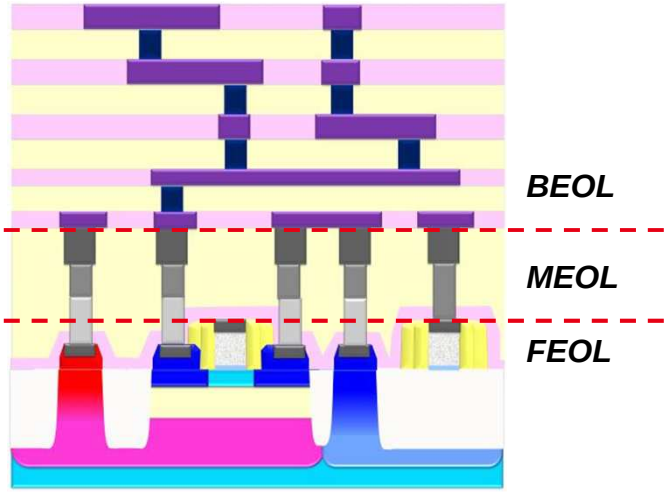
PLANAR 14NM FDSOI TECHNOLOGY FOR BENCHMARKING

- CPP = 90nm
- Nominal supply voltage Vdd=1V

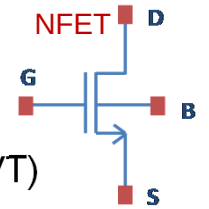


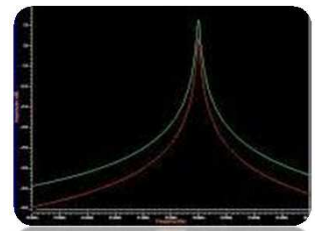
- **BEOL:**
  - Metal levels: Metal 1 to Metal 5,
  - Pitch = 64nm (similar to 20nm bulk)
- **MEOL:**
  - Trench contact
  - Metal0
- **FEOL:**
  - FDSOI transistor with Lmin = 20nm
  - Standard Well definition (similar to bulk) with possible back-biasing up to Vdd
- **DRM:**
  - simplified design rules

FULL CUSTOM DESIGN FLOW

Technology

Devices Library:
→ N/P FET (multi-VT)
→ Spice Modeling





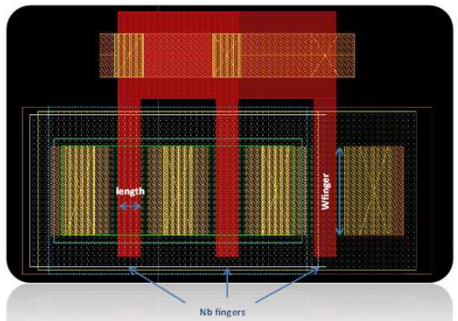
Design Library Simulation

PDF

DRM, Reference manuals

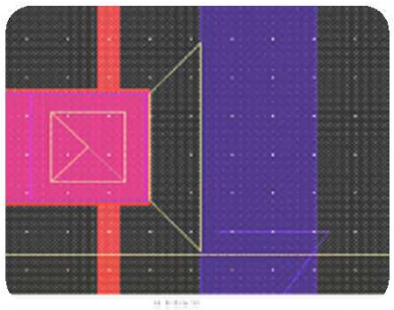
Layout

Parameterized cells
(MOS Pcells)



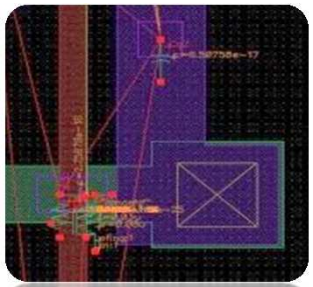
Verification (DRC/LVS)

→ Design Rules Checking
→ Extraction Devices

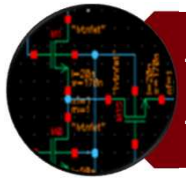


Post-Layout Simulation

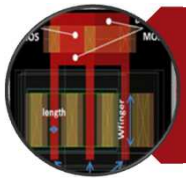
→ Parasitic extraction (PEX)
→ RC Simulation



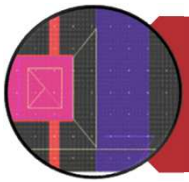
PDK FDSOI 14NM CONTENTS



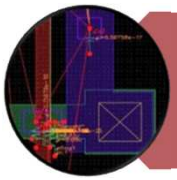
- Electrical simulation for design performance (Schematic → Netlist)
- SPICE Model: library of MOSFET devices (UTSOI2) integrated



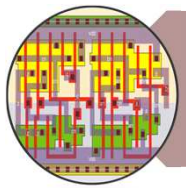
- Layout: physical implementation of all technological layers (Techfile)
- Pcell: library of parameterized MOSFET for layout automation



- Design Rules Check (DRC): deck file describing all design rules (DRM)
- Layout Versus Schematic (LVS): comparison layout vs simulation



- Parasitic EXtraction (PEX): extraction of parasitic elements (RC)
- Post-Layout Simulation (PLS): netlist simulation with RC elements



- Digital Library: preliminary basic logic cells for Power Performance Area (PPA) analysis, architecture definition (template)

LIBRARY NAME: DK_FDSOI14LIB

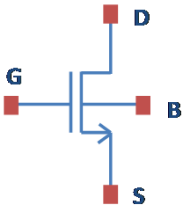
Library

- Technological file include technology, layer information, display and layer map files,
- Based on the OpenAccess Database

Symbol

- Symbol library contains 8 variants of device symbols for MOS => 8 n/p fet (SVT1/SVT2/LVT/HVT),
- Associated SPICE models for simulation

LVTNFET

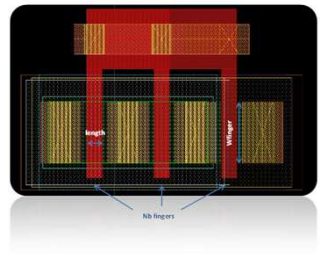


Parameters:

l : 20nm
w : 46nm
nf : 1
m : 1

Pcell

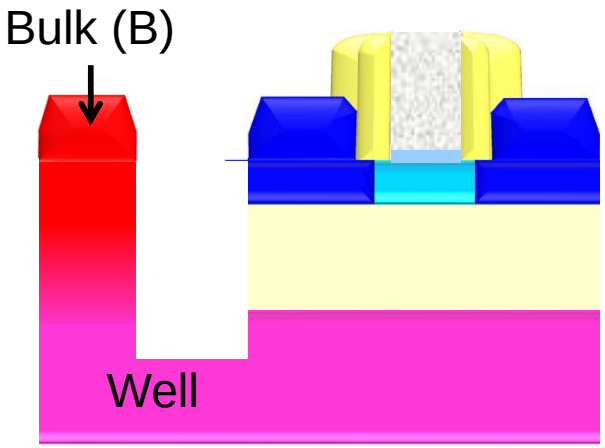
- MOS parameterized cells available to reduce layout time and design rule mistakes,
- Pcells manage all kinds of MOS devices and all VT options



SPICE MODEL FOR FDSOI: UTSOI2

- The UTSOI2 compact model was developed to describe the electrical behavior of FDSOI transistor: especially back biasing effect
- Several versions are available in major IC simulators (Eldo, Spectre, Hspice, ADS,...)

- The FDSOI MOSFET is a 4 pins device as bulk



FDSOI MOSFET is symmetric:
drain ⇔ source: no junction as in bulk

<u>Included in device library:</u>
Parasitic effects: Area SD region (AS-AD)
Stressor effects: Continuous RX, Isolated MOS
Pre-layout effects: R, C, R+C

MULTI-VT DESCRIPTION FOR BENCHMARKING

VT definition in PDK: several gate workfunctions

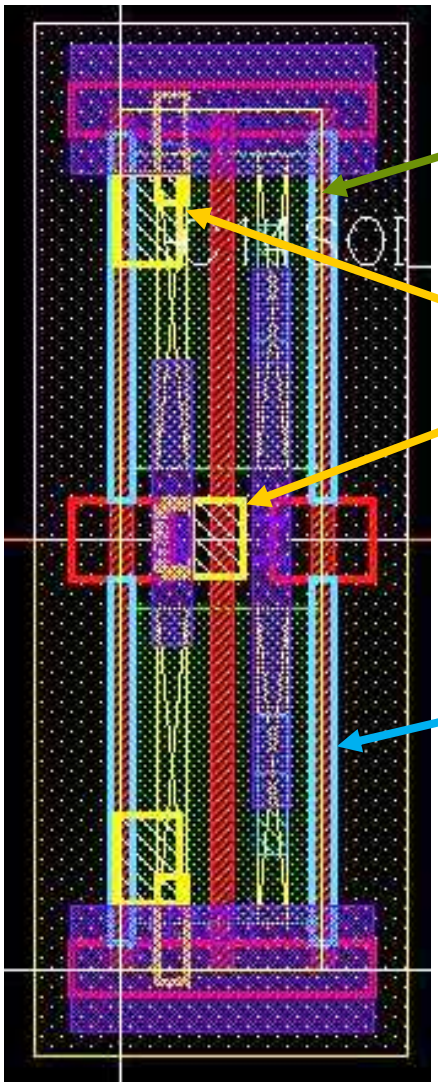
VT	Description	Well for nfet	Well for pfet
LVT	Low-VT	N	P
SVT1	Standard-VT1	N	P
SVT2	Standard-VT2	P	N
HVT	High-VT	P	N

Multi-VT platform can be managed using several solutions:

- Poly-biasing: Lnom + x nm
- Back-biasing: for example +Vdd under nfet
- Gate workfunctions

Multi-VT strategy is foundry-dependent

LAYOUT STRATEGY



Continuous RX: used for increasing devices performance

Poly pitch: value is 90nm

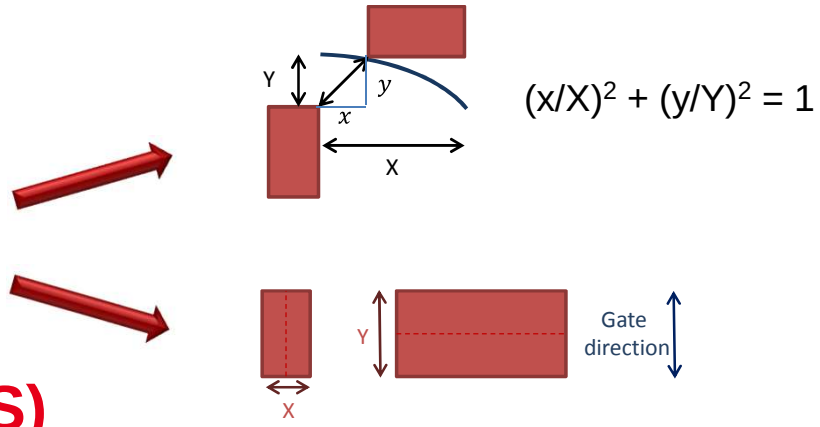
Special Construct: used for MEOL layers in dedicated areas. To highlight special construct, used the associated marker (MKR_ SpeConst). This allows to waive a set of default rules and check some other specific design rules (see DRM for more details)

MKR_GateTie: this marker must be placed on poly regions.

These gates are formed each time we want to abut 2 devices which don't share the same active regions. The device we are getting is a transistor in OFF state called gate tie. With this marker, the LVS will be able to extract this device

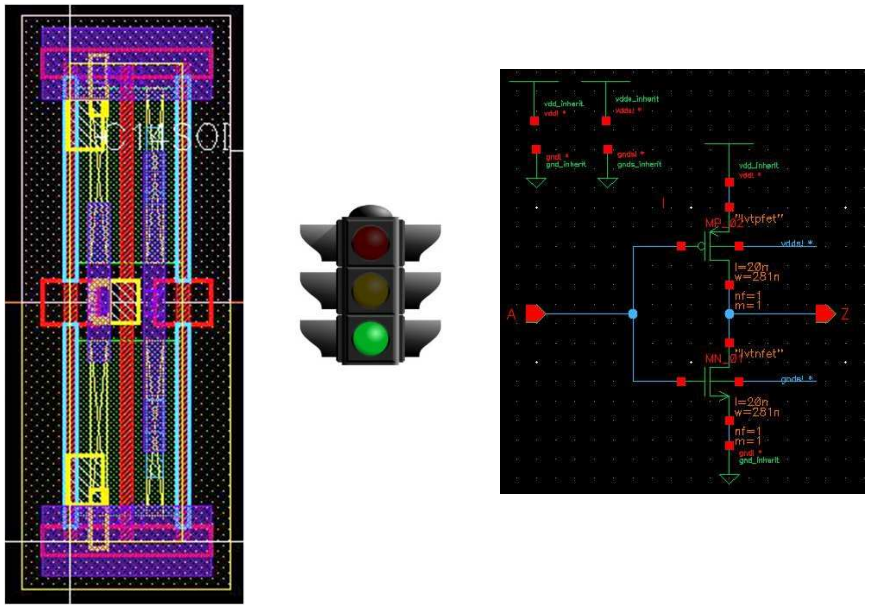
Design Rules Checking (DRC)

- DRC deck file manage:
  - One-Dimensional check,
  - Multi-Dimensional check,
  - Interdependent Multi-Layer check



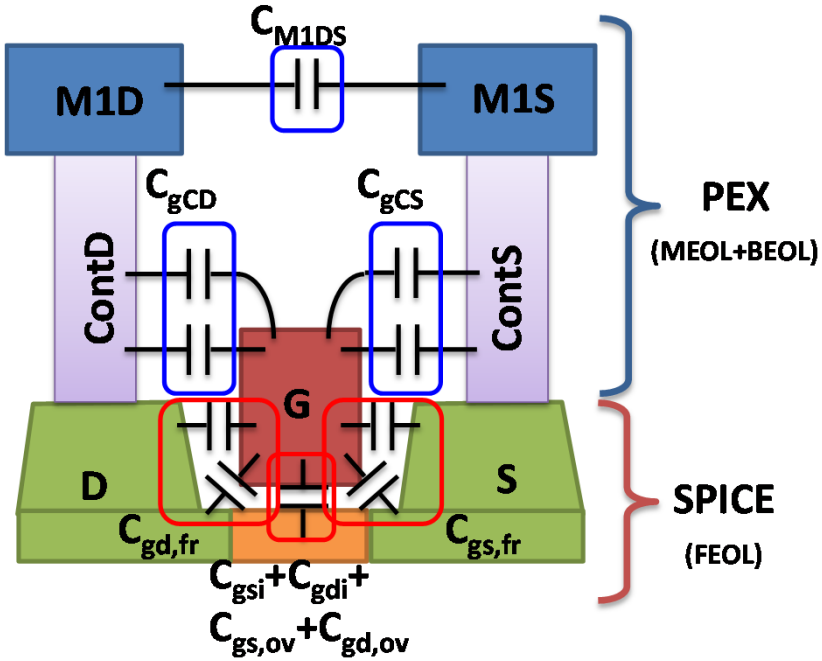
Layout Versus Schematic (LVS)

- MOS devices extraction:
  - VT option & Gate Tie device
  - Well-tie for Back-gate control
- MOS parameters extraction:
  - Geometry: l/w/nf/m
  - Area: as/ad/ps/pd
  - Stressor effects: sa/sb/sd
- Connectivity declaration

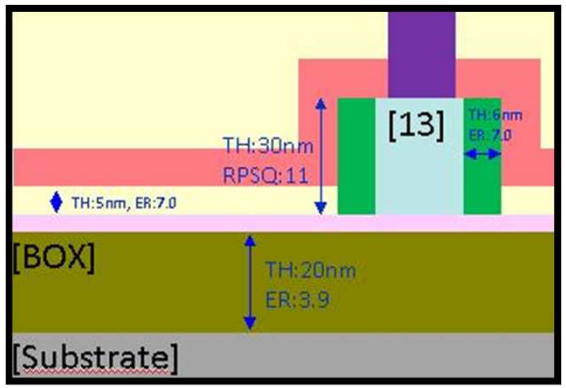


POST-LAYOUT SIMULATION:

- Parasitic extraction files:
- → Technological and mapping files,
- → Nominal (corners not available)
- 2 descriptions: StarRC / xCalibrate,
- Ignore FEOL capacitances (SPICE)
- Metal resistance included



IGNORE_CAPACITANCE
(embedded in SPICE model)



Description of the FDSOI cross-section:
➡ *DIELECTRIC / CONDUCTOR / VIA*

Technological information:
➡ *THICKNESS / PERMITTIVITY / RESISTIVITY*

Output: netlist including RC parasitic elements for PLS

CAD TOOLS RECOMMENDATION

Flow	CAD tools & releases
Framework	Virtuoso **(Cadence) release IC6.1.5.500.9**
Simulator	Eldo (Mentor) release 13_2c HSPICE (Synopsys) release 2013.03-SP2
DRC/LVS	Calibre (Mentor) release 2015.1_14.11
PEX	Star-RC (Synopsys) release 2012.12-SP2 Calibre (Mentor) release 2015.2.19.13

Virtual Access Users

Ref	User	Institute	Country
002	G. Angelov	T.U. Sofia	Bulgaria
006	G. Fatin	Univ. Maynooth	Ireland
008	A. Durgaryan	Synopsys	Armenia
022	A. Nejadmalayeri	Phoelex Ltd (SME)	UK
031	X. Wang	Univ. Glasgow	UK
035	K. Miyaguchi	IMEC	Belgium
036	G. Ghibaudo	IMEP-LAHC/INPG	France
037	F. Gamiz	Univ. Granada	Spain
043	M. Karner	GlobalTCAD Solutions GmbH	Austria
045	T. Kelly	EOLAS Designs	Ireland
047	A. Pezzotta	EPFL ICLAB	Switzerland
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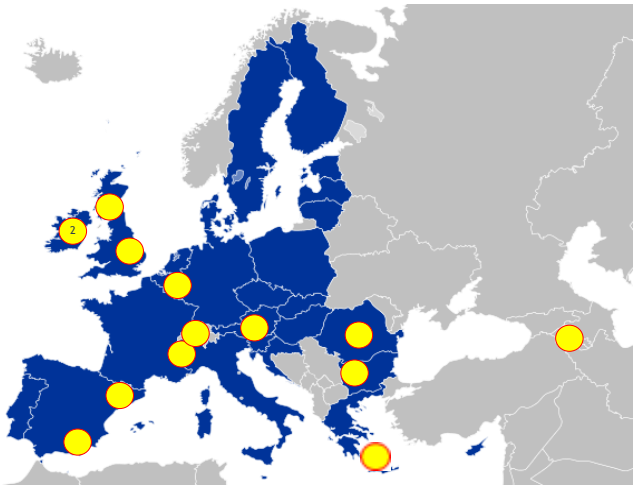

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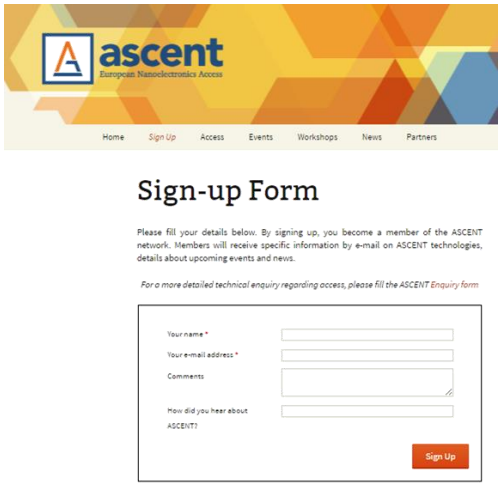

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