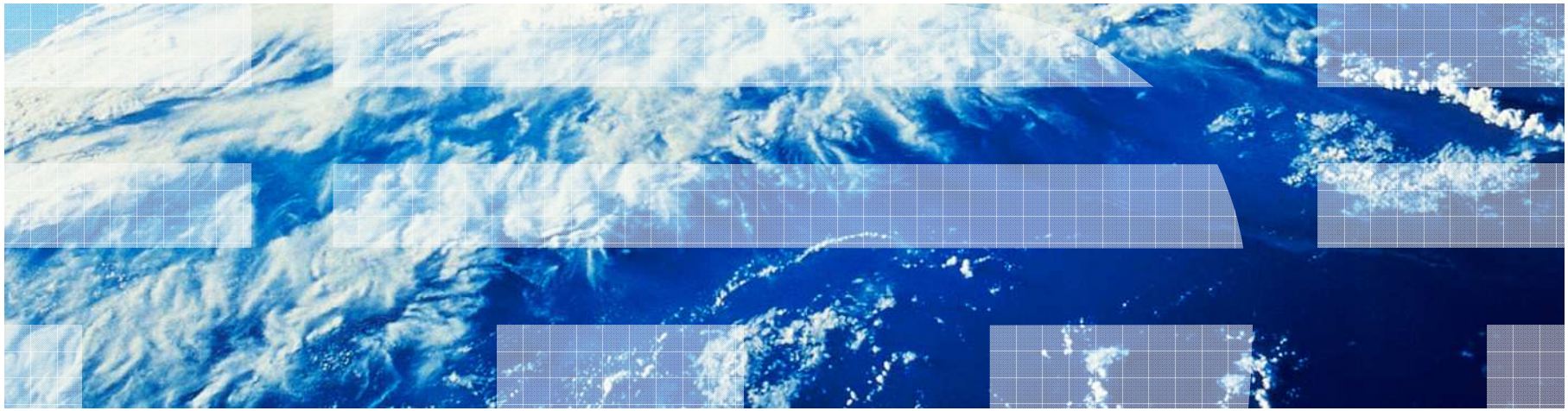
High Voltage MOSFET Technology, Models, and Applications

Vaidyanathan Subramanian, PhD

200mm Foundry Enablement

IBM Systems and Technology Group (STG)

Email: vaisubra@in.ibm.com



© 2009 IBM Corporation

Outline

- Introduction to HV MOSFETs
- IBM's HV value proposition
- IBM's HV PDK offering
  - Technology
  - Devices
  - Models
- Recent publications, highlights
- Summary

© 2009 IBM Corporation

High Voltage MOSFETs

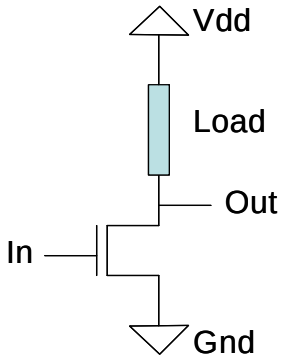
- High Voltage MOSFETs are those that can support a higher VDS & ID than regular MOSFETs
- Because of this versatility they are used
  - To switch loads ON/OFF
  - To up- or down-convert between different voltage levels, or more generally, for Power Management
  - To provide high-power amplification
  - … And many more

© 2009 IBM Corporation

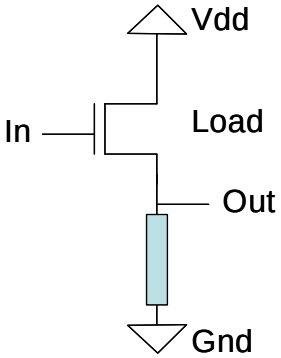
Basic HV MOSFET circuits (building blocks)

Switch

Low Side Switch

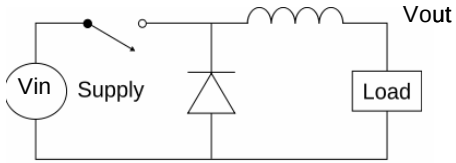


High Side Switch

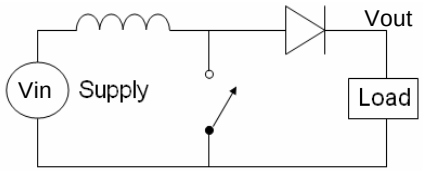


Voltage Converter

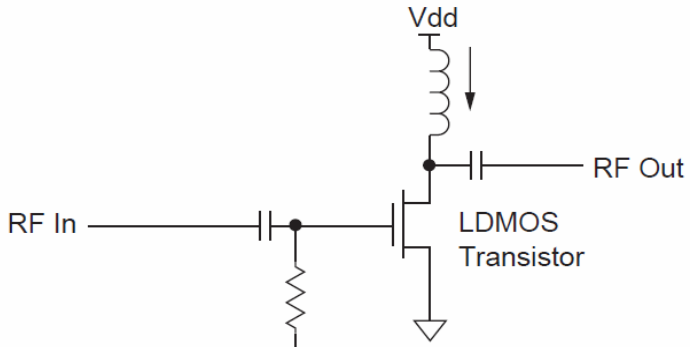
Vout < Vin; 'Buck' converter



Vout > Vin; 'Boost' converter



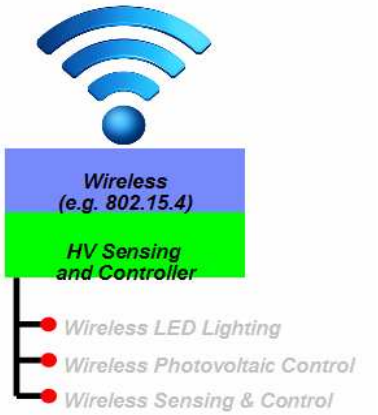
Amplifier

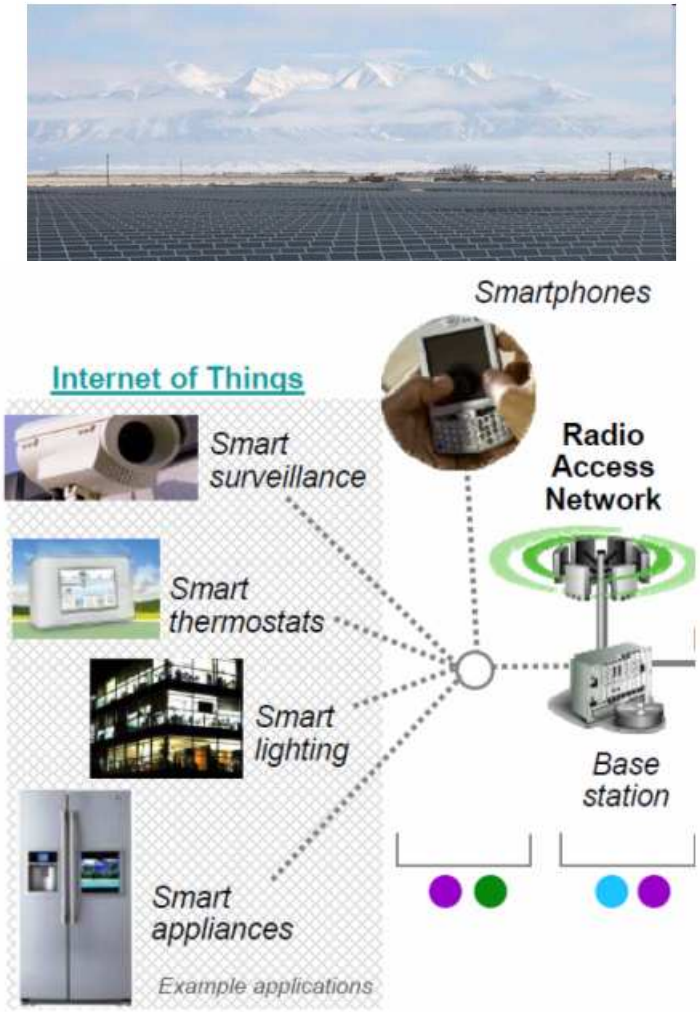


© 2009 IBM Corporation

End applications of High Voltage Technology

- Consumer electronics
- Home appliances
- Automotive
- Medical
- Commercial & industrial lighting
- Controls
- Energy
- …And more



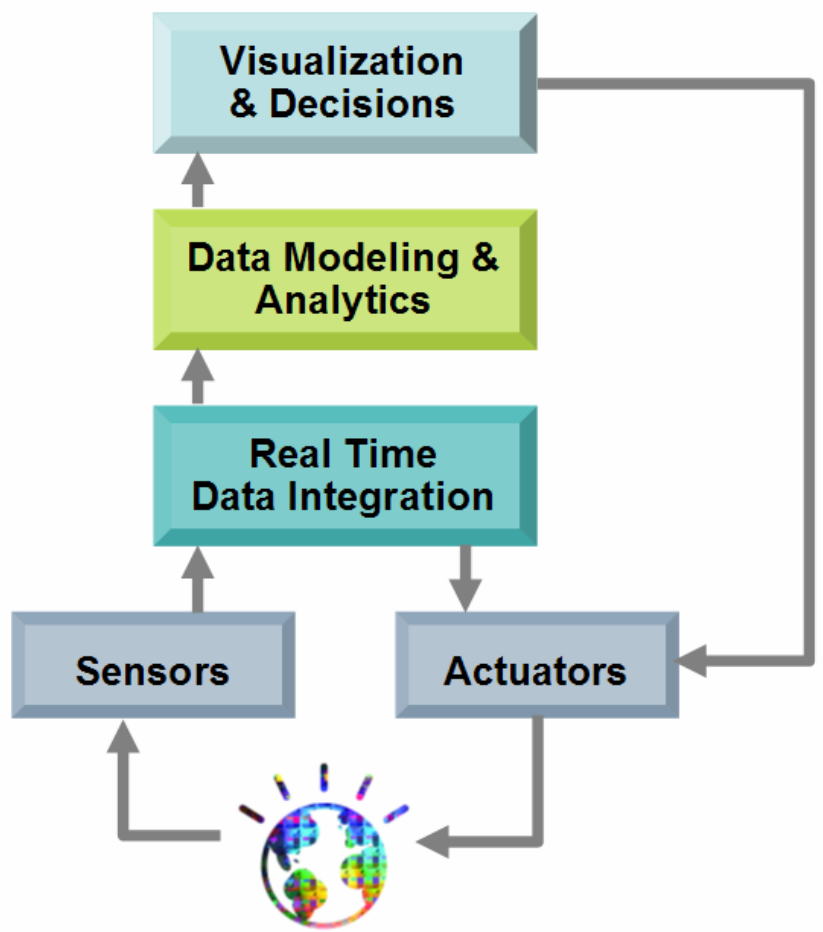


Applications of HV technology are in almost every aspect of modern life

© 2009 IBM Corporation

High Voltage Technology for a Smarter, Greener Planet

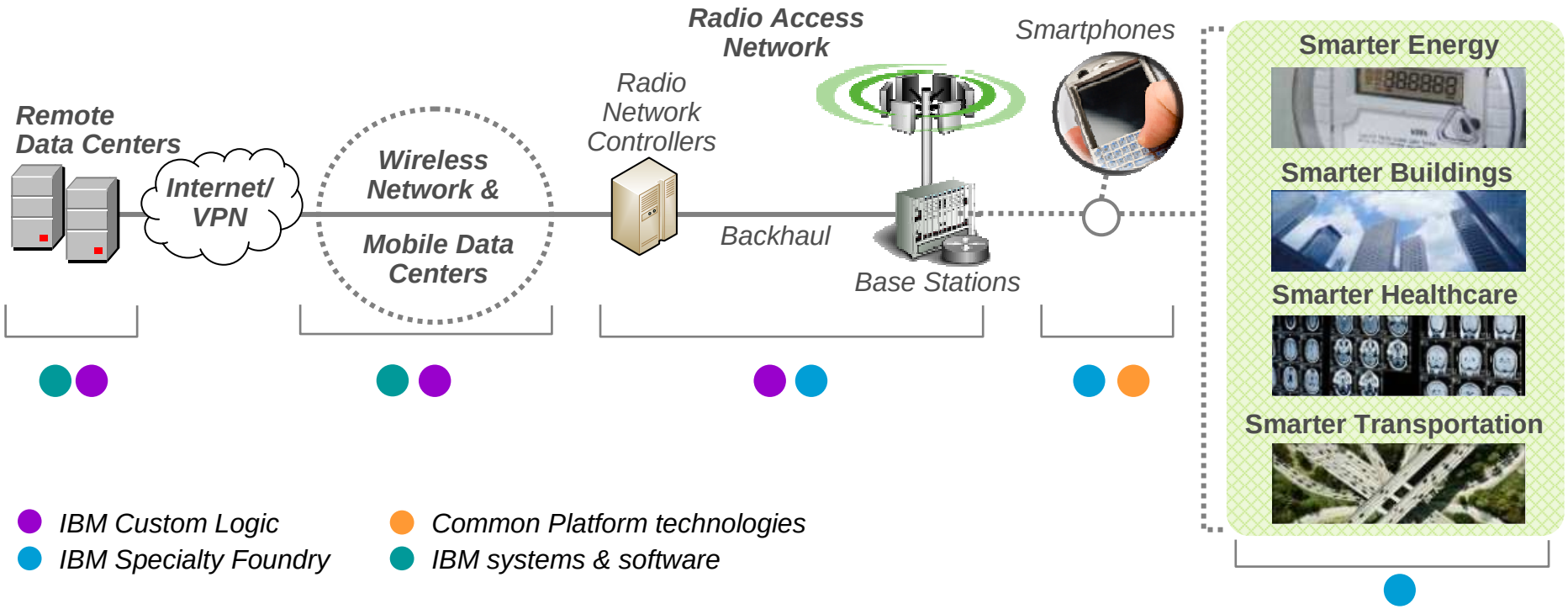
- High Voltage Technology can help in the following ways
  - A more efficient switch implies reduced switching losses, resulting in reduced power consumption
  - If the above switch can be controlled remotely (wirelessly), it translated into even more savings in power
  - Above (switch with wireless control) approach can be used not only to *save* power, but also to *harness* power



High Voltage technology contributes to a Smarter, Greener Planet

© 2009 IBM Corporation

How IBM technology fuels a Smarter Planet, from smarter computing to smarter devices



IBM's USP is in providing a complete ecosystem for implementing end-to-end solutions encompassing digital, wireless and High Voltage technologies

© 2009 IBM Corporation

Smarter Silicon Applications

Smarter Energy

- IBM offers unique RF + HV integrated solution which enables reliable, inexpensive Maximum Power-Point Tracking (MPTT) for solar panels
- Panel-Level Smarter Energy solution boosts the energy efficiency from 10-30%

Smarter Buildings / Industrial Control

- Seamless integration of digital, analog, power and RF enables more cost effective sensor and actuator designs
- Industrial rated technology 10+ year lifetime. High temp (150 C) rated for hostile environments

© 2009 IBM Corporation

Smarter Silicon Applications

Smarter Lighting

- LED lighting is the future due to its potential for cost + energy savings
- Unique RF + HV integration capability enables new class of LEDs capable of remote control and management
- Wide range of voltages to enable wide range of LED applications
- Seamless integration of digital, analog, power and RF in single SoC
- Industrial rated technology 10+ year lifetime. High temp (150 C) rated for hostile environments

© 2009 IBM Corporation

Outline

- Introduction to HV MOSFETs
- IBM's HV value proposition
- IBM's HV PDK offering
  - Technology
  - Devices
  - Models
- Recent publications, highlights
- Summary

© 2009 IBM Corporation

IBM's High Voltage PDK offering: CMOS7HV

First IBM Technology for Power-Management Chips
Brings new functionality to critical infrastructure

ARMONK, N.Y., Sept., 16, 2010 – IBM today announced innovative new chip-making technology for power-management semiconductors – the company's first foray into a segment seen as critical to the development of alternative energy sources, smart buildings and new consumer devices.

IBM's process integrates wireless communications into a single power-management chip, a first that cuts production costs (20% or more) to allow chip designers and manufacturers to create a new class of semiconductors – ultra-small and affordable chips that control power usage while they communicate in real-time with systems used to monitor "smart" buildings, energy grids and transportation systems.

"Advanced power management techniques will become increasingly important to support new forms of energy, communications and entertainment," said Regina Darmoni, IBM Microelectronics. "By integrating new functions such as wireless communications, IBM's process gives a head start to manufacturers who are looking to bring new advancements to consumers."

IBM is rolling out the new chip-making process to manufacturers in the consumer electronics, industrial, automotive, digital media and alternative-energy segments. The company's semiconductor plant in Burlington Vt., will be the primary manufacturing location for the new technology. IBM is already accepting designs from customers and is scheduling full production for the first half of 2011.

Result of collaboration between IBM and Austria Microsystems (AMS)

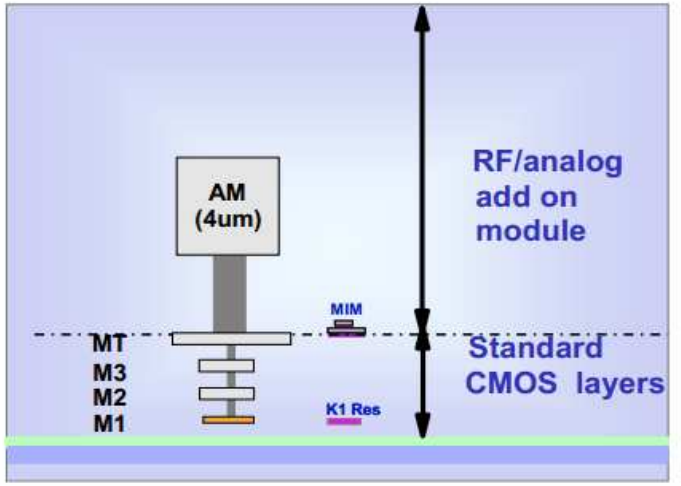
© 2009 IBM Corporation

IBM's High Voltage PDK offering: CMOS7HV

- 180nm minimum lithography
- Triple gate oxide technology supporting HV FETs
- Shallow trench isolation

- 3 to 7 levels of Al
  - Final thick wiring level for low resistance
- RF Features
  - Poly, diffusion, and well resistors, precision resistors
  - MIM Capacitors, Vertical Natural Capacitors
  - Varactors
  - HV Schottky Barrier Diode (SBD)
  - Inductors
- Electrically programmable fuse
- Wire bond or solder bump terminals

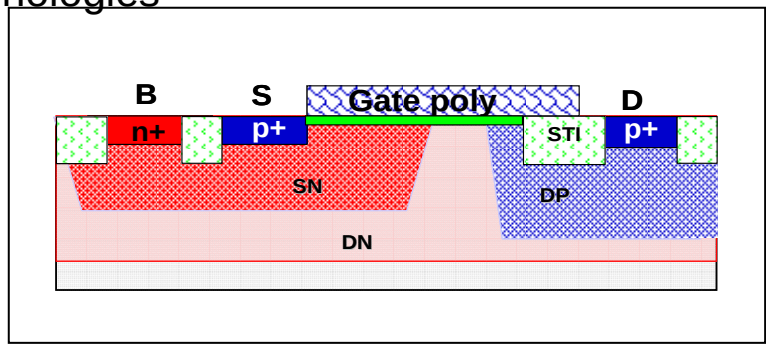
	AM Last Metal Option				
# Levels	3	4	5	6	7
					MT
				MT	M5
Standard Al wiring Levels			MT	M4	M4
		MT	M3	M3	M3
	MT	M2	M2	M2	M2
	M1	M1	M1	M1	M1

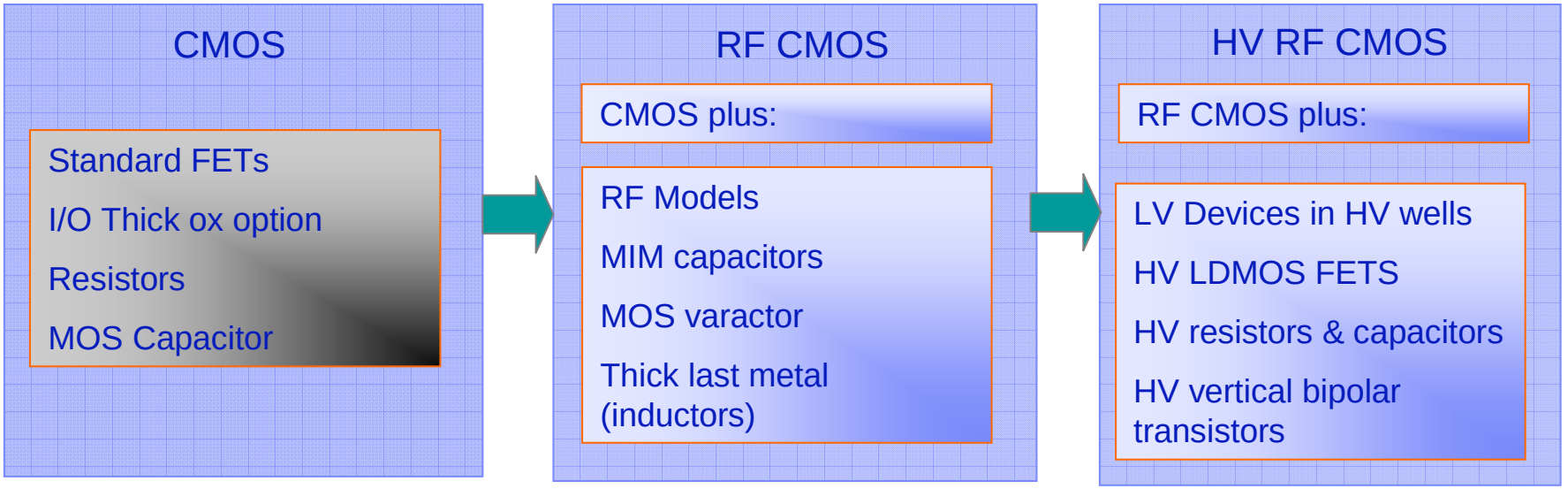


© 2009 IBM Corporation

Technology Development Approach

- Approach
  - Build from previously qualified Logic CMOS base
  - Port common elements across multiple generation technologies
  - Add new features for RF Circuit Capability
- Advantages:
  - Faster learning
  - Common process recipes for improved process control
  - Enables reuse of existing design IP





© 2009 IBM Corporation

CMOS 7HV Devices

Base 7RF Devices

Thin oxide NFET/PFET 1.8V
Medium oxide NFET/PFET for 5V use
High Vt NFET/PFET
Super High Vt NFET/PFET*
N+ diffusion resistor
P+ diffusion resistor
N+ poly resistor
P+ poly resistor
K1 BEOL resistor
RR High resistivity poly resistor
RP precision poly resistor
Single Nitride MIM
Dual Nitride MIM
MOS Varactor
PCDCAP for 1.8V use
PCAP for 1.8 and 5V use
Vertical parallel plate capacitor (VNcap)
P- Schottky Barrier Diode
Efuse
Bondpad
Inductors and T-lines

Modifications to 7RF devices for HV process

Thin ox NFET/PFET 1.8V in HV wells
High Vt NFET/PFET in HV wells
Super High Vt NFET/PFET*
Medium oxide NFET/PFET for 5V use in HV wells
N+ diffusion resistor in HV well
P+ diffusion resistor in HV well

High Voltage Devices

Medium oxide NFET/PFET for 12V use
Thin oxide NFETi/PFET for 20V use
Medium oxide NFET for 20V use
Thick oxide NFETi/PFET for 20V use
Thick oxide NFETi/PFET symmetric for 20V use
Medium oxide NFETi/PFET for 25V use
Thin oxide NFETi/PFET for 50V use
Medium oxide NFETi/PFET for 50V use
Thick NFETi/PFET for 50V use
Thick NFETi/PFET symmetric for 50V use
Medium Oxide NFETi/PFET for 120V use
3 terminal JFET
Parasitic VPNP (high V)
Parasitic VNPN (isolated)
NWell resistor in HV well
PWell resistor in HV well
High Voltage VNcap (50 and **120V use**)
High Voltage Schottky Barrier Diode

© 2009 IBM Corporation

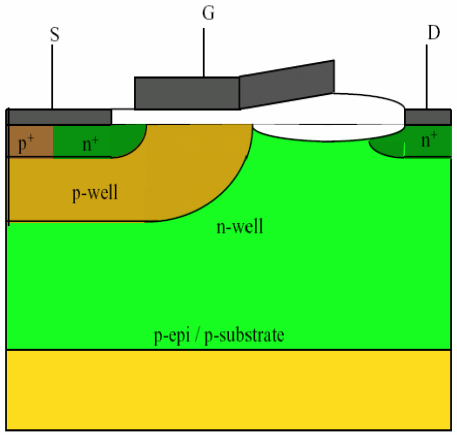
CMOS7HV device menu

Device	CMOS Base	HV Features	RF/HPA Features
FETs	1.8V Thin ox N/P FET 5.0V Medium ox N/P FET High Vt N/P FET Super High Vt N/P FET	20V/50V Thin, Med and Thick ox N/P LDMOS Thick ox N/P FET symm 12 and 120V Med ox N/P LDMOS HV JFET, HV VPNP, HV VNPN	RF Analog FET Models
Resistors	N+, P+ diffusion resistor N+, P+ Poly resistor	NWell / PWell resistor in HV well N+, P+ diffusion resistor in HV well	K1 BEOL resistor Poly res - RR High resistivity & RP Precision
Diodes	Low turn on Schottky Barrier Diode	High Voltage Schottky Barrier Diode	
Decoupling caps and Varactors	Thin/thick ncaps/varactors, pcap	Thin/thick oxide pcap in HV well	Single / Dual MIM OR Single / Dual HD MIM
BEOL Capacitors	Vertical Native Capacitor	High Voltage VNcap	
BEOL	6LM: M1 –M5, MT	Analog Metal	Analog Metal
Inductors			Analog Metal
ESD	1.8V/5V rc-clamp, esdnfet(opp), esdnfeti(opp), P/AP diodes	20V/25V/50V rc_clamp_EOS 2kV,4kV,8kV ratings, HV ESD trigger diodes, up/down diodes	Low capacitance options for RF pins
Triple well Isolation	Yes	Yes	Yes

© 2009 IBM Corporation

LDMOS FETs: What, Why

- The sub-200V domain is of great interest because of
  - Rapidly expanding applications and customer base ➔ $$$
  - Opportunities for integration and cost reduction ➔ $$$



- **In OFF state, gate turns off current flow**
- **In ON state, gate turns on current flow via channel and drift region**
- **ON resistance (R_{on}) and Breakdown Voltage (BV) are important Figures of Merit of the LDMOS: Low R_{on} and High BV are desirable**
- **However, trade-off exists between R_{on} and BV**

© 2009 IBM Corporation

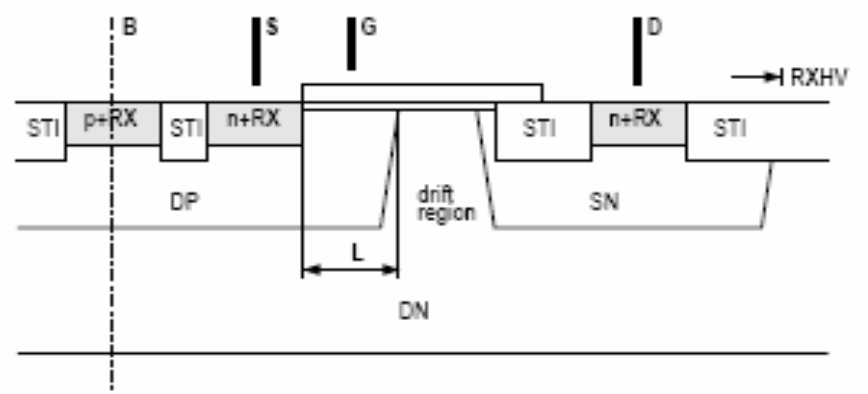
HVFET flavors

- Thin(T), Medium(M), Thick(H) or Step(MH) Oxide
  - Thin(1.8V), Medium(5V), Thick(20V)
  - To support different driving logic levels
- Symmetric or Asymmetric
  - To support unidirectional vs bidirectional operation
- Non-isolated or Isolated
  - Non-isolated
    - Used for low-side applications
    - Lower mask count and cost; lower RON
    - However, prone to substrate current injection effects
  - Isolated
    - For high side (half bridge) applications, isolated device (floating source) needed.
    - Immune from substrate current injection effects
    - Higher mask count and cost

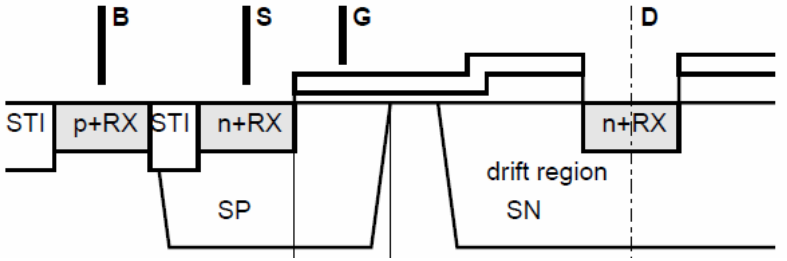
© 2009 IBM Corporation

CMOS7HV FET Flavors

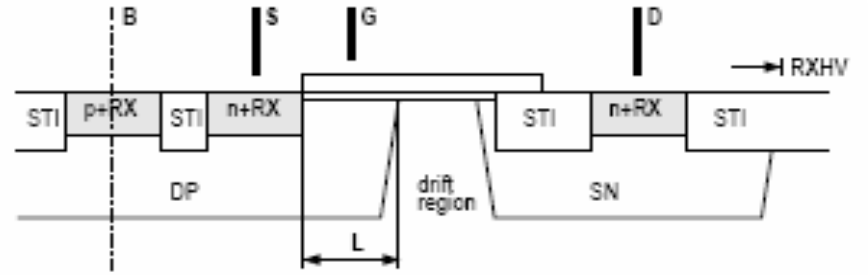
Asymmetric, Isolated, STI



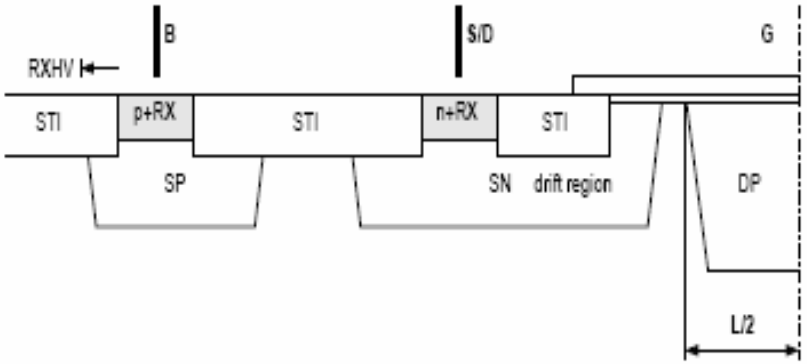
Asymmetric, Non-Isolated, Step Oxide



Asymmetric, Non-Isolated, STI



Symmetric, Non-Isolated, STI



© 2009 IBM Corporation

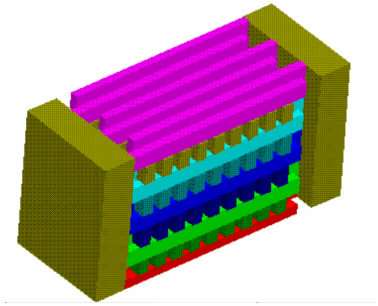
HVFET target applications

Vds	Vgs=1.8V	Vgs=5V	Vgs=20V
12V	Mobile PMU/LMUs Handheld PAs		
20/25V	Mobile LEDs & LED backlights Audio Class D	Industrial LEDs & LED backlights Building automation 24V Industrial sensors (& MEMs) Motor drivers & actuators Wireless charging	Industrial sensors (& MEMs) Motor drivers & actuators Industrial voltage regulators Medical applications
50V	Automotive Renewable energy		
	RF base stations	Building automation 48V Industrial sensors (& MEMs) Motor drivers & actuators Wireless charging	
	Wired industrial controls		
85V	RF base stations		
	Network communications LED backlights		
120V	Renewable energy Hybrid & electric vehicles Medical imaging		

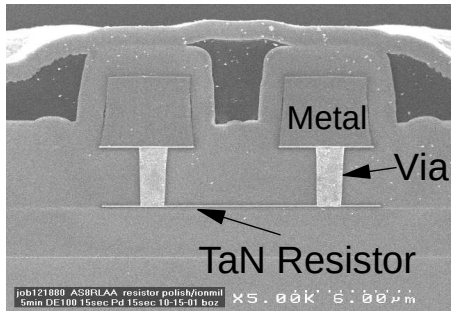
© 2009 IBM Corporation

RF features in HV technology will enable new applications

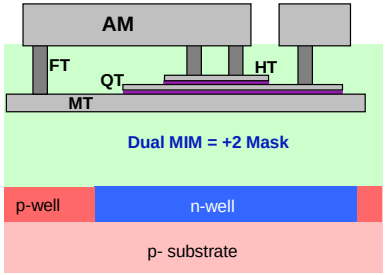
- **Resistors**
  - Wide range of sheet resistances
  - Silicon/Polysilicon/TaN resistors available
  - Low VCR and TCR alternatives
- **Capacitors**
  - MIM caps as well as vertical VNCAPs
- **Varactors**
  - Scalable gate width/Length
  - 1.8V nMOS / pMOS accumulation caps
- **Inductors**
  - Scalable pCells with supporting models
  - Center tapped / symmetric spiral designs



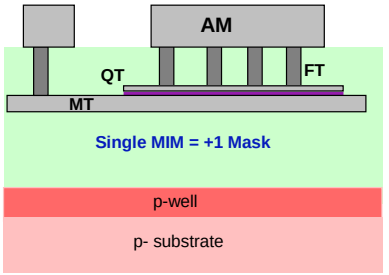
Dual



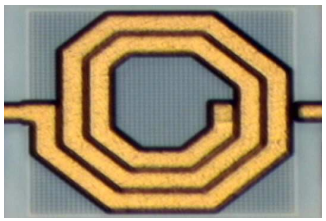
Single



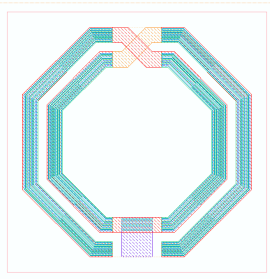
Shown with NW ground plane option



Shown with SUB ground plane option



Center tapped spiral



Center tapped spiral

© 2009 IBM Corporation

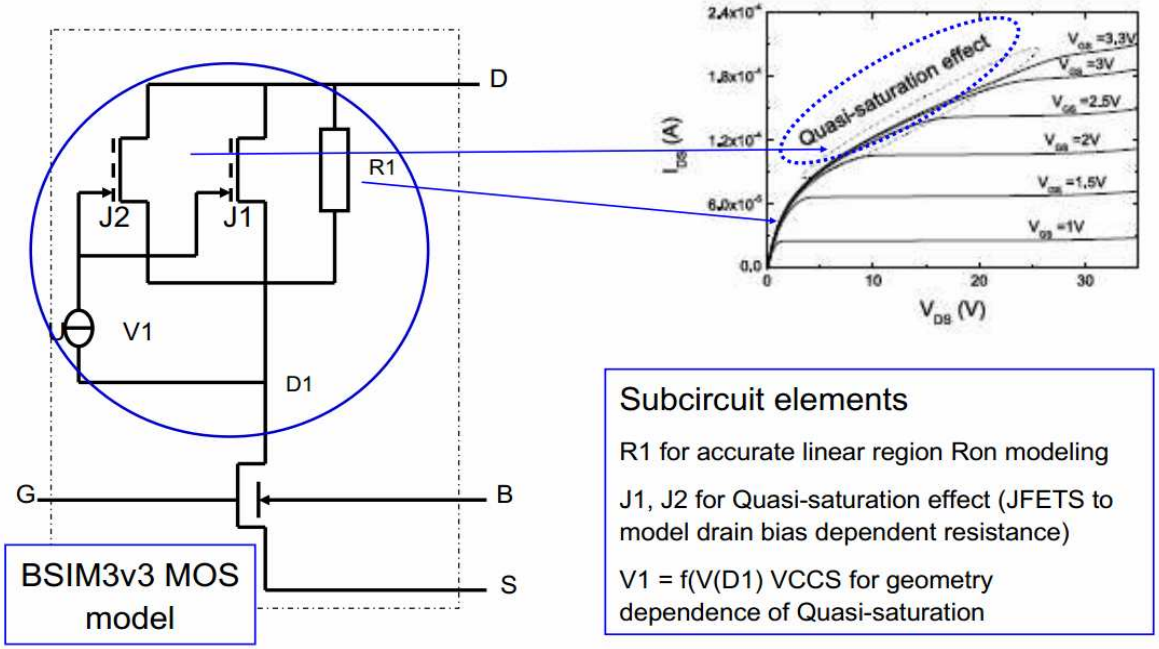
HVFET models at IBM

- BSIM + subcircuit based
  - Core model is BSIM3
  - Subcircuit wrapper in order to model high voltage phenomena
- HiSIM-HV-based
  - High voltage features built-in to the model

© 2009 IBM Corporation

BSIM-based models

- Regular models + sub-circuit extensions
  - **BSIM3** + JFET, resistor
  - Resistor and JFET for modeling drift resistance in linear and Quasi Saturation



E.Seebacher, K.Molnar, W.Posch, B.Senapati, A.Steinmair, W.Pflanzl et al

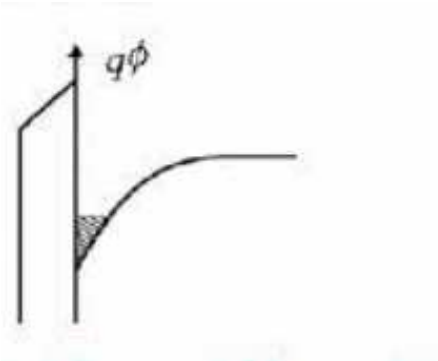
Limitations

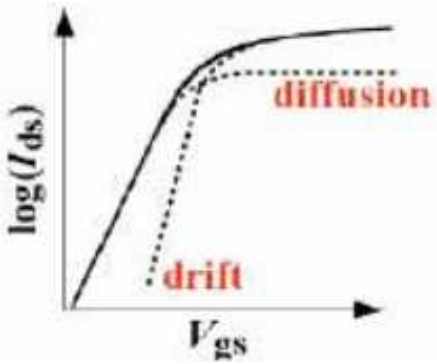
More complex sub-circuit topology
Despite sub-circuit elements, model accuracy is limited in linear and QS regions
Capacitance model accuracy is limited
No self-heating effect model
Cannot model double Impact Ionization

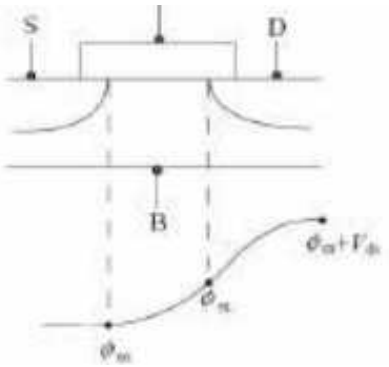
© 2009 IBM Corporation

HiSIM-HV model

- High Voltage Model "**HiSIM-HV**"
  - HiSIM_HV is the surface-potential (Φs)-based model which was selected by the Compact Model Council (CMC) as the industry standard high-voltage MOSFET model in December 2007.
  - HiSIM_HV is based on the HiSIM (Hiroshima-university STARC IGFET Model) model and features a consistent potential description across MOSFET channel and drift region
  - Complete surface potential based model (including drift region)
  - Based on drift-diffusion theory using charge sheet and GCA
  - Includes all effects observed in state-of-art MOSFETs
  - Applicable to symmetric & asymmetric LDMOS FETs







© 2009 IBM Corporation

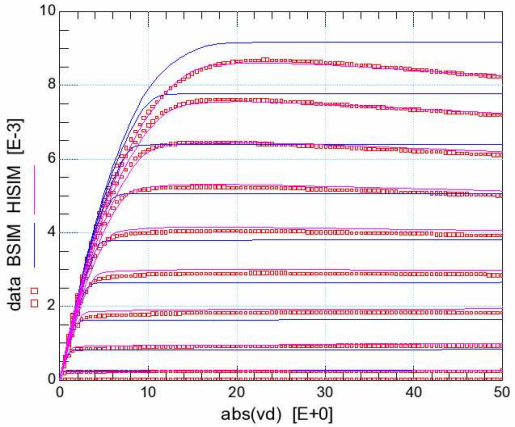
HiSIM-HV modeling options (Switches) available

Symmetric vs Asymmetric device	COSYM=1,0
Modeling of Source/Drain Resistance	CORSRD=0,1,2,3,-1
Overlap charges/capacitances	COADOV=0,1
Bias-dependent overlap capacitance at Drain side	COOVLP=0,1
Bias-dependent overlap capacitance at Source side	COOVLPS=0,1
Calculation of surface potential in overlap region	COQOVSM=0,1,2
Inclusion of Self Heating Effect	COSELFHEAT=0,1
Substrate current calculation	COISUB=0,1
Gate current calculation	COIIGS=0,1
GIDL current calculation	COGIDL=0,1
STI leakage current calculation	COISTI=0,1
NQS model	CONQS=0,1
Gate resistance calculation	CORG=0,1
Substrate resistance calculation	CORBNET=0,1
1/f noise	COFLICK=0,1
Thermal noise	COTHRML=0,1
Induced gate noise	COIGN=0,1

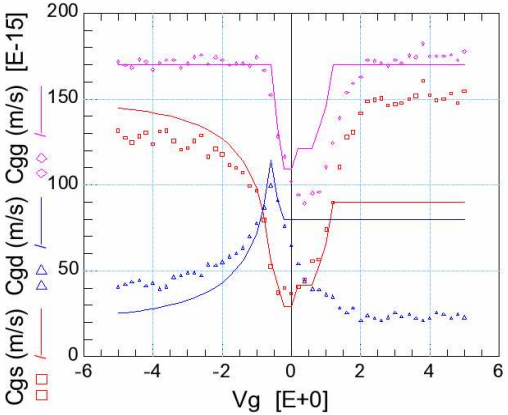
© 2009 IBM Corporation

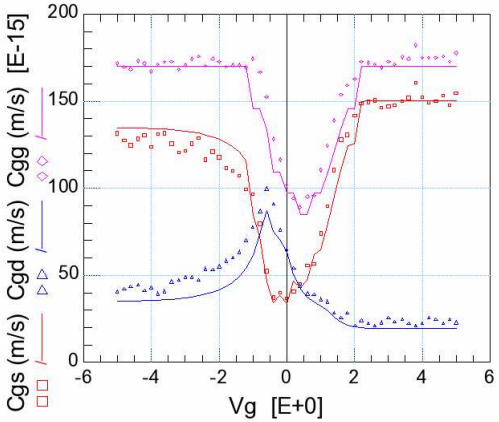
HISIM vs BSIM models comparison

I-V fits: BSIM (blue) vs HiSIM (red)



C-V fits: BSIM (left) vs HiSIM (right)



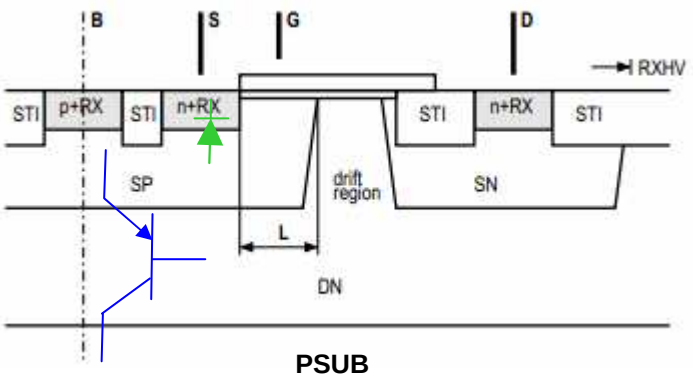


More accurate modeling of I-V and C-V using HiSIM-HV

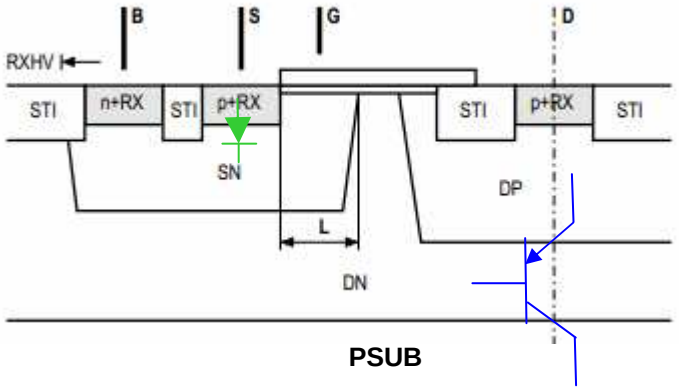
© 2009 IBM Corporation

HiSIM_HV Modeling flow and strategy

NFET



PFET



FET-mode measurements (currents, capacitances) ➔ FET model parameters

Internal diode I-V and C-V, 1/f noise

Diode-mode measurements (currents, capacitances)➔ External diode parameters

BJT-mode measurements (currents, capacitances) ➔ External BJT model parameters

Statistical model (MC, Corners, mismatch)

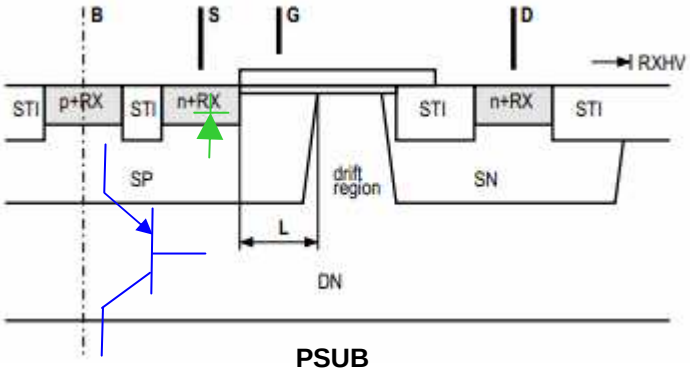
Safe Operating Area model

➔ Centered model ➔ As-fit model

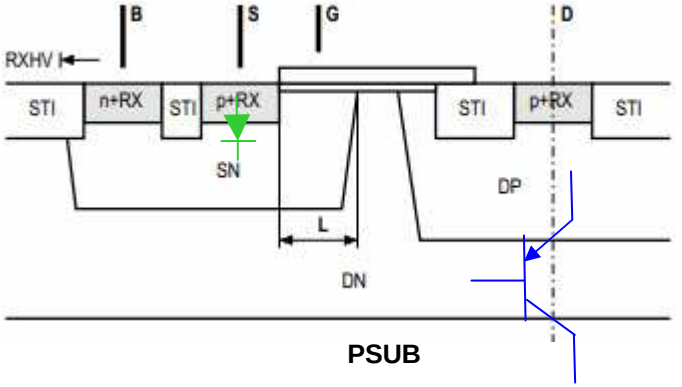
© 2009 IBM Corporation

Modeling of junctions

NFET



PFET



Junctions: RX/SP, SP/DN, DN/Psub

Junctions: RX/SN, DP/DN, DN/Psub

Each of the junctions has area and perimeter intensive layouts for extracting bottom and sidewall parameters

In addition, RX/SP and RX/SN junctions have STI-bounded layouts for extracting STI sidewall junction capacitance

External BJT model (Gummel-Poon) is used for modeling Forward & Reverse Gummel characteristics

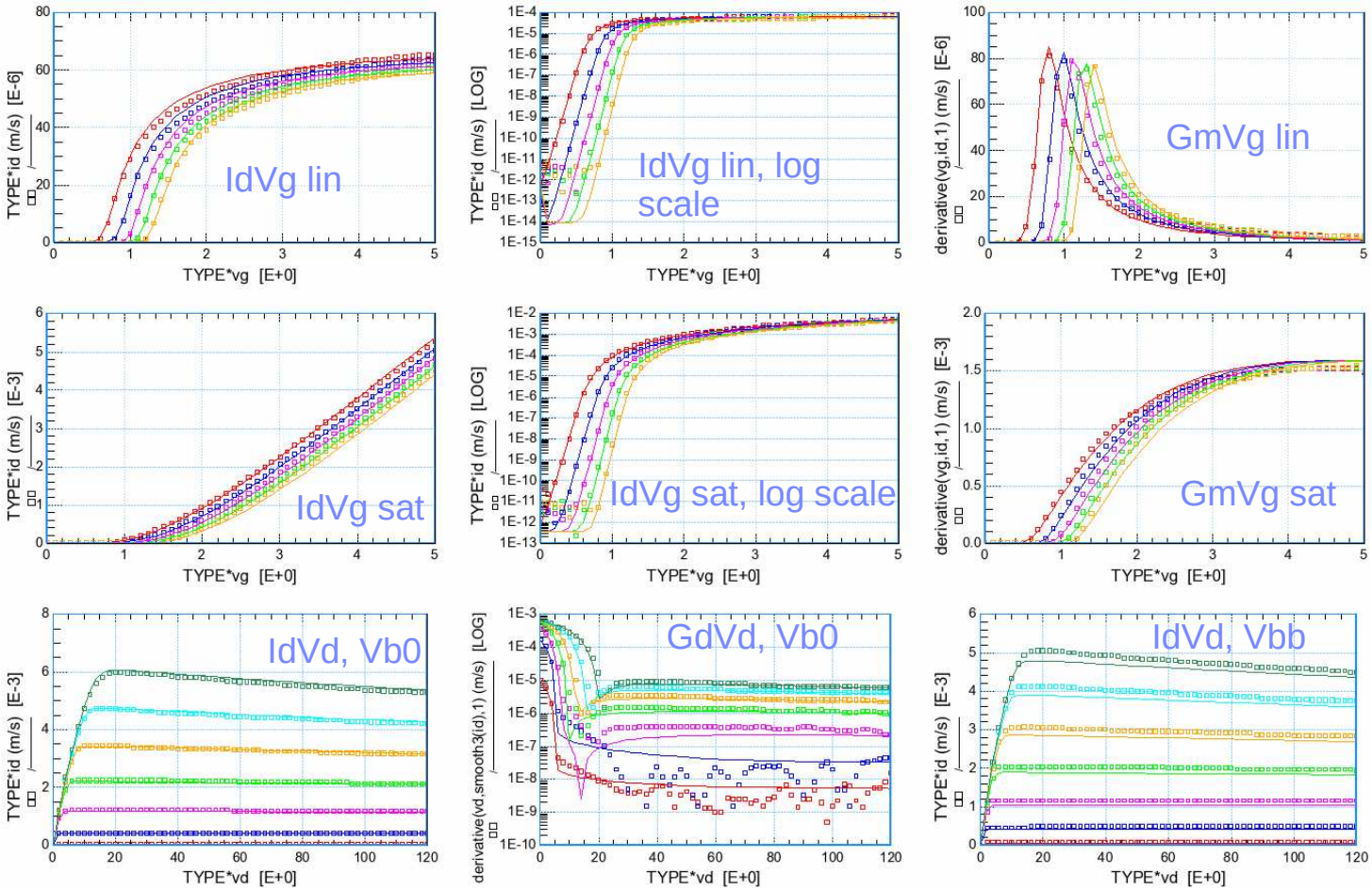
© 2009 IBM Corporation

Model features

- Existing HVFET models (20V, 25V, 50V) BSIM-based; New models (12V, 120V, 36V, 72V, 85V..) HiSIM-HV based
- All models validated across W,L and T(-40C to 180C)
- Models include
  - Process variations (Monte Carlo and corners)
  - Mismatch
  - 1/f noise (nominal & statistical)
  - Safe Operating Area (SOA)

© 2009 IBM Corporation

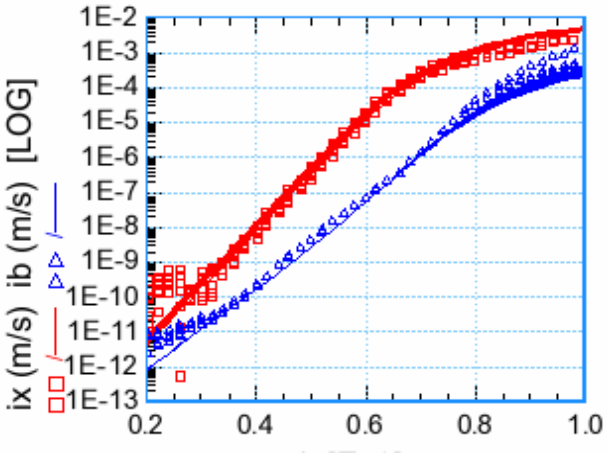
Typical DC Model-Hardware Correlation (MHC) plots



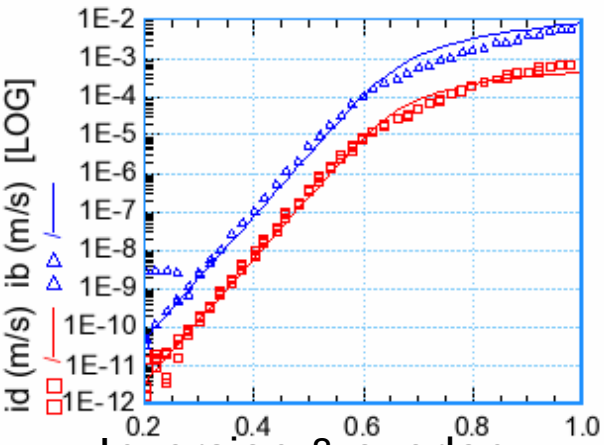
© 2009 IBM Corporation

Typical Model-Hardware Correlation (MHC) plots

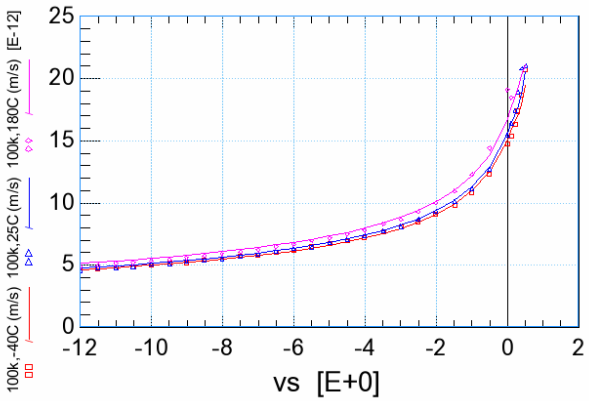
Forward Gummel



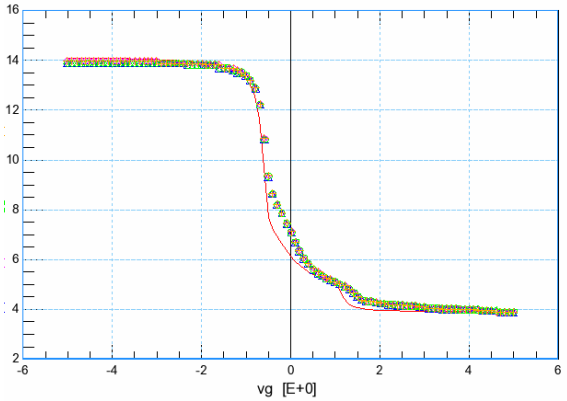
Reverse Gummel



Junction capacitance



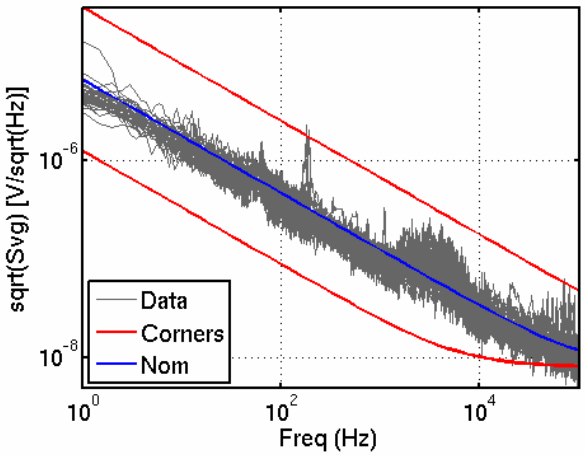
Inversion & overlap capacitance



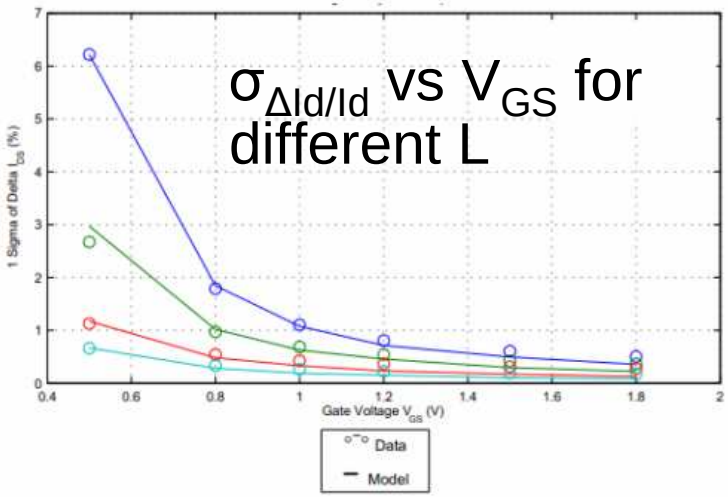
© 2009 IBM Corporation

Typical Model-Hardware Correlation (MHC) plots

1/f noise



Mismatch



© 2009 IBM Corporation

Outline

- Introduction
- IBM's HV value proposition
- IBM's HV PDK offering
  - Technology
  - Devices
  - Models
- Recent publications, highlights
- Summary

© 2009 IBM Corporation

IBM Publications on HV CMOS

ISPSD 2010

A 120V 180nm High Voltage CMOS smart power technology for System-on-chip integration

R. Minixhofer*, N. Feilchenfeld+, M. Knaipp*, G. Röhrer*, J.M. Park*, M. Zierak+, H. Enichlmair*, M. Levy+, B. Loeffler*, D. Hershberger+, F. Unterleitner*, M. Gautsch+, K. Chatty+, Y. Shi+, W. Posch*, E. Seebacher*, M. Schrems*, J. Dunn+, D. Harame+

*R&D Department
austriamicrosystems AG
Unterpremstaetten, Austria

+Analog and Mixed Signal Development
IBM Microelectronics Division
Essex Junction, Vermont

ISPSD 2011

Drift Design Impact on Quasi-Saturation & HCI for Scalable N-LDMOS

Yun Shi, Natalie Feilchenfeld, Rick Phelps, Max Levy, Martin Knaipp*, Rainer Minixhofer*

Analog and Mixed Signal Technology Development, IBM Microelectronics Division,
Essex Junction, Vermont, 05452, USA
*R&D Department, Austriamicrosystem, AG, Unterpremstaetten, Austria

ISPSD 2012 (accepted)

Design & Optimization of 120V NLDMOS in 180nm HVCMOS Technology

Yun Shi, Theodore Letavic, Santosh Sharma, John Ellis-Monaghan, Natalie Feilchenfeld, Rick Phelps, Don Cook, Christopher Lamothe, Jim Dunn

Analog and Mixed Signal Technology Development, IBM Microelectronics Division
Essex Junction, Vermont, 05452, USA
Email: yunshi@us.ibm.com
Phone: 1-802-769-5867 Fax: 1-802-769-9452

Planar dual-gate oxide LDMOS structures in 180nm power management technology

Santosh Sharma[1], Theodore Letavic[1], Yun Shi[1], John-Ellis Monaghan[1], Natalie Feilchenfeld[1], Rick Phelps[1], Christopher Lamothe[1], Don Cook[1], Jim Dunn[1], Georg Roerher[2], Helmut Nauschnig[2], Rainer Minixhofer[2]

[1] *Analog and Mixed Signal Development, IBM Microelectronics, Essex Junction, VT*
[2] *austriamicrosystems AG, A-8141, Unterpremstätten, Austria*
Email: *sharmasa@us.ibm.com*
Phone: *802 769 2211*

A 90 to 170V scalable P-LDMOS with accompanied high voltage PJFET

John Ellis-Monaghan, Yun Shi, Santosh Sharma, Natalie Feilchenfeld, Ted Letavic, Rick Phelps, Crystal Hedges, Don Cook, Jim Dunn

IBM Microelectronics Division, Essex Junction, Vermont
Email: jjem@us.ibm.com
Phone: (802) 769-8627 Fax: (802) 769-9452

Hot-Carrier Behaviour and Ron-BV Trade-off Optimization for p-channel LDMOS Transistors in a 180 nm HV-CMOS Technology

Jong Mun Park[1], Martin Knaipp[1], Hubert Enichlmair[1], Yun Shi[2], Rainer Minixhofer[1], and Natalie Feilchenfeld[2]

[1]*R&D Department austriamicrosystems AG Tobelbader Strasse 30 Unterpremstaetten, Austria*

[2]*Analog and Mixed Signal Development IBM Microelectronics Division Essex Junction Vermont, USA*

Influence of Drift region on the 1/f noise in LDMOS

A. A. Dikshit[1], V. Subramanian[1], S. J. Pandharpure[1], S. S. Sirohi[1] and T. J. Letavic[2]

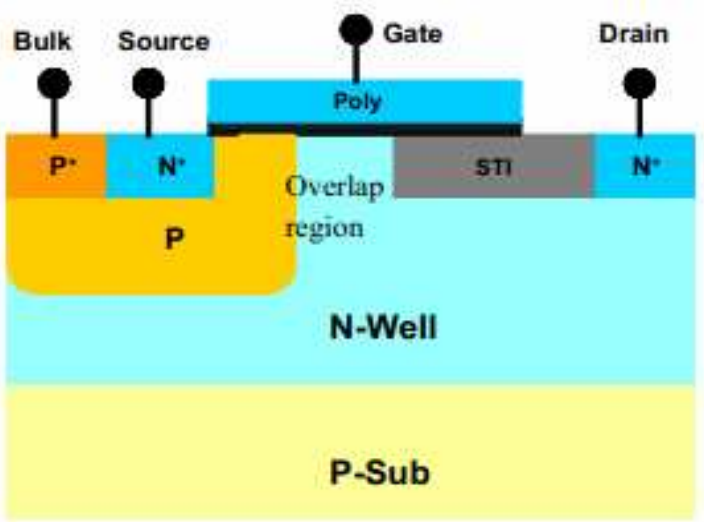
[1]*Semiconductor R & D Center, IBM India Pvt Ltd, Bangalore, India,* [2]*Analog Mixed Signal Technology Development, IBM, Hopwell Junction, NY, USA*
Email: *amdikshi@in.ibm.com*
Phone: *91-80-28061320*

© 2009 IBM Corporation

Influence of Drift region on the 1/f noise in LDMOS

A. A. Dikshit[1], V. Subramanian[1], S. J. Pandharpure[1], S. S. Sirohi[1] and T. J. Letavic[2]
[1]*Semiconductor R & D Center, IBM India Pvt Ltd, Bangalore, India,* [2]*Analog Mixed Signal Technology Development, IBM, Hopwell Junction, NY, USA*
Email: *amdikshi@in.ibm.com*
Phone: *91-80-28061320*

- **RON has channel and drift region component**
- **1/f noise also has channel and drift component**
- **This paper explores**
  - Contribution of channel vs drift components of 1/f noise
  - Extent of correlation between RON and noise
  - Vd dependence of noise to study noise in saturated vs quasi-saturated LDMOS FETs



© 2009 IBM Corporation

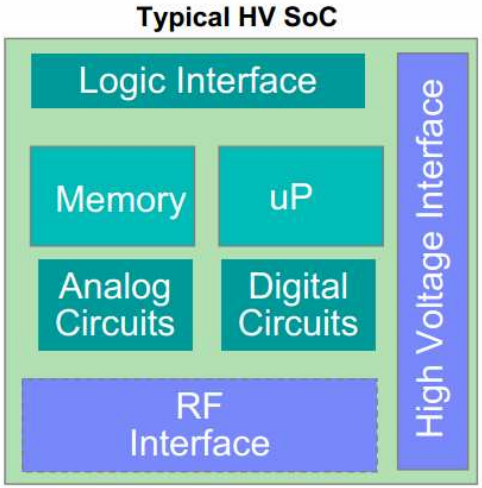
CMOS7HV Summary

- PDK Offering catering to a large spectrum of target applications
- Large base of IPs that have been co-developed and validated on silicon hardware
- Overall platform comprising digital (logic & memory), analog, RF and HV devices/IPs all integrated into a single design/simulation/validation flow

© 2009 IBM Corporation

CMOS7HV Summary

- **Enables** cost-efficient integration of power-management technology
- **High voltage** design flexibility
  - A wide range of rated-voltage/BVds devices via 2D layout; derivative products without additional mask steps
  - 20V Gate Oxide, and 85V and 120V devices
- Integrated Wireless capabilities
  - Capacitors, Varactors, Precision Resistors, Inductors
- **Offers** risk-mitigation and time-to-market advantages
  - Industry-leading analog design enablement
    - Best of Breed correlation / accuracy in the industry
    - Rebust library and device support
  - Leadership ESD enablement with reference circuits
  - Analog performance exceeding BCD technologies
    - Proven high-voltage CMOS technology
- **Enables** IP re-use
  - Compatibility with existing CMOS infrastructure ⇨ existing CMOS IP can be re-used on integrated designs
- Lower complexity when compared with bipolar CMOS/DMOS (BCD) technology



Thank you for the attention

© 2009 IBM Corporation

Acknowledgements

- IBM US
  - Ted Letavic
  - Natalie Feilchenfeld
  - Dan Maynard
  - Kim Newton
  - Jui-chu Lee
  - Ted Anderson
  - Stephen St Onge
- IBM India
  - Amit Dikshit
  - Shrinivas Pandharpure
  - Vipin Madangarli
  - Anirban Bandyopadhyay

© 2009 IBM Corporation

© 2009 IBM Corporation

© Copyright International Business Machines Corporation 2011.

IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

Produced in the United States of America July 2011
All Rights Reserved.

IBM, the IBM logo, and ibm.com
are trademarks of International Business Machines Corporation in the United States, other countries or both. A current list of IBM trademarks is available on the Web at “Copyright and trademark information” at ibm.com/legal/copytrade.shtml.

Other company, product and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in applications such as implantation, life support, or other hazardous uses where malfunction could result in death, bodily injury, or catastrophic property damage. The information contained in this document does not affect or change IBM product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.

While the information contained herein is believed to be accurate, some of it is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will IBM be liable for damages arising directly or indirectly from any use of the information contained in this document.

The IBM home page can be found at **ibm.com**
The IBM Microelectronics home page can be found at **ibm.com**/technology

© 2009 IBM Corporation