SMALL SIGNAL MODELING AND PARAMETER EXTRACTION TECHNIQUE FOR OVERLAP AND UNDERLAP DOUBLE GATE MOSFET FOR RF CIRCUIT DESIGN

Saptak Niyogi, Kalyan Koley, Chandan Kumar Sarkar and Soumya Pandit[1]

Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata-700032, India

[1]IC Design Laboratory, Institute of Radio Physics and Electronics, University of Calcutta, Kolkata-700009, India

1. Introduction

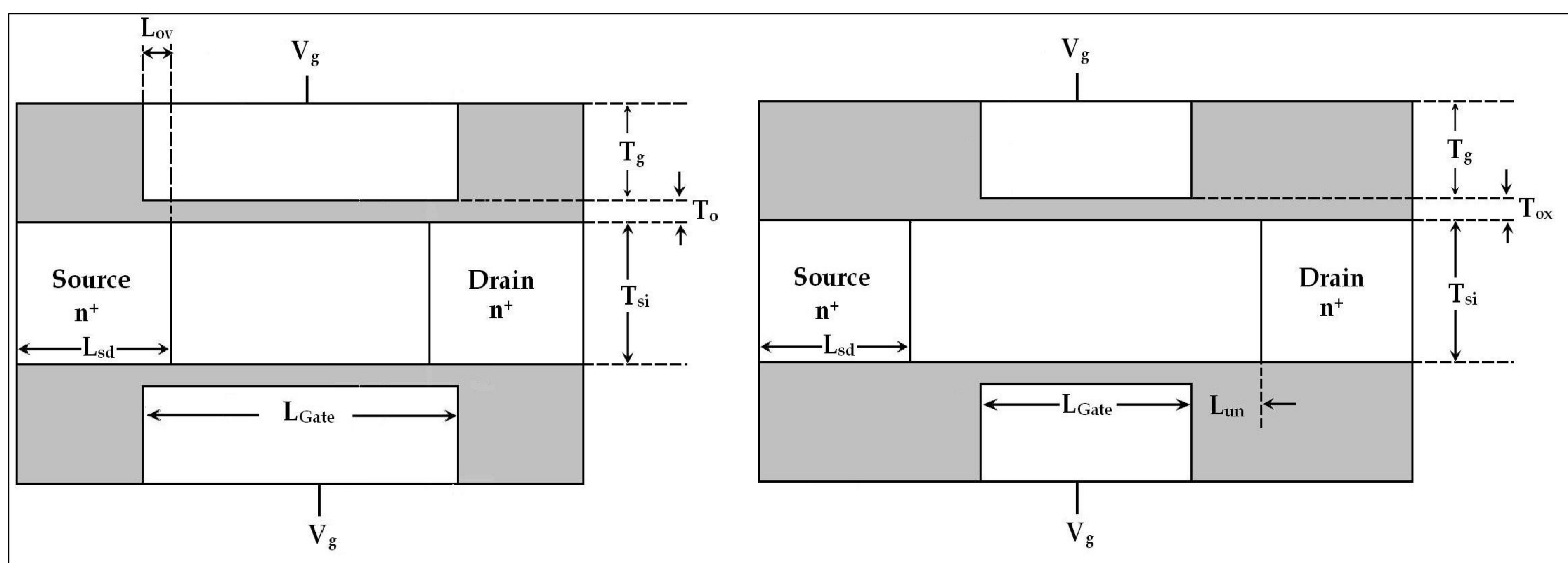
Our work deals with the design of Low Noise Amplifier (LNA) using small-small models of DGFET. The gain and Noise Figure are compared for the circuit. The LNA is designed at tuning frequency of 10 GHz.

2. DGFET

Two types of structures used:

i. Overlap DGFET
ii. Underlap DGFET

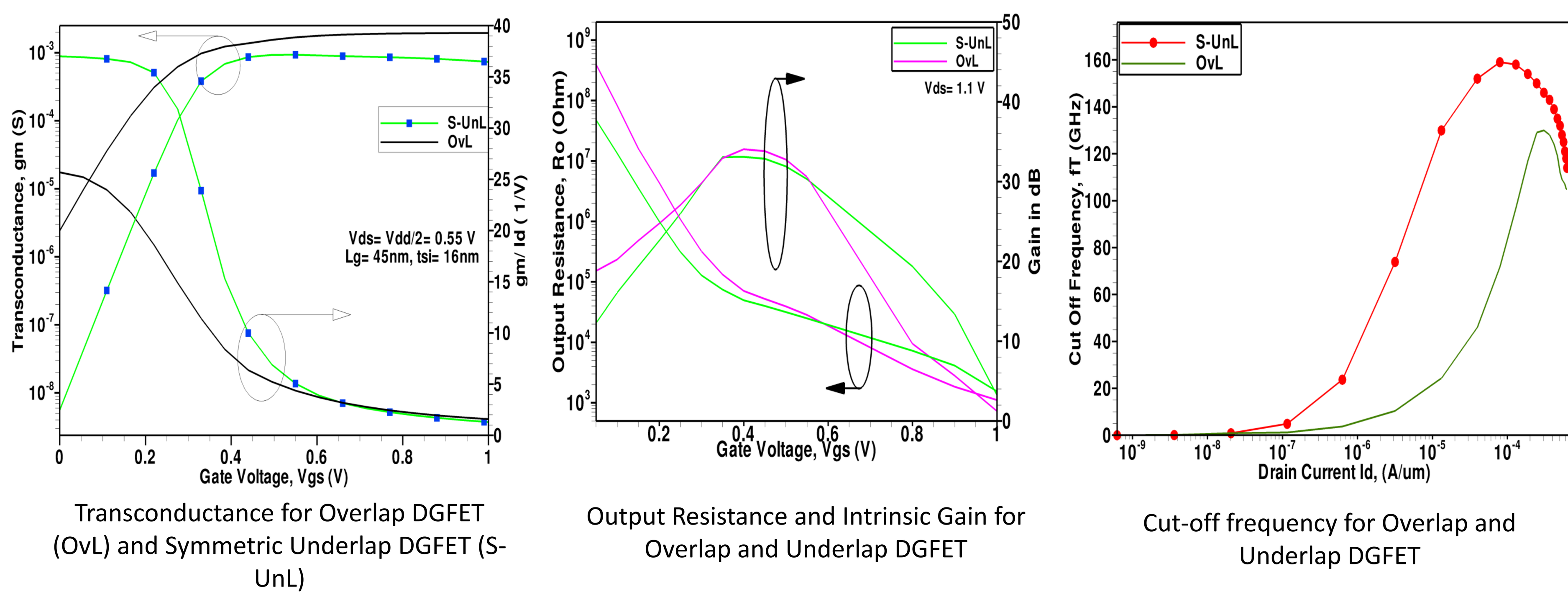
Gaussian doping profile is considered with constant Lateral Straggle of 3 nm.



Overlap DGFET and Underlap DGFET

Dimension

Gate Length (L_{gate}) = 45nm
Channel Thickness (T_{si}) = 16nm
Gate Height (T_g) = 10nm
Oxide Thickness (T_{ox}) = 1.9nm
Overlap Region (L_{ov}) = 3nm
Underlap Region (L_{un}) = 20nm



Transconductance for Overlap DGFET (OvL) and Symmetric Underlap DGFET (S-UnL)

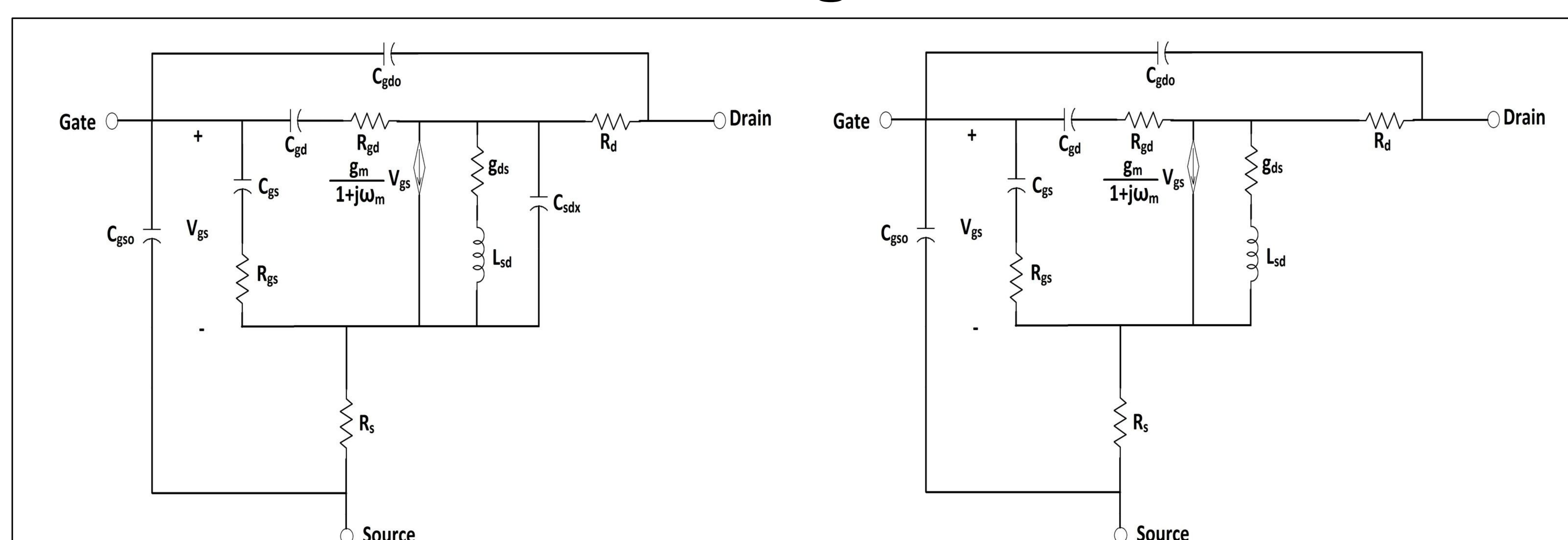
Output Resistance and Intrinsic Gain for Overlap and Underlap DGFET

Cut-off frequency for Overlap and Underlap DGFET

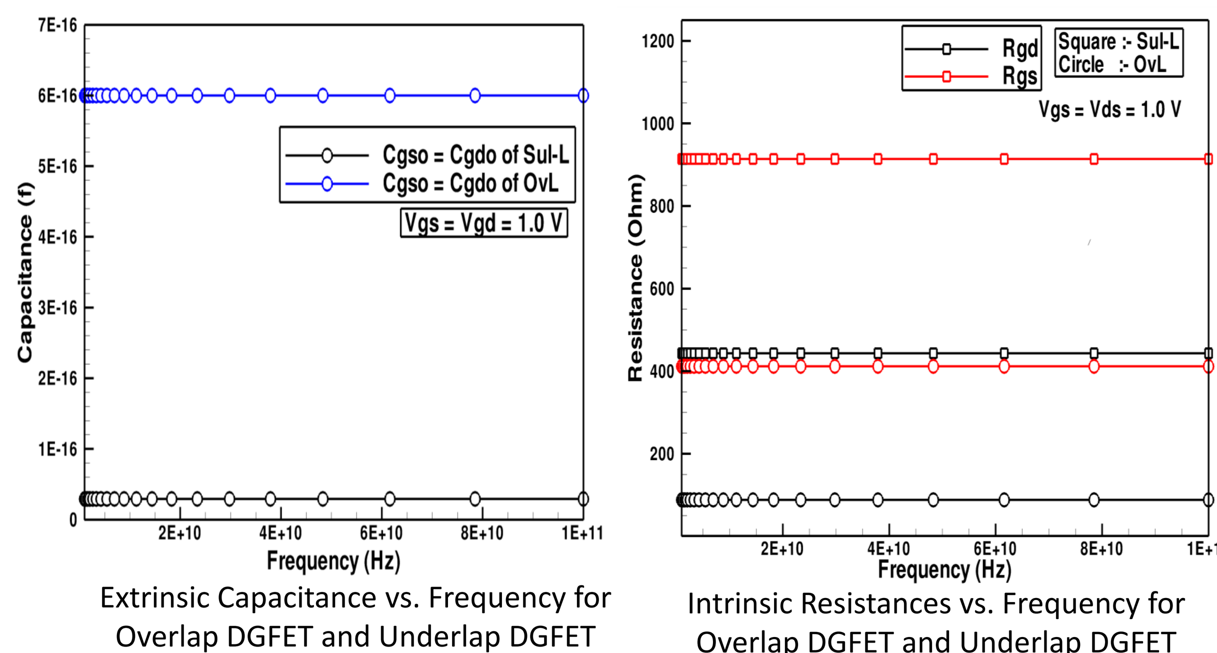
Observation

- Transconductance (gm) for Overlap DGFET is higher due to smaller effective channel length
- For the same reason output resistance (r_o) is smaller in Overlap DGFET
- Overall intrinsic gain is higher for Underlap DGFET
- Cut-Off frequency (f_t) is higher in Underlap DGFET due to lower gate capacitances

3. AC Small-Signal Model



Small-Signal Models of Overlap DGFET and Underlap DGFET



Extrinsic Capacitance vs. Frequency for Overlap DGFET and Underlap DGFET

Intrinsic Resistances vs. Frequency for Overlap DGFET and Underlap DGFET

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12}^{int})}{\omega} \qquad R_{gd} = -\frac{\mathrm{Re}(Y_{12}^{int})}{\omega^2 C_{gd}^2}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}^{int}) + \mathrm{Im}(Y_{12}^{int})}{\omega} \qquad g_m = \mathrm{Re}(Y_{21}^{int})\Big|_{\omega^2=0}$$

$$R_{gs} = \frac{1}{C_{gs}^2}\left[\frac{\mathrm{Re}(Y_{11}^{int})}{\omega^2} - R_{gd}C_{gd}^2\right]$$

$$\tau_m = -\frac{1}{g_m}\left[\frac{\mathrm{Im}(Y_{21}^{int})}{\omega} + C_{gd}\right] \qquad g_{ds} = \mathrm{Re}(Y_{22}^{int})\Big|_{\omega^2=0}$$

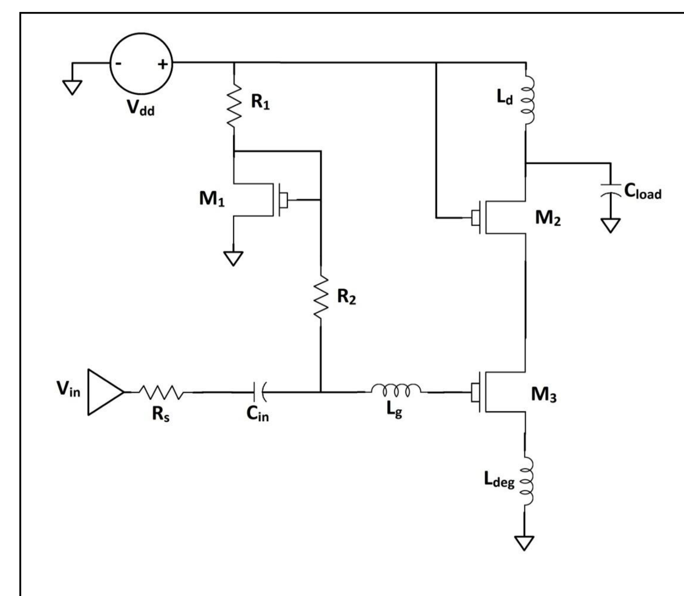
$$C_{sdx} = \frac{\mathrm{Im}(Y_{22}^{int})}{\omega} - C_{gd} + g_{ds}\tau_m$$

Model Parameter extraction equations

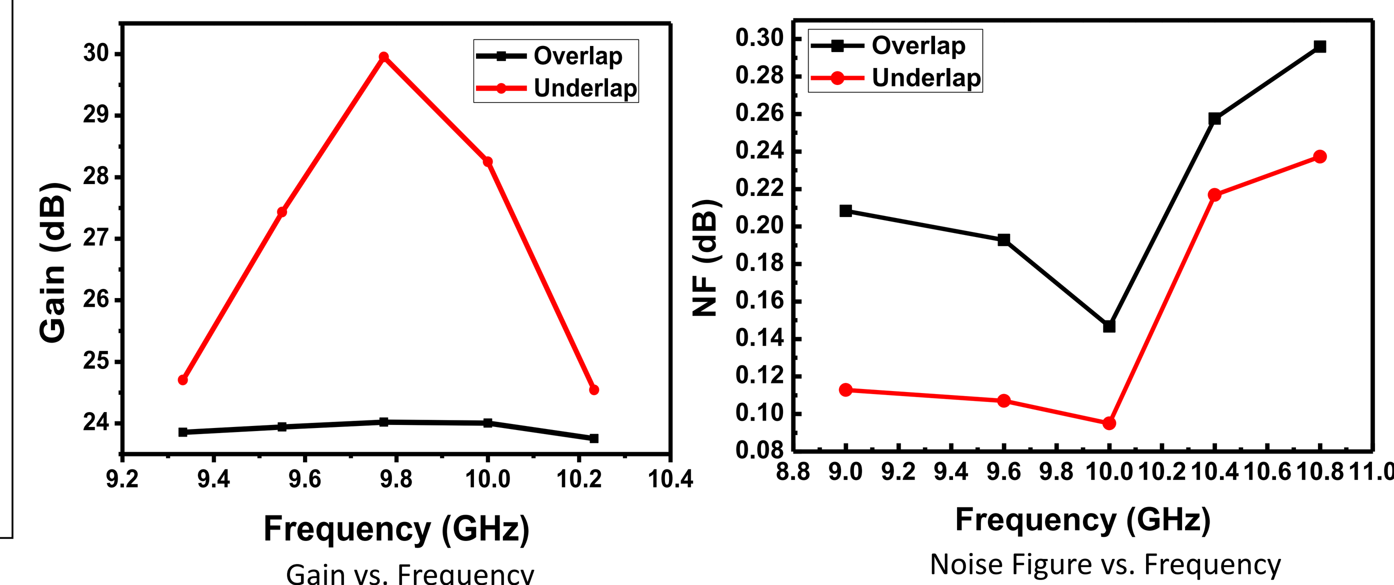
Observation

- The parameter C_{sdx} is absent in Underlap DGFET due to lower DIBL effect
- The extrinsic capacitances is lower in Underlap DGFET due to non-existence of overlap region
- Due to longer effective channel the intrinsic resistances is larger in Underlap DGFET

4. Low Noise Amplifier (LNA)



Low Noise Amplifier (LNA)



Gain vs. Frequency

Noise Figure vs. Frequency

Observation

- LNA using Underlap DGFET gives higher gain by 5 dB due to higher intrinsic gain
- It also gives lower NF by 0.04 dB due to higher f_t

5. Conclusion

- **LNA using Underlap DGFET gives better performance in respect of gain and NF**
- **Lateral Straggle would increase the gain but will also increase the DIBL effect, so we need to find the optimal Lateral Straggle**

Acknowledgement

The second, third and fourth author would like to thank DST, Govt. of India under INSPIRE, SERC scheme and Fast Track Scheme for Young Scientist

References

1. **In Man Kang, "Non-Quasi-Static RF Model for SOI FinFET and Its Verification", Journal of Semiconductor Technology and Science, Vol. 10, No. 2, June, 2010**
2. **International Technology Roadmaps for Semiconductor (ITRS), 2008 edition**
3. **Karan Bhatia, et. al., "Double-Gate FET Technology for RF Applications: Device Characteristics and Low Noise Amplifier Design", IEEE International SOI Conference Proceedings, pp. 75-76, 2006**