LOOK-UP TABLE BASED AUTOMATED FinFET CIRCUIT DESIGN

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1. Introduction :

- ✓ FinFET: Promising multi-gate structure
- ✓ Mathematical models for FinFET device are under investigation and study
- ✓ Look-up Table (LUT) approach does not require physical description of device
- ✓ Process, voltage, and supply (PVT) variations can be considered in automatic circuit design

2. $I_D - V_G$ Template based LUT Approach:

- ✓ Difficult to model moderate inversion region
- ✓ $I_D - V_G$ at $V_{DS} = V_{DS,max}$ is taken as a template
- ✓ $I_D - V_G$ at other V_{DS} is normalized with template
- ✓ Normalized data is easily fitted with cubic splines
- ✓ $I_D - V_G$ template based approach accurately models moderate inversion region and does not require non-uniform grid points

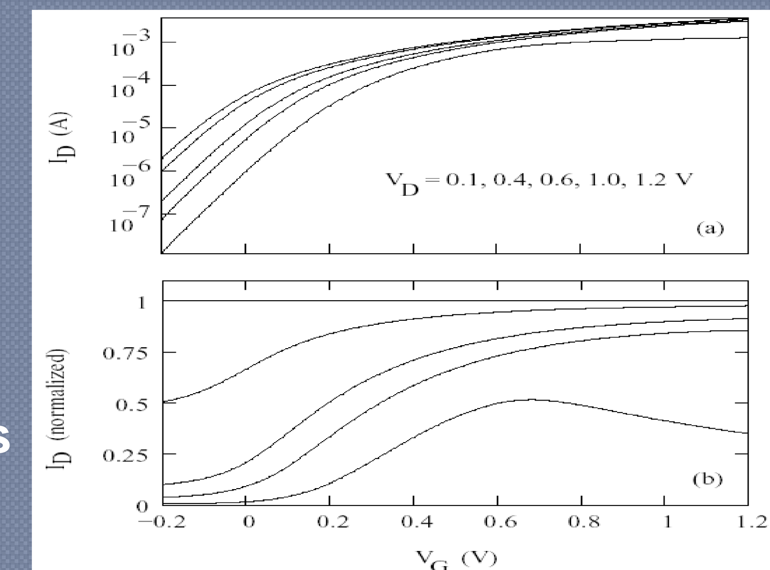

Fig. 1: (a) $I_D - V_G$ on a log scale, (b) Normalized $I_D - V_G$.

3. Automatic Circuit Design Platform:

- ✓ $I_D - V_G$ template based LUT approach is implemented in SEQUEL circuit simulator
- ✓ Particle Swarm Optimization (PSO) algorithm is used for circuit optimization
- ✓ Optimizer is integrated with SEQUEL circuit simulator for automatic circuit design for given specification
- ✓ PSO algorithm mimics behavior of birds flocking in search of food and reported to be efficient in solving multimodal optimization problem

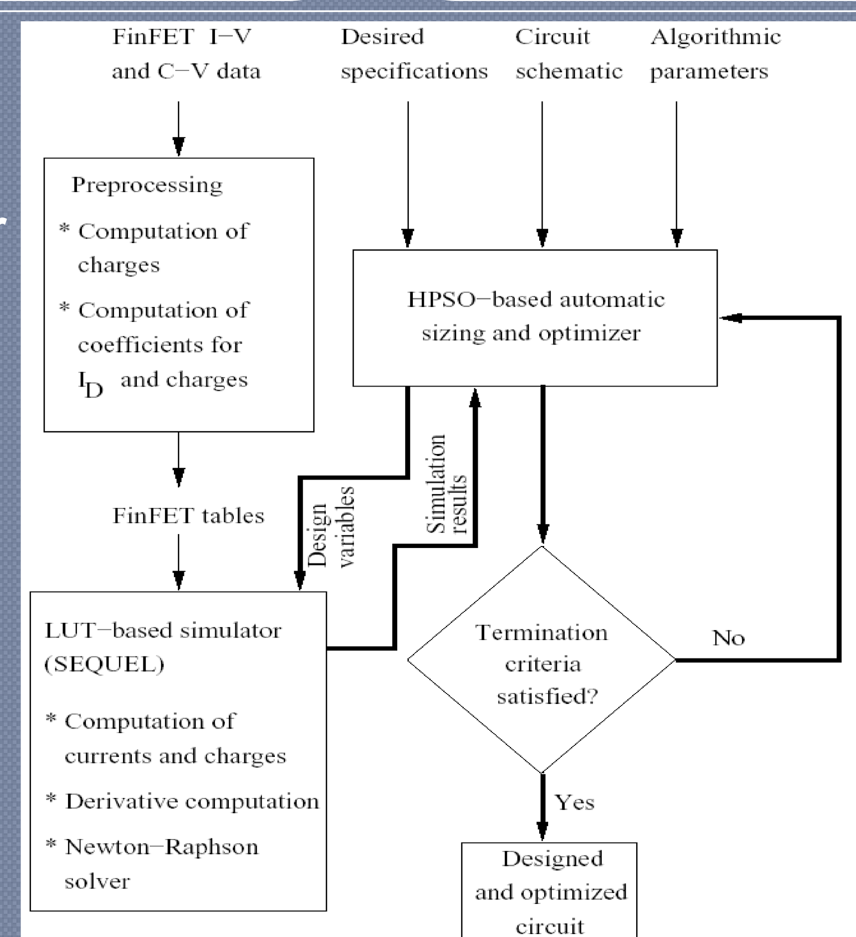

Fig. 2: FinFET circuit optimizer.

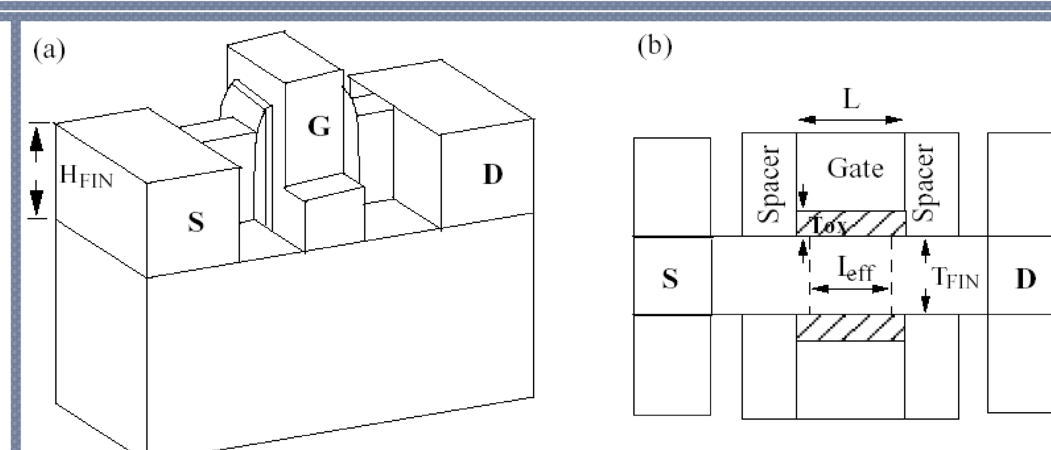

Fig. 3: FinFET device structure simulated using Sentaurus TCAD simulator to generate LUT. Minimum channel length (L) = 20 nm, effective oxide thickness = 0.9 nm, fin thickness (TFIN) = 6 nm, fin height (HFIN) = 30 nm.

- ✓ LUTs generated at T = 27, 70℃
- ✓ Variations in L, TFIN, and EOT considered equal to ± 2 nm, ± 1 nm, and ± 0.1 nm to generate LUTs at process corners
- ✓ V_{DD} variation is taken ± 10 % of 1 V

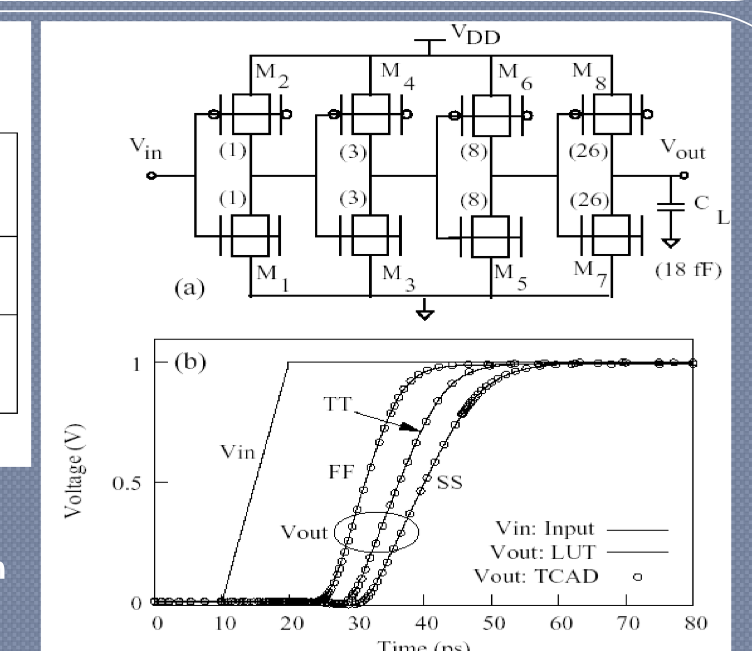

Fig. 4: (a) Buffer chain circuit designed using optimizer (Fig. 3) to minimize rise and fall propagation delay times, (b) Validation of response at different process corners using TCAD simulator. Numbers in bracket in figure (a) shown number of fins which are design parameters.

4. Design of op-amp based FinFET Circuits:

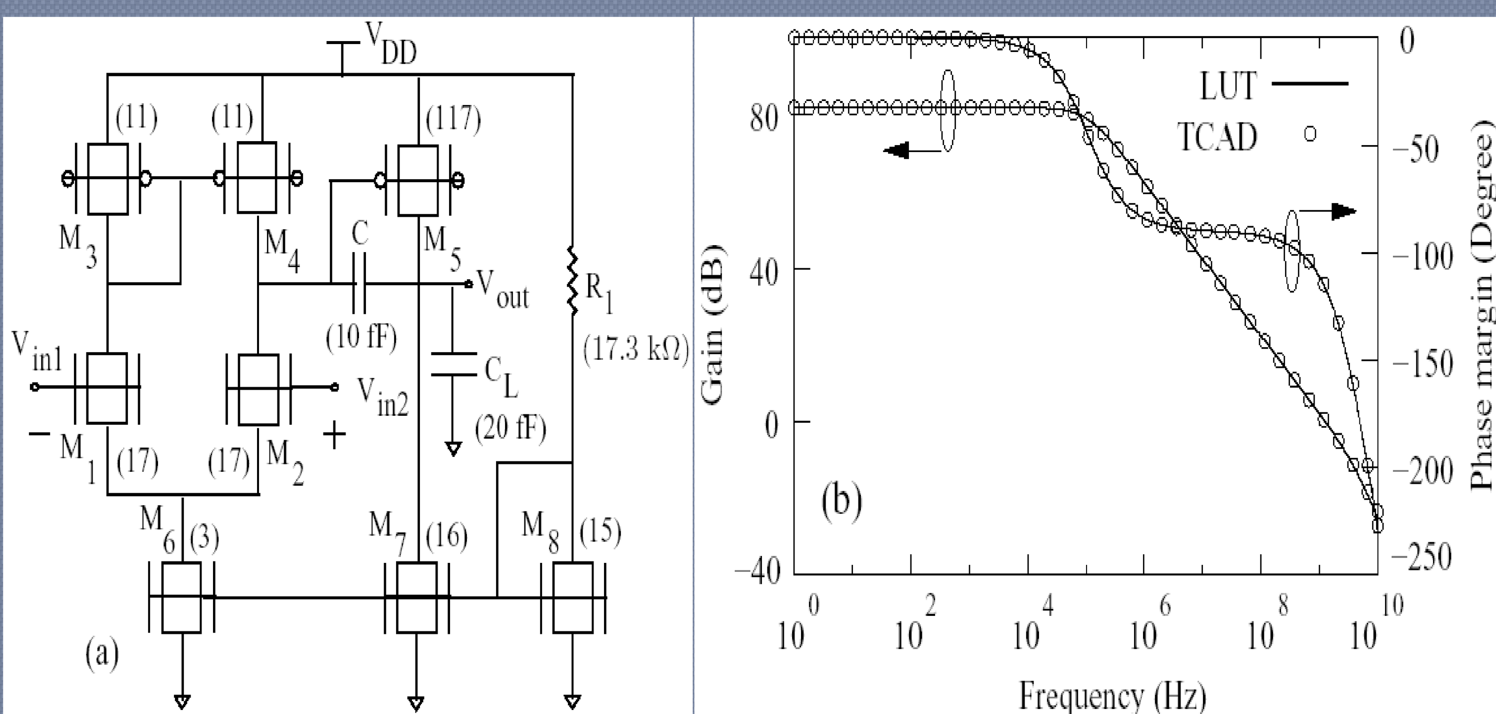

Fig. 5: (a) Two-stage wide-band op-amp designed using optimizer. (b) Frequency response of designed circuit validated using TCAD simulation for typical device at V_{DD} = 1V. C_L = 20 fF, channel length (L) = 50 nm for M_1 to M_5 and 250 nm for M_6 to M_8.

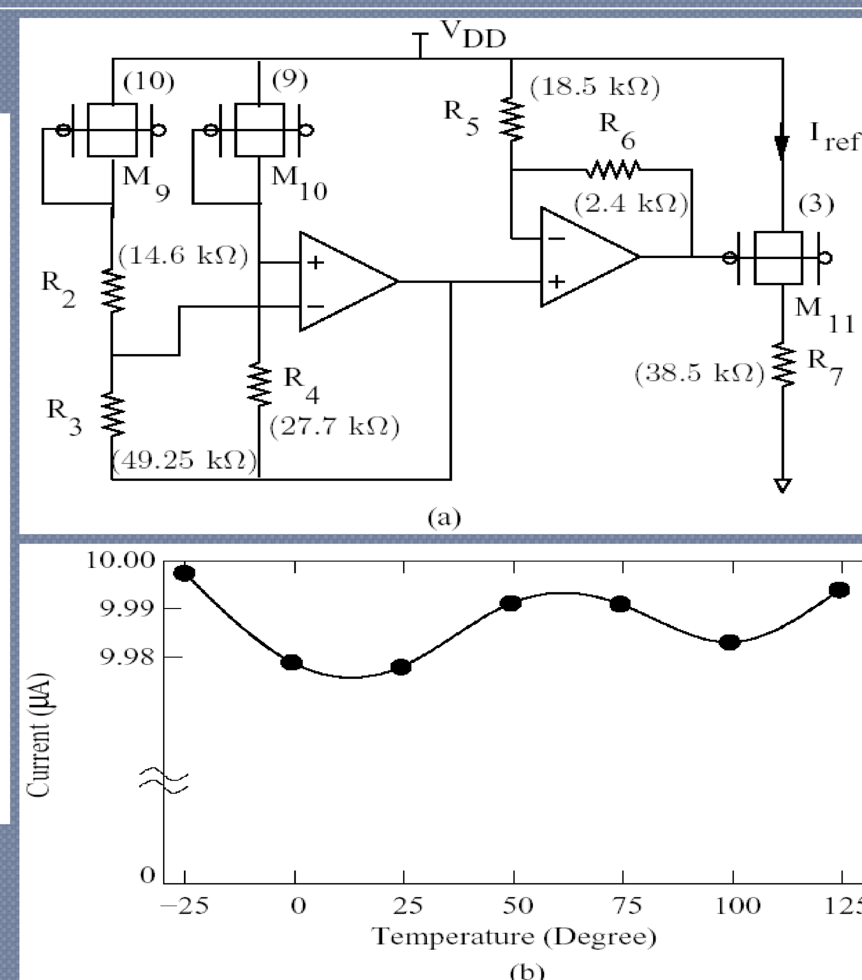

Fig. 6: (a) Current reference circuit designed for a current equal to 10 μA ± 1 % over a T = -25 to 125℃. (b) I_{ref} v/s Temp of designed circuit.

Table 1: Desired and obtained specifications of the circuit shown in Fig. 5.

Desired Specifications	V_{DD}= 1.1 V TT	FF	SS	V_{DD}= 0.9 V TT	FF	SS
Gain (≥ 80 dB)	82	79.6	84.7	81.3	78.8	83.3
PM (≥ 60°)	62	64	59.4	65.4	67.65	62.5
UGF (≥ 1 GHz)	1.53	1.58	1.55	1.0	1.05	1.02
PD (≤ 100 μW)	85	105	72	50	61	42
SR (≥ 100 V/μS)	529	562	523	372	394	368
SF (≥ 100 V/μS)	469	494	465	207	225	198

Table 2: CPU time taken for the design of various FinFET circuits by the optimizer.

Design Example	Design variables	CPU time
Buffer chain	3	00 h 34 m
Two-stage op-amp	7	02 h 29 m
Three-stage op-amp	9	04 h 30 m
Sense amplifier	5	05 h 24 m
Current reference	16	20 h 30 m

5. Impact of Process Variations Study:

- ✓ A LUT represents a device with a particular geometry
- ✓ Process variations study requires large number of LUTs
- ✓ LUT interpolation scheme is used to generate sufficiently large number of LUTs (41) from a small number of LUTs (5) for the process parameters: L, TFIN, and EOT.
- ✓ LUTs for L, TFIN, and EOT are generated using TCAD simulator at following values:
- ➢ L = 17, 19, 20, 21, and 23 nm.
- ➢ FIN = 5, 5.5, 6, 6.5, and 7 nm.
- ➢ EOT = 0.8, 0.85, 0.9, 0.95, and 1 nm.
- ✓ Data of interpolated LUTs are validated using TCAD simulator

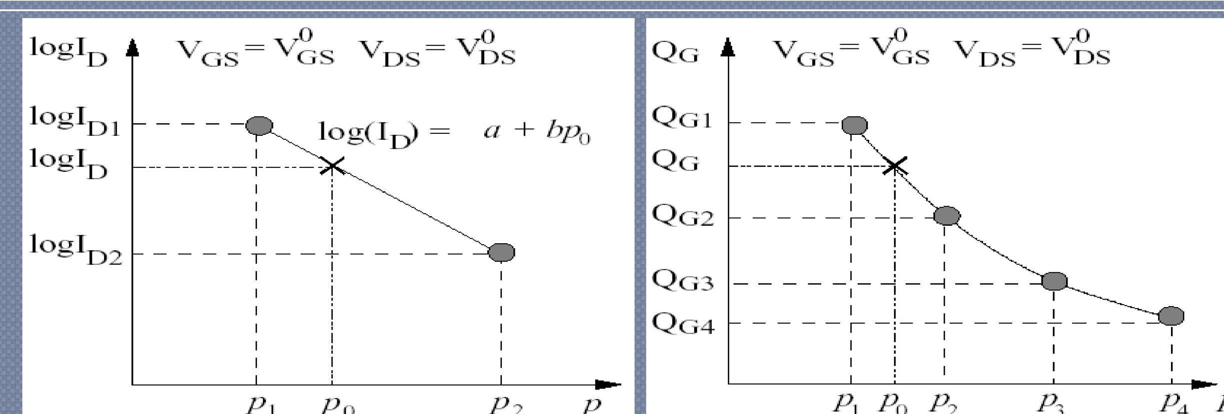

Fig. 7: LUT interpolation scheme for I_D and charge Q. 'p' represents process parameter.

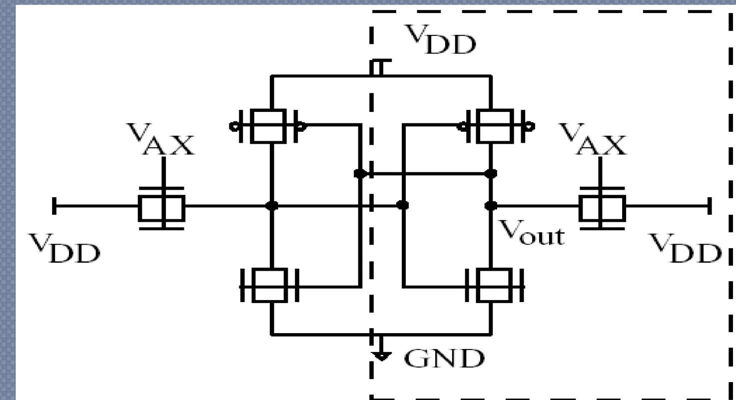

Fig. 8: SRAM Cell. The number of fins for all transistors is '1'. The circuit enclosed in dashed lines is simulated for process variations study.

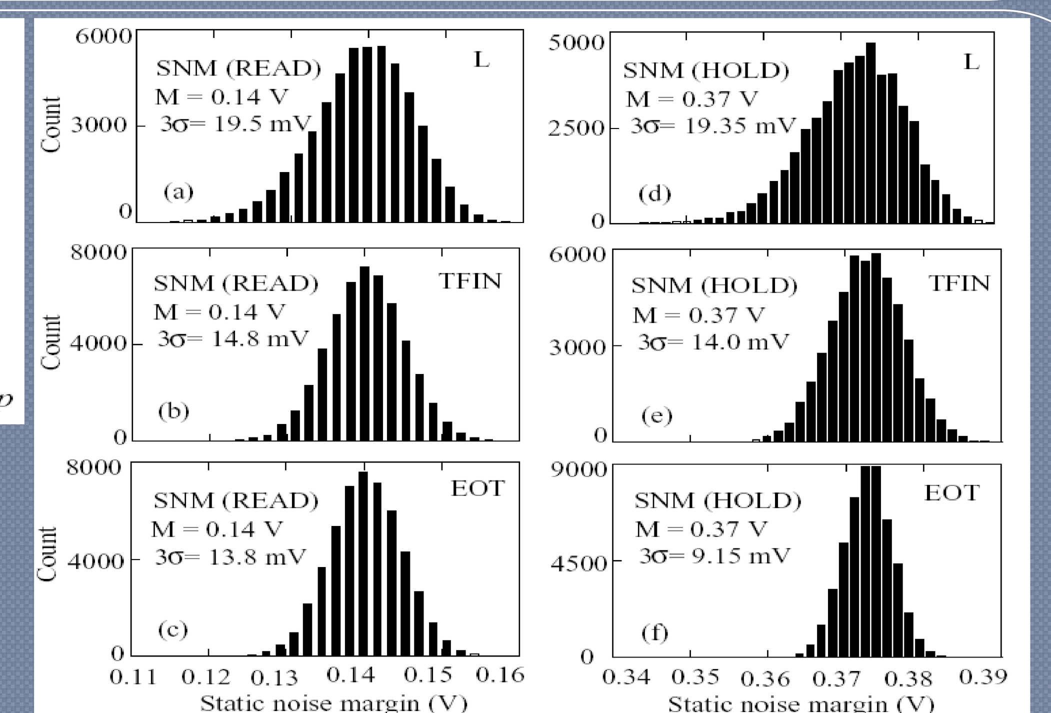

Fig. 9: Impact of process variations on SNM (static noise margin) of SRAM cell at V_{DD} = 1V. 50000 simulations are carried for each process parameter. 4 hours are required to generate these results (excludes LUT generation time).

References:

[1] R. A. Thakker, C. Sathe, A. B. Sachid, M. Shojaei Baghini, V. Ramgopal Rao, M. B. Patil, IEEE ASP-DAC, pp. 504-509, Japan, Jan. 2009.
[2] R. A. Thakker, C. Sathe, A. B. Sachid, M. Shojaei Baghini, V. Ramgopal Rao, M. B. Patil, IEEE Transactions on CAD, pp. 1061-1070, July 2009.
[3] R. A. Thakker, C. Sathe, M. Shojaei Baghini, M. B. Patil, IEEE Transactions on CAD, pp. 627-631, Vol. 29, April 2010.