Compact Model Extensions for Realistic Circuit Simulation: a Perspective from Industry

MOSAK Workshop

Jaypee Institute of Information Technology (JIIT)

Noida, 16th March 2012

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Abstract

- While CMOS Technology scaling has been steadily pursued to offer deca-nanometer devices, Circuit Design Community has benefited from successful development of core compact models able to capture important aspects of MOSFET electrical behavior in Circuit simulation tools. While BSIM4 models is still widely used within Industry for planar Bulk and SOI CMOS technologies, new MOSFET model generation (PSP, HiSIM…) has enabled high accuracy for Analog-Rf Circuits Design. Moreover, innovative modeling solutions are coming to Industry for new devices like planar FDSOI or 3D Finfet transistors.

- Beyond the successful development of core models from Academia, model extensions are still needed to be developed in Industry for a bunch of Technology and Design dependent effects, in close interaction with the Design tool providers to enable continuity of Design flow.

- Presentation will highlight model extensions developed in Industry to account for realistic Layout of single devices met due to circuit integration; examples of applications dealing with modeling of MOSFET Parasitics and Layout Proximity effects will be highlighted. The presentation is intended to bring circuit designers and compact modelers with a survey of such effects through their potential impact, and examples of methodology implementation.

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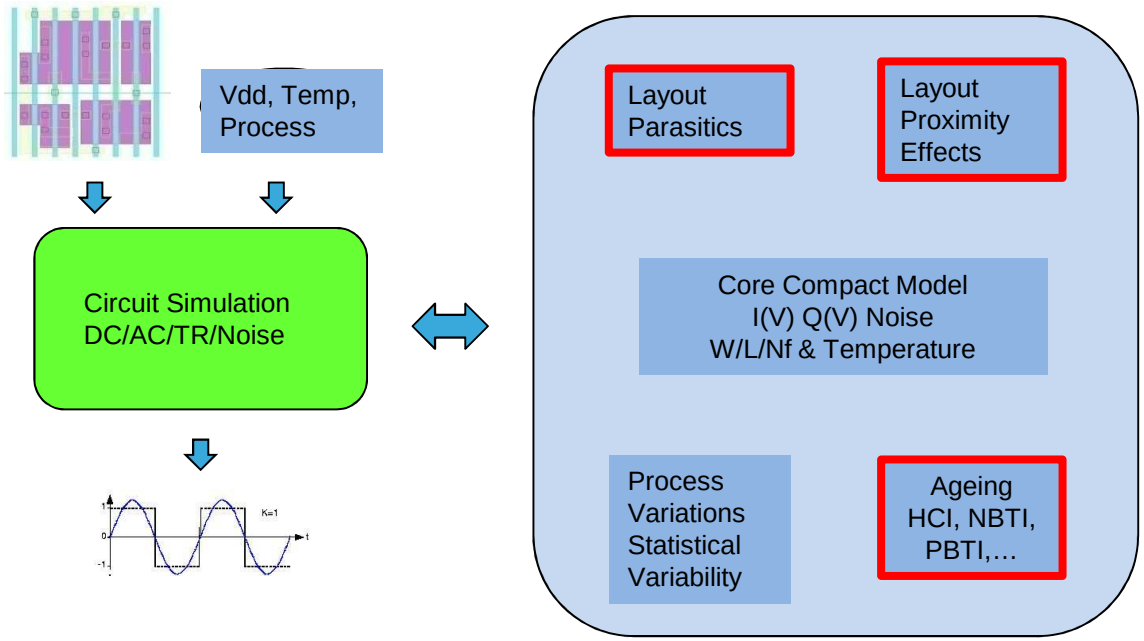
Contents

- MOSFET Compact Model Extensions for Realistic Circuit Simulation: A Perspective from Industry

- Objective
- Parasitic capacitances
- Layout Proximity effects
- Reliability aware Design
- Summary and Perspective

Objective



- *Core* models account for Bias, Geometry (W/L/NF) and Temperature, Noise
- *Extensions* account *for Parasitics, Layout effects, Process Variations,* and *Ageing*
- *Circuit simulation methodologies* need to be adapted concurently and made compatible with Design flow

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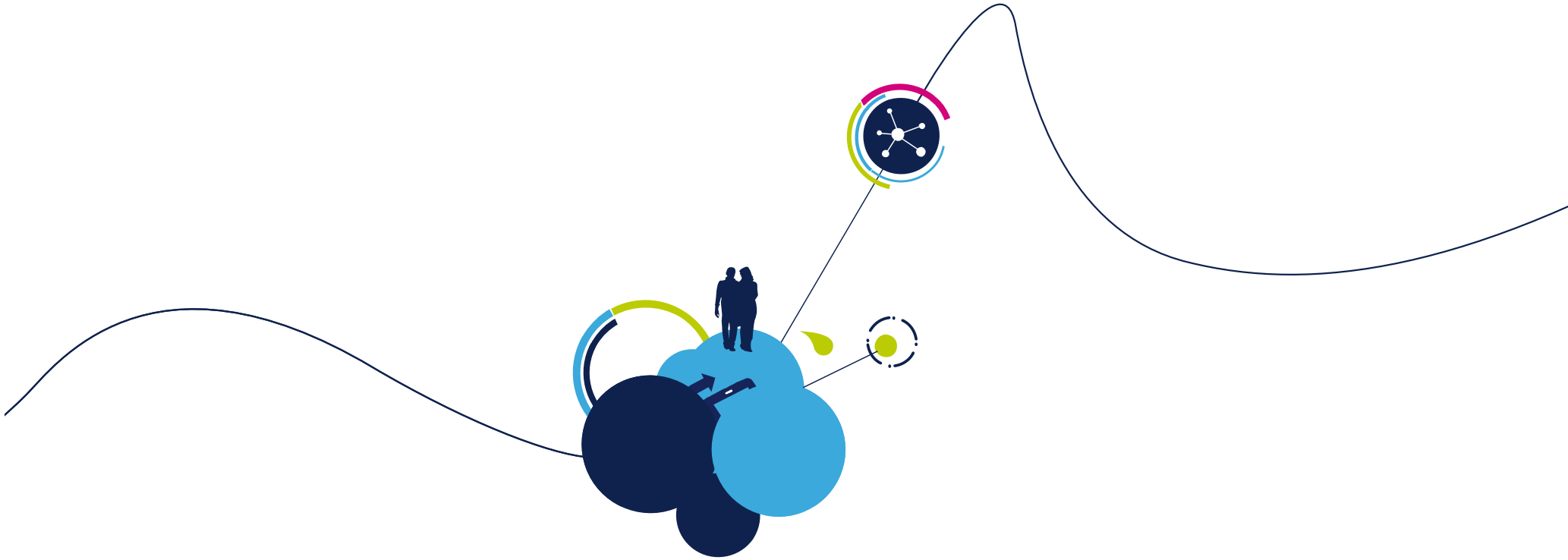

MOSFET Parasitics

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MOSFET Parasitic effects

- Extrinsic Parasitic capacitances
- Dependences to Layout
- Modeling/Simulation approach
- Perspective and ITRS

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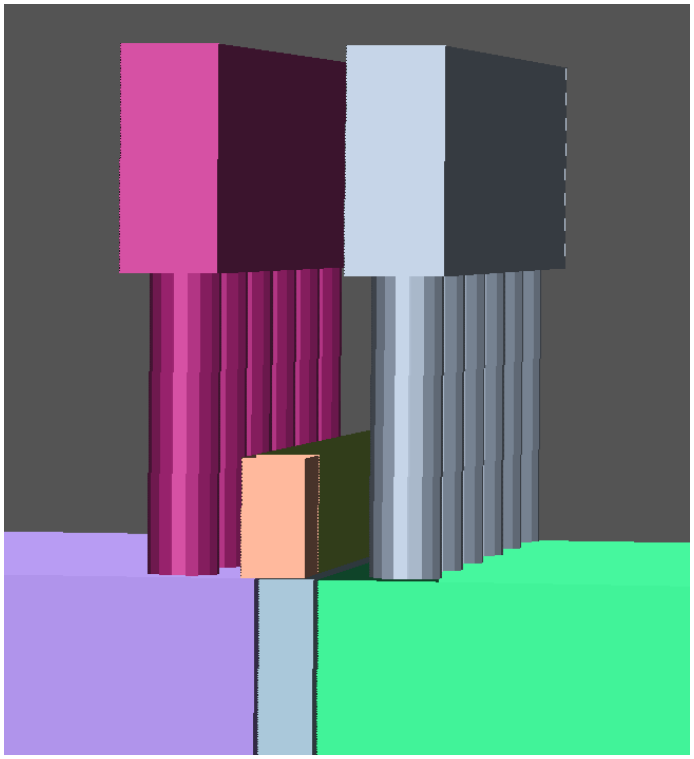
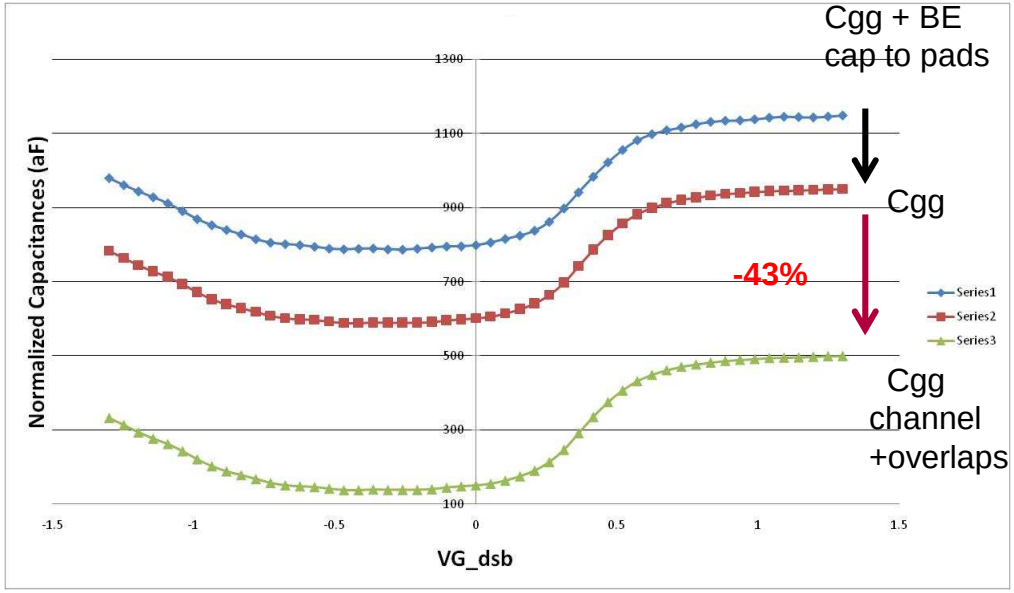
MOSFET Parasitic Capacitances



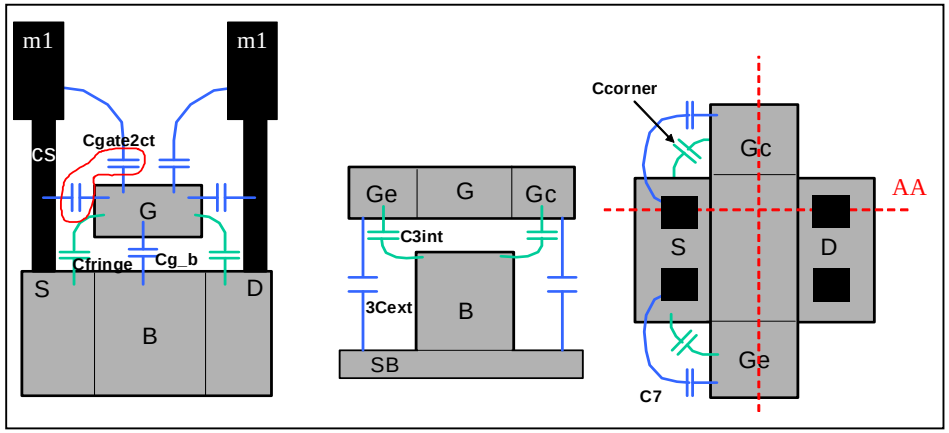
MOSFET 3D view with fully contacted SD access



Nmos Lnominal Gate Capacitance

- Even for Planar Mosfets, Parasitic Capacitances surrounding gate is a 3D problem
- Cgg @Lnom almost x2 through lateral coupling between Gate and SD regions
- Cgg depends on W/L, S/D cts number/pitch, distance between gate and S/D cts

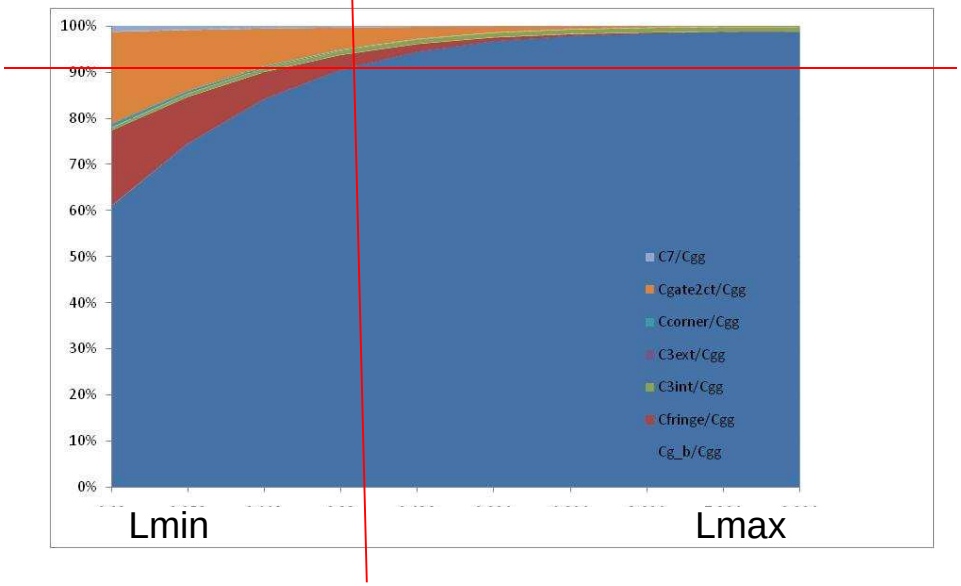
Scaling of MOSFET Capacitance partitioning on gate length



J.Mueller, SSE 2006

- Lscaling @W mean
  - Lmin: 40 % Cgg is extrinsic
    - Gate to S/D diffusion
    - Gate to S/D contacts
  - Lmin x 10: 90% Cgg is extrinsic

L dependence @Wnominal



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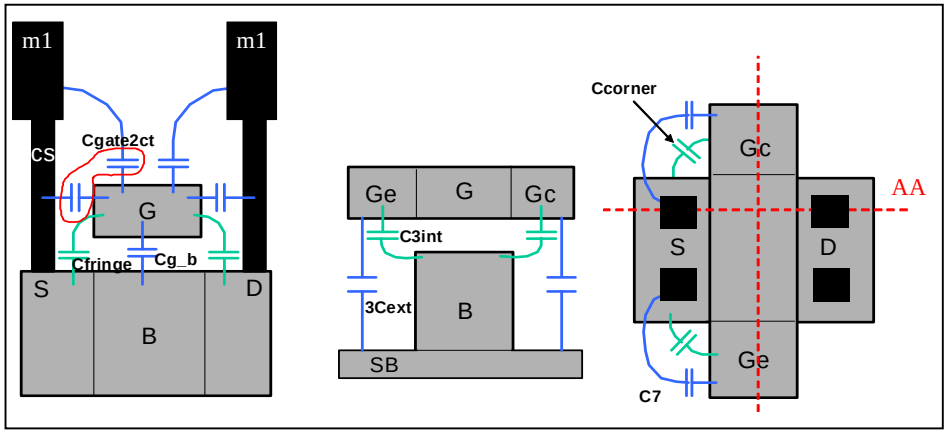
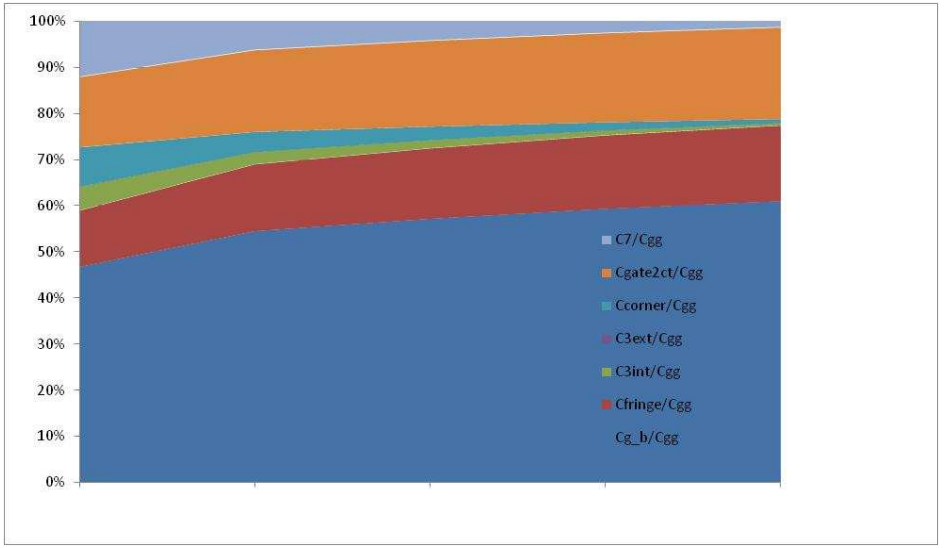
Scaling of MOSFET Capacitance partitioning on gate W



J.Mueller, SSE 2006

- Wscaling @Lnom

W dependence @Lmin



- W large: 40 % Cgg is extrinsic
  - Gate to S/D diffusion
  - Gate to S/D contacts
- W Narrow: up to to 53%
  - Corner capacitances

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Wmin Wmax

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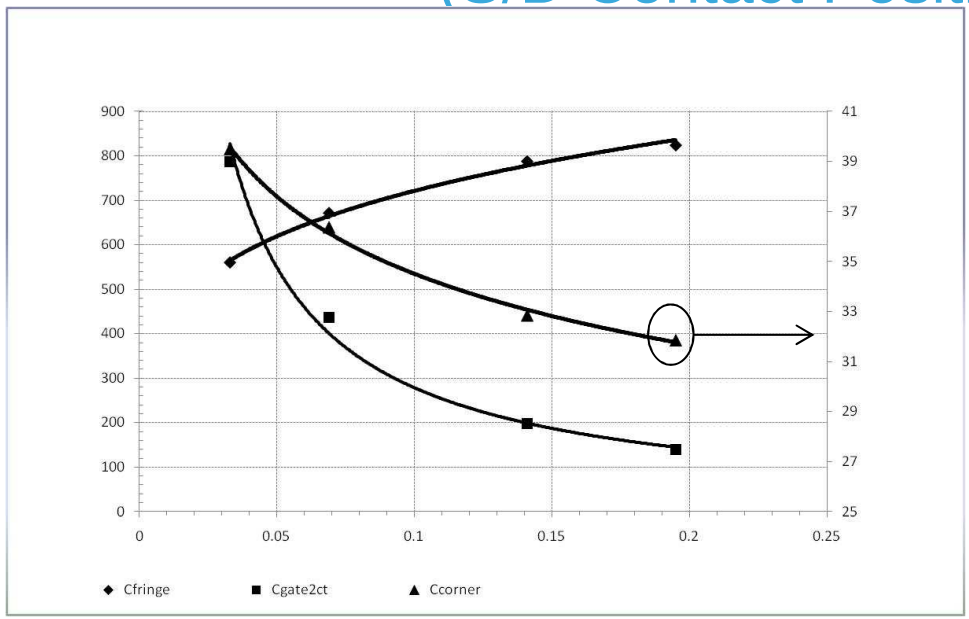
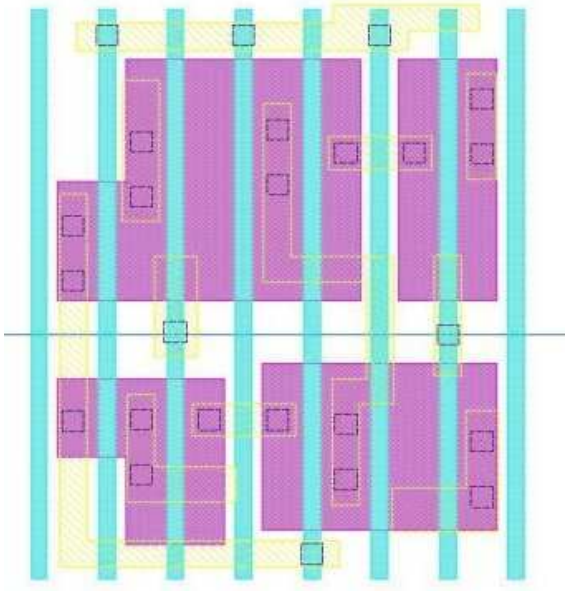
MOSFET capacitances in real Design (S/D Contact Position vs Gate)



Scaling Capacitances vs distance S/D Cts to Gate



Semi-regular Std cell layout (Example)

- Extrinsic Capacitances depend on
  - SD contact distance to gate (left)
  - Number of contacts (right)

- Solutions:
  - Core models: limited layout assumptions => suited for Pre-Layout simulation
  - PEX tool: adaptative to Layout style => suited for Post-Layout simulation
  - Number of netlist instance parameters required minimum for large circuit simulation

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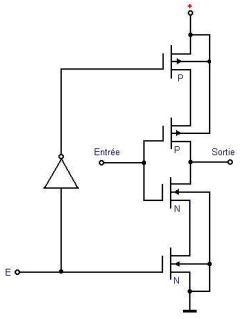
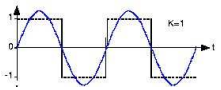
MOSFET capacitances in real Design (Adaptative simulation flow)

- Pre-layout simulation (default layout)



circuit netlist

simu

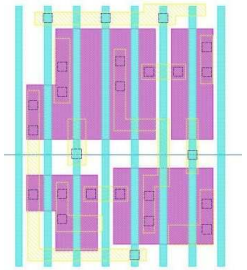


contains:
- network
- device instantiation
- device parameters (As/Ad/Sa/Sb/…) for default layout

- Mosfet R C parasitics for default layout , computed by SPICE model

Simulation results

- Post-layout simulation (real layout)



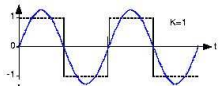
LVS step

circuit netlist

PEX

back annotated circuit netlist

simu



contains:
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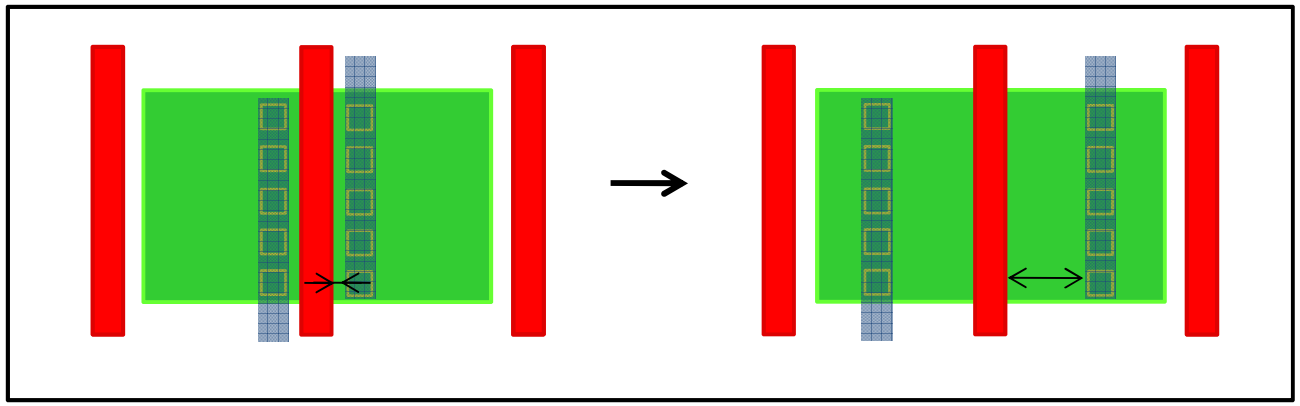
- device instantiation
- device parameters (As/Ad/Sa/Sb/…) computed from layout
- device parameters can be "geometrical" or "electrical"

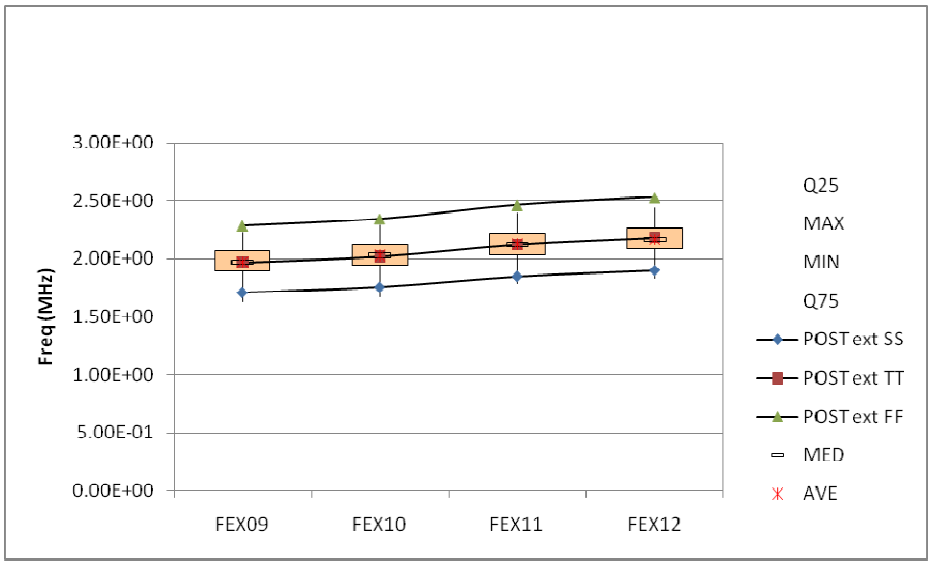
Addition of R C parasitics, computed from layout Applies to MOSFET devices and interconnect

Simulation results

Verification DOEs: Impact on RO frequency



RO	dgc
FEX09	Min
FEX10	X 1.43
FEX11	X 2.5
FEX12	X 5



- F increase vs dgc: benefit of extrinsic capacitance reduction
- Efficient CAD accuracy monitoring methodology.

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MOSFET Parasitics vs ITRS roadmap

- From ITRS, we have for each year and each device structure the following parameters:
  - **L**
  - **CPP (contacted gate pitch)**
  - **t_{inv}**
  - X_j for Bulk devices
  - **t_{si}** for FDSOI or multigate devices
- Structural parameters are derived =>

Parameters	Evaluation
t_{sp}	(CPP-L)/3
H_g	2L
W_{ext}	L
W	3xCPP
dL	L/4
t_{ox}	$2t_{inv}$
W	3xCPP
H_{si}	$3xt_{si}$
FP	$t_{si} + H_{si}$
N_{fin}	W/FP
t_{mask}	t_{si}

- Parasitics impact have been evaluated for each year for the following devices: Bulk, FDSOI, planar DG and FinFET (J.Lacord, SSDM 2011)

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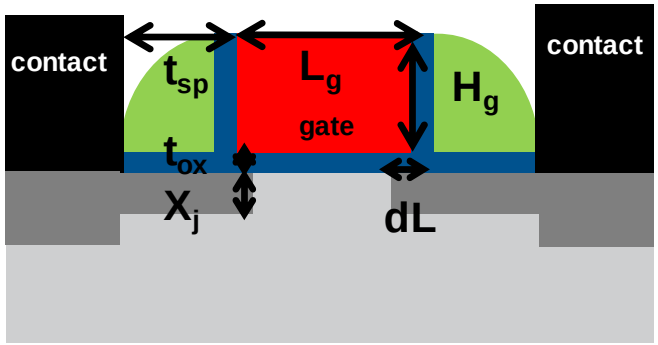
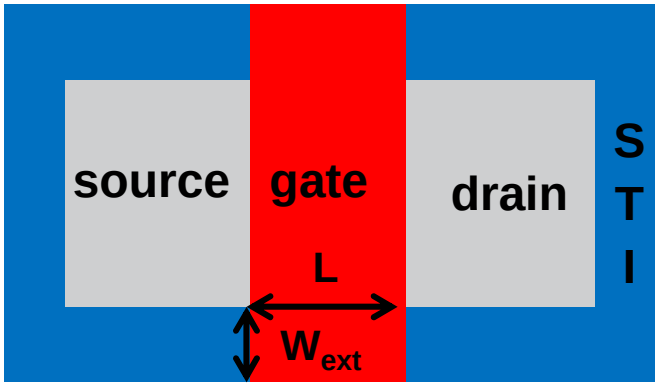
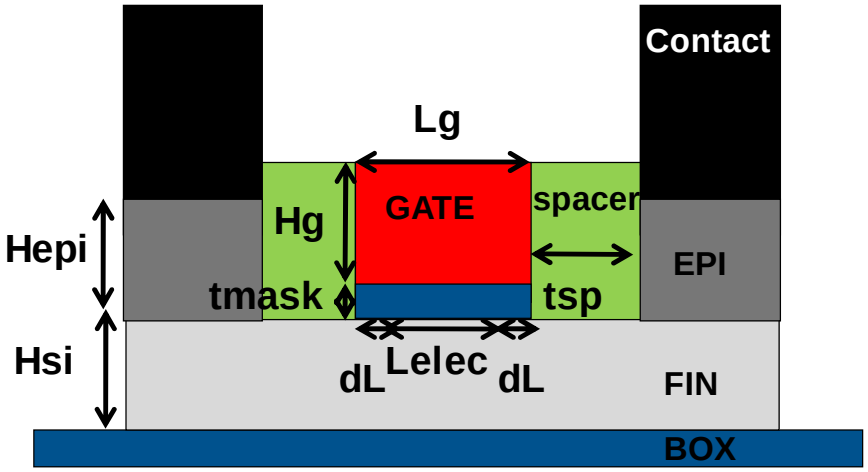
MOSFET Parasitics vs ITRS roadmap



Bulk FET cross-section

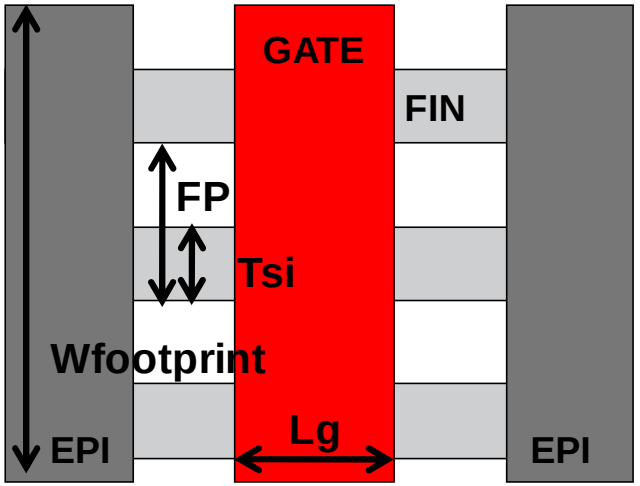


Bulk FET top view (wo contact)



FinFET cross-section

Courtesy of J.Lacord, SSDM 2011

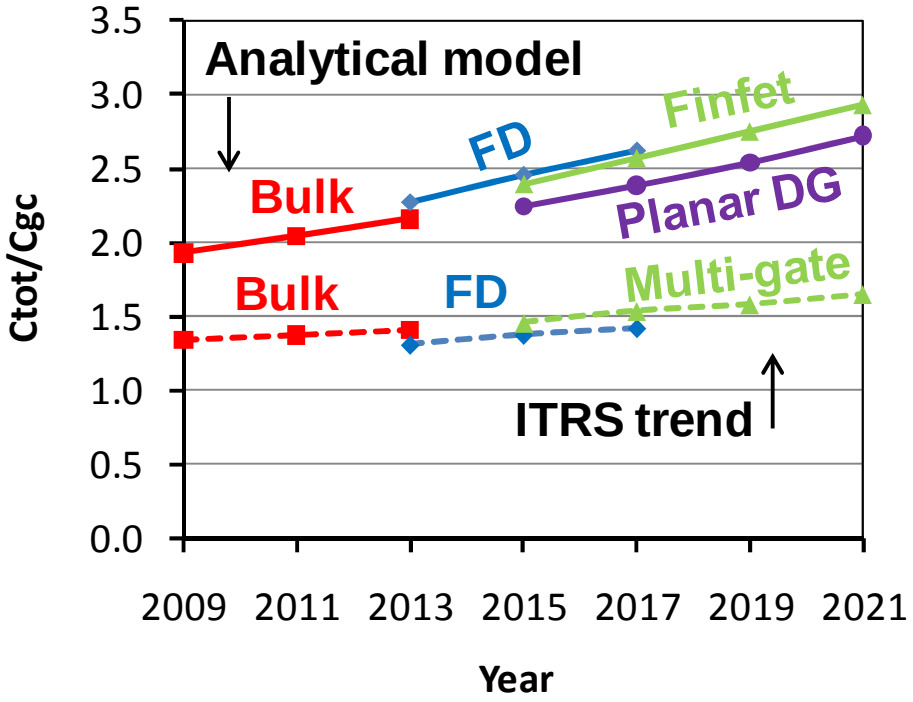


FinFET top view

MOSFET Parasitics vs ITRS roadmap

Total Gate + Parasitics over Gate cap. Ratio

$= C_{par}+C_{gc}$ ↘



Courtesy of J.Lacord, SSDM 2011

- ITRS Parasitics weight and evolution below FS simulation
- Planar DG presents a lower C_{tot}/C_{gc} ratio than FinFET MOSAK 2012 Q1

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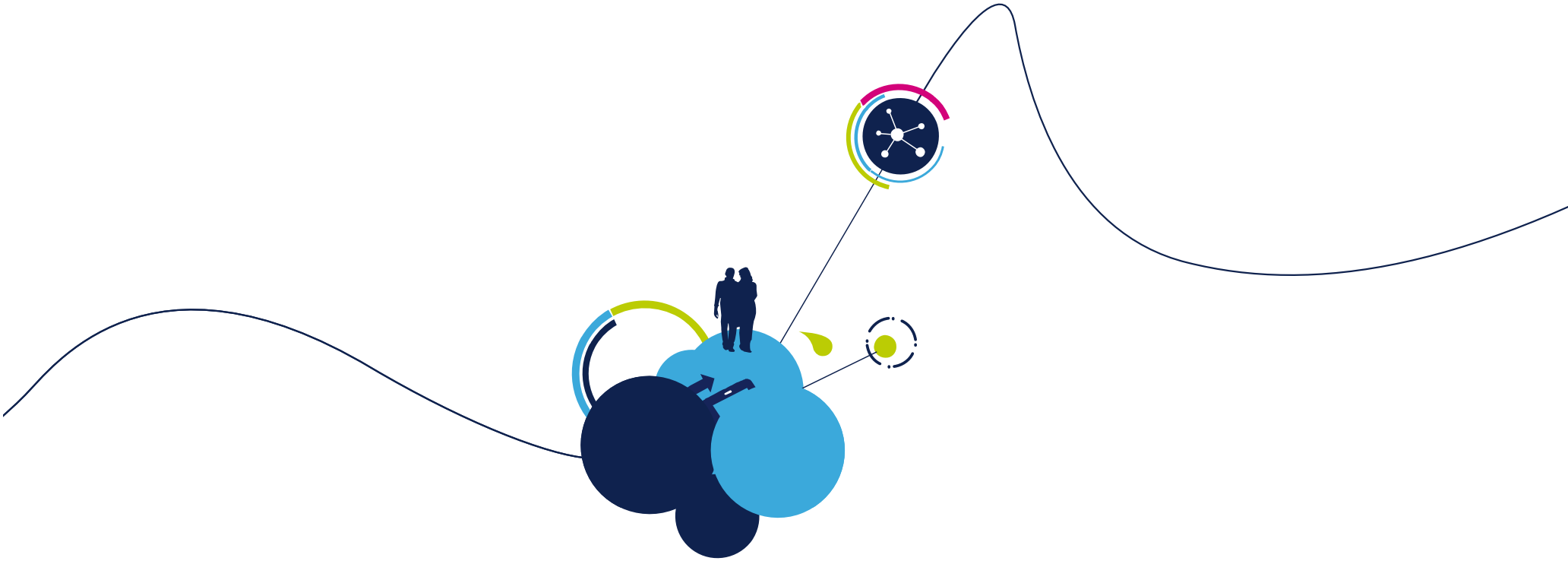

MOSFET Layout Proximity Effects

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Layout Proximity effects

- Overview
- Modeling approach
  - STI example
- Modeling Accuracy dilemna
- Simulation flow
- CAD Accuracy

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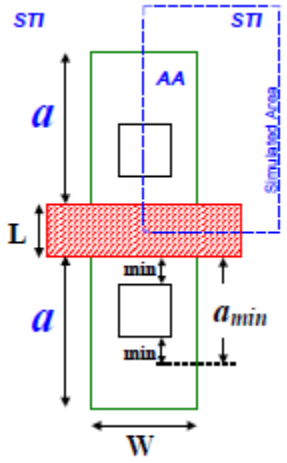
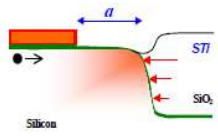
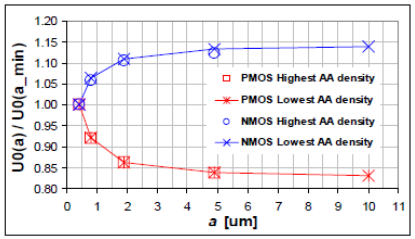
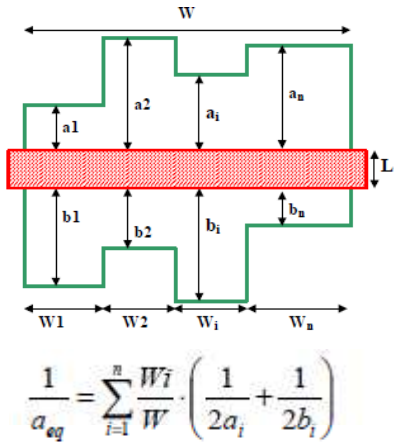
Layout Proximity effects: STI example

STI stress effect on Mobility (RA Bianchi, IEDM 2002)



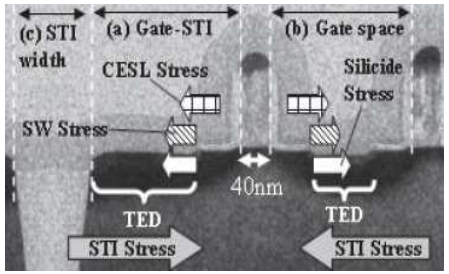




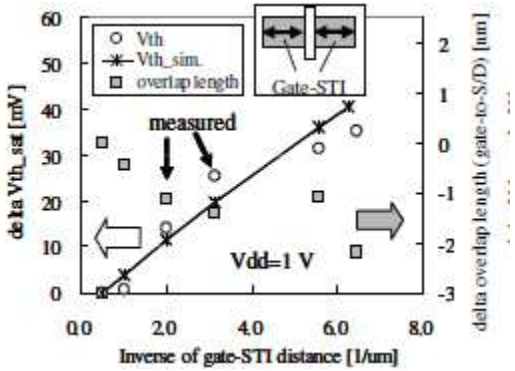


$$\frac{1}{a_{eq}} = \sum_{i=1}^{n} \frac{Wi}{W} \cdot \left(\frac{1}{2a_i} + \frac{1}{2b_i} \right)$$

STI stress effect on Mobility and VT (Tsuno, VLSI 2007)



Tsuno, VLSI 2007



- Regular Layout: Mobility impacted by Stress, VT impacted by SD diffusity (modulated by stress)
- Handling Complex Layout in Design flow requires approximations:
  - Implementation shared bw Netlisting (Geometrical parameters) and Model (Electrical parameters)

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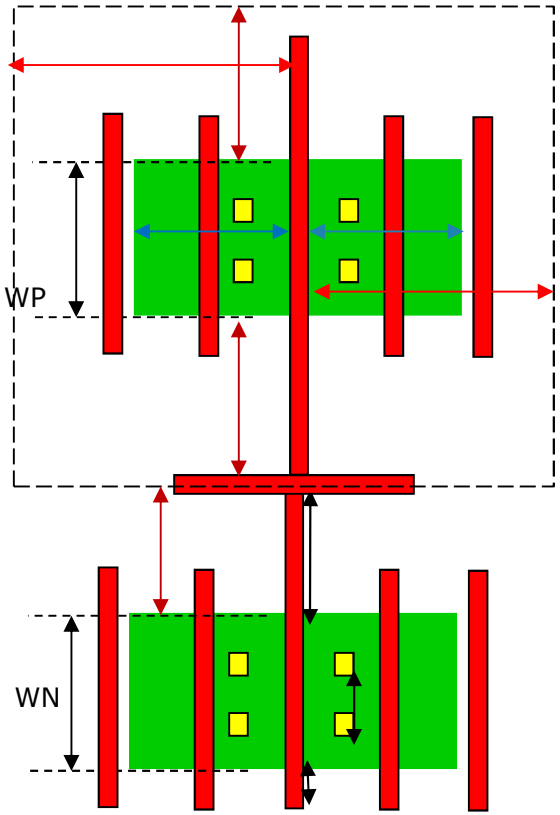
- Accuracy verification is challenging

MOSFET Layout Proximity effects overview

Effect	Contributions	Critical distance	Post-Layout Per Instance parameters
WPE	Ion scattering on well photoresist	>1um	SCA, SCB, SCC
STI(LOD)	STI Stress SD diffusion	1um Local	SA, SB
STI (OD2OD)	Litho and Etch STI stress	Context 1um	VT and Mu correction
Active corner rounding	Litho and Etch	Local	Weff correction
Gate pitch	Litho and Etch CESL Stress SD diffusion	Context Context up to 1 um Local	VT and Mu correction
Gate corner rounding	Litho and Etch	Local	Leff correction
Contacts position	SD Rseries Channel stress	Local	Rs and Cs correction
Others …			



• A bunch of Design dependent effects related to distances between Well, Gate, Active, Contact layer patterns and related density context

•Different physical effects interplay; impact, amplitude are technology dependent

•Each transistor sensitivity to each effect also depends on instance W/L

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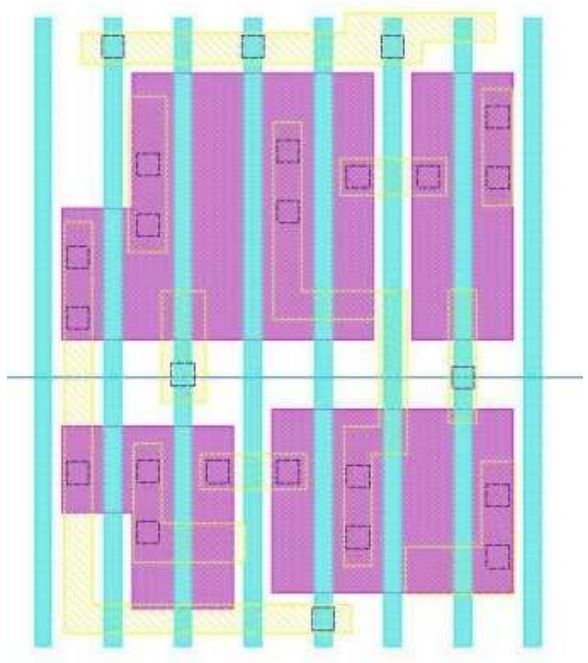
MOSFET proximity effects: Accuracy dilemna

- A bunch of effects with 1-10% impact of performance (Low Power technology), and more (High Power technology , where Stress effect is dominant)

- **Characterization dilemna: Layout DOEs**
  - WPE: 4W x 4L x 6 distances x 2 orientations x 2 N/P devices= 394 DUTs
  - Overall about 2K DUTs per N/P device, not considering interaction between effects!

- **CAD Netlisting dilemna : Post Layout extraction**
  - Nb Geometrical instances > 100, loss of simulation efficiency
  - Pre-processing of geometrical/ electrical parameter variation through LVS: a must!

- **Modeling:**
  - Compact modeling of all effects with interactions is not experimentally applicable
  - Focus on first order layout effects and their dependence with W/L
  - Monitoring of CAD + Models accuracy through test structures offering efficient test methods



Layout example

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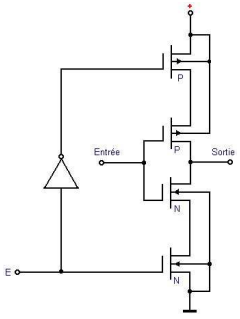
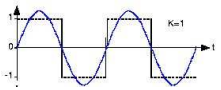
MOSFET capacitances in real Design (Adaptative simulation flow)

- Pre-layout simulation (default layout)



circuit netlist

simu



contains:
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- device parameters (Sa/Sb/Sc…) for default layout

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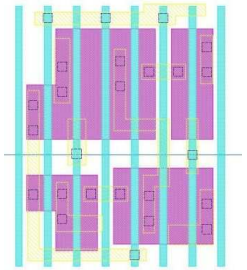
Simulation results

- Post-layout simulation (real layout)



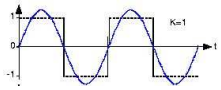
LVS step

circuit netlist

PEX

back annotated circuit netlist

simu

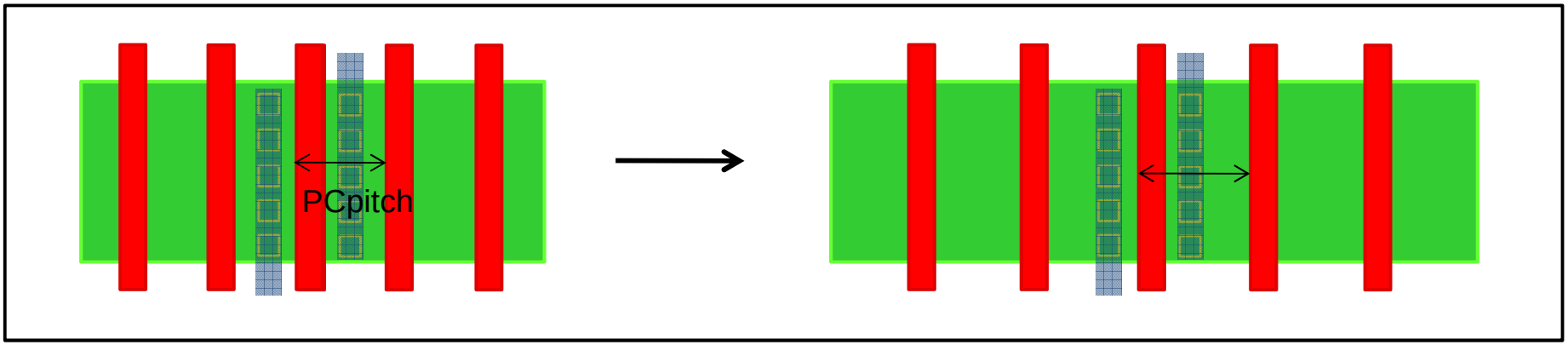


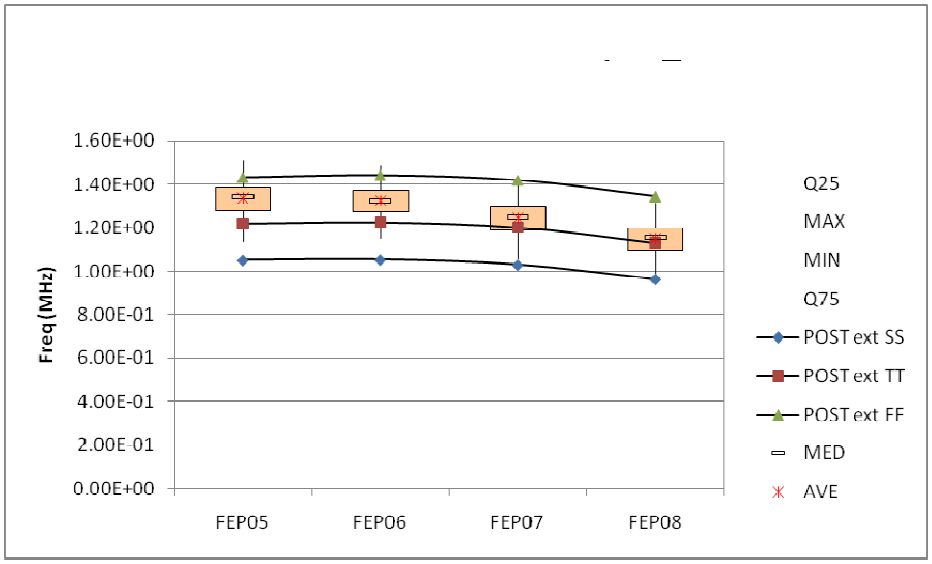
contains:
-network
- device instantiation
- device parameters (computed from layout
-
- device parameters can be "geometrical" (Sa/Sb/Sc…) or "electrical" (dvt, dmu)

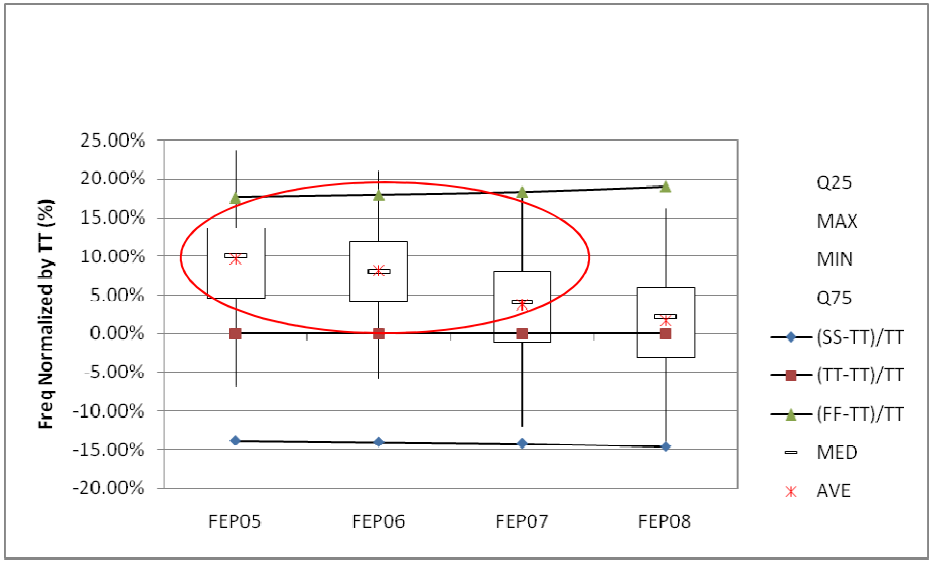
Addition of R C parasitics, computed from layout Applies to MOSFET devices and interconnect

Simulation results

MOSFET Layout Proximity effects: CAD Accuracy







- Example of Monitoring Gate Pitch effects with Ring Oscillator: CAD to Silicon mismatch can be depicted

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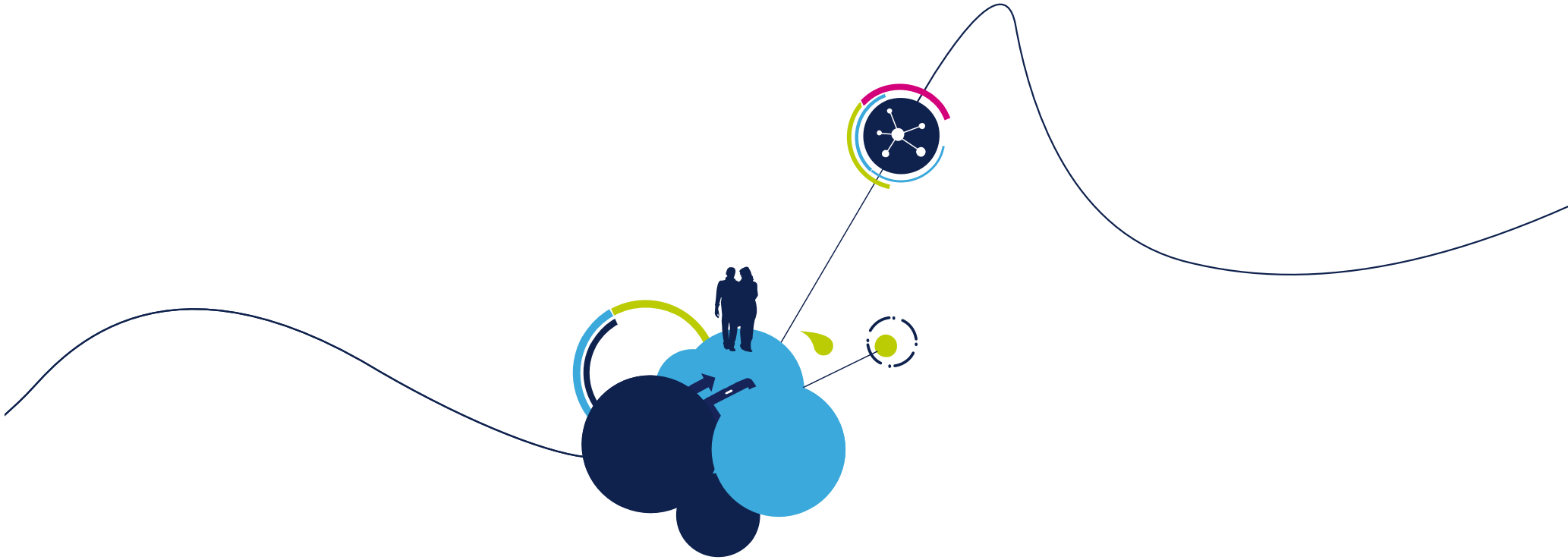

Reliability Aware Design

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Reliability Aware Design

- Reliability aware design

- Results: Std Cells

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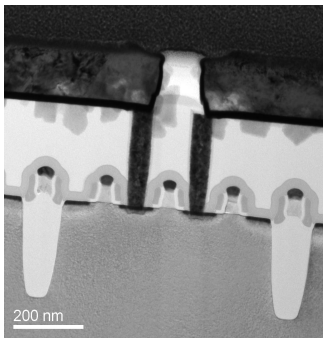
Reliability-aware design

DEVICE LEVEL



All degradation modes impact?

CIRCUIT LEVEL

Reliability impact on circuits is a function of

- ❑ operating modes of circuits,
- ❑ operating conditions faced by devices as a combination of these modes and the various input stimuli
- ❑ sensitivity of the performance of the circuit in the context of its place in design hierarchy

  E.g., a small shift in differential pair could affect the product, while a big shift in transistors in a power-down control block may affect nothing

Design-in Reliability (DiR) =

set of methodologies and tools enabling **quantitative reliability assessment** at design-level

- Translate device reliability information for use by circuits
  - Library reliability information is requested by system designers
- Identify potential reliability problem conditions
  - Take into account the actual operating conditions of a design library
    - mode, stimuli, ambient conditions
- **Secure without over-design**

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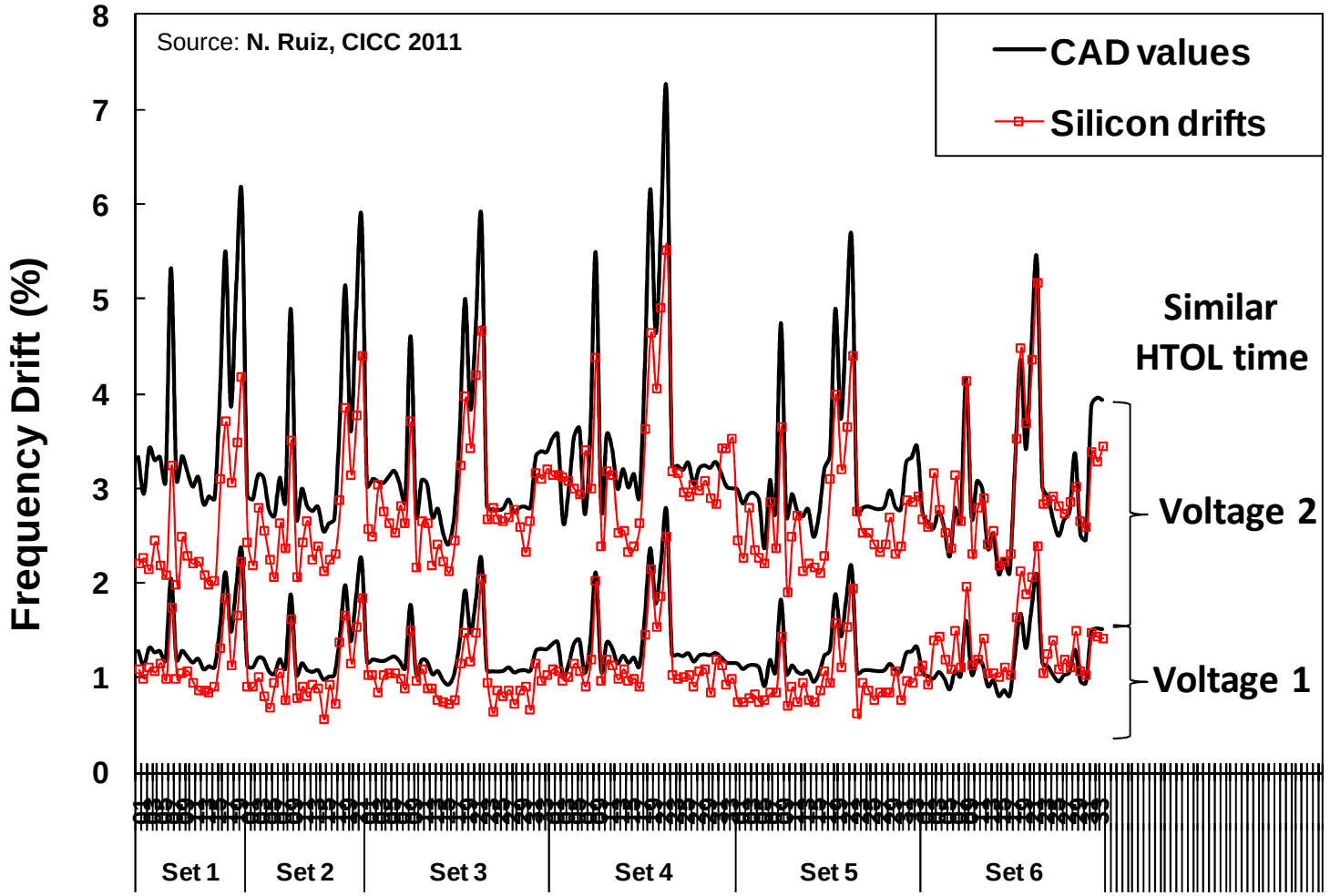
Reliability-aware modeling – Std cells results

- Reliability CAD values must be compared to drifts observed during HTOL test campaigns on library qualification testchips.



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Summary

- Mosfet parasitics are performance limiting factors
  - Extrinsic cap may exceed ~x2 intrinsic cap for coming device generations
- Impact of Layout effects is difficult to estimate for coming technologies (as long as impact of each individual effect is less than 10 %) .
  - The experimental methodology learnings to account for these effects in current technologies will help
- Reliability aware Design is coming
  - Requires a set of methodologies and tools enabling quantitative life-time assessment at circuit-level
- In Industry, those subjects will keep attention from the Modeling and Reliability expert communities from now and through the coming years.

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