Modeling and Parameter Extraction of SiGe HBTs at Cryogenic Temperatures using Open-Source Tools DMT and VerilogAE

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OUTLINE

- Introduction, device and measurement set-up
- Transfer current of SiGe HBTs at cryogenic temperature
- Parameter extraction tools: DMT and VerilogAE
- Conclusions

Introduction, device and measurement set-up

Motivation

- Silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology has achieved f_T > 500 GHz for industry prototyping processes
- BiCMOS technology has enabled commercial and emerging mm- and sub-mm-wave system-on-chip applications
- many applications can benefit from operating electronic circuits and devices at cryogenic temperatures (CTs):
  - space exploration
  - material physics and chemistry
  - satellites (e.g. for providing world-wide access to the Internet)
  - quantum computing
- SiGe HBTs have been demonstrated to operate at CTs with superior performance compared to room temperature => high speed can be traded in for lower noise and energy efficiency

=>attractive technology for cryogenic applications

- Circuit design at cryogenic temperatures requires accurate compact model

Status of SiGe HBT modeling for low temperatures

- Process design kits (PDKs) for cryogenic circuit design still not available

- need to extend ALL device models to cover low temperature operation

- Challenges for semiconductor foundries:
  - - significant (additional) measurement effort, lack of cryo equipment
  - - need to extend compact models for all devices (actives and passives)
  - - reliance on standard models for transistors
- HBT mainstream [standard] models used by foundries: [HICUM, MEXTRAM], SGP, VBIC
  - - VA uses the same EC/models for large and small signal
  - - *All* compact models: main current and charge formulations based on drift-diffusion (DD) transport

=>present HBT compact models miss physics of low temperatures, especially tunneling current

Status of SiGe HBT modelingfor low temperatures

- Attempts of modeling SiGe HBTs at low temperatures so far:
  - Standard SGP with an extension: fit DC down to 78 K (old SiGe tech.) [1]
  - MEXTRAM with an extension: fit DC down to 43 K, and AC down to 93 K (old SiGe tech.) [2]
  - small-signal EC: fit measurement at CT only for single *T* and single operating point (advanced SiGe tech.) [3]
  - HICUM/L0 (advanced SiGe tech.): fit of existing parameters to cryo data at 12 K [4]
  - HICUM/L2 (advanced SiGe tech.): extension by empirical formulations and parameters fit DC and AC data from 4.3 to 298 K [5]

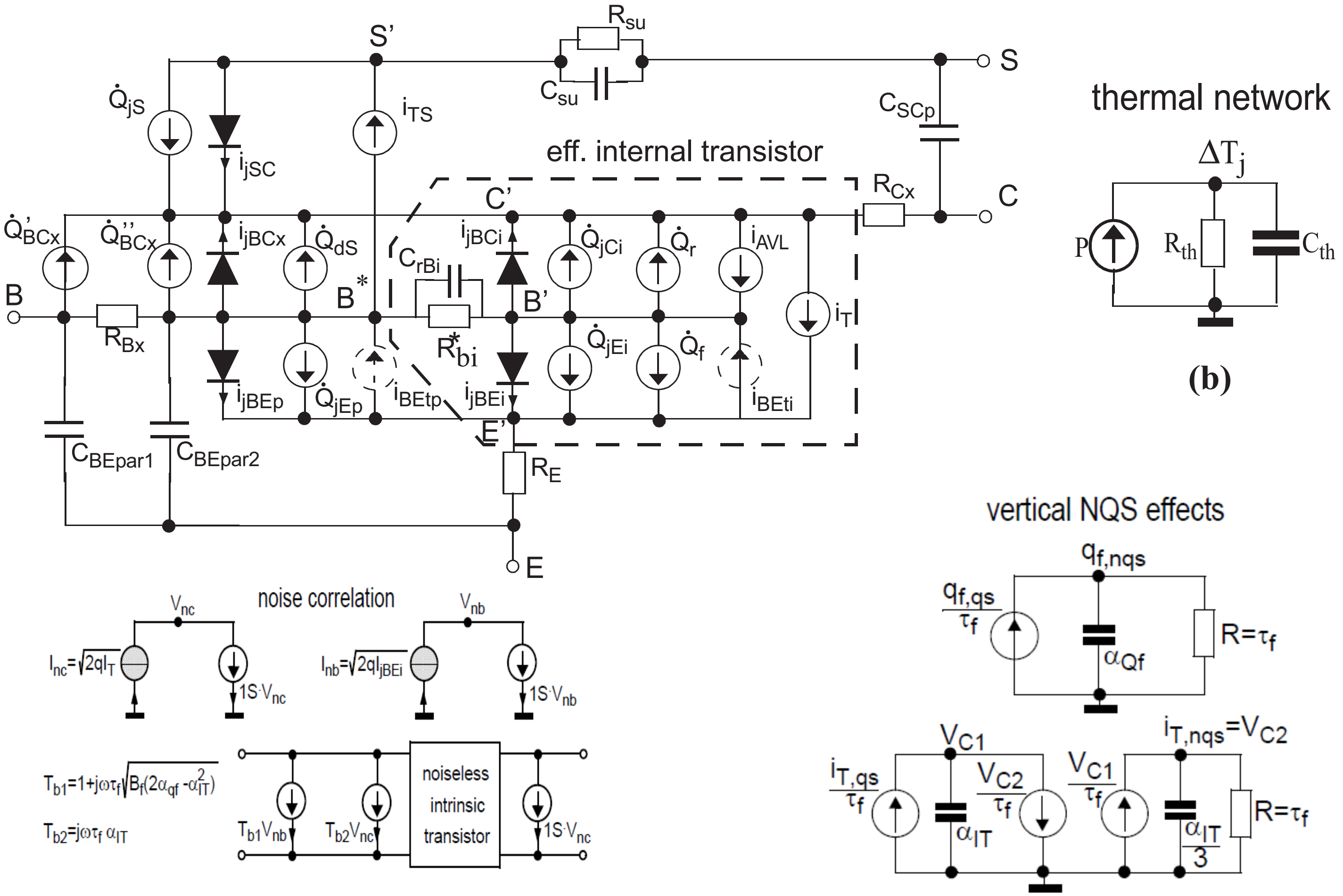
=>focus here: large-signal compact HBT modeling for "cryogenic" PDK base on HICUM/L2 v3.0.0

Ref.	BiCMOS Tech.	f_T (GHz)	DC	AC	*T* scaling (K)	bias scaling
[1]	0.25 μm	50	✓		78 to 300	✓
[2]	0.25 μm	50	✓	✓	43 to 393(DC) 93 to 383(AC)	✓
[3]	0.13 μm	170	✓	✓	15, 40, 77, 120, 200, 300*	
[4]	0.13 μm	260	✓	✓	12	✓
[5]	0.13 μm	300	✓	✓	4.3 to 298	✓

*The model parameters were optimized for each temperature, respectively.

Large-signal equivalent circuit of HICUM/L2

(physics-based geometry-scalable industry standard model [6])



=>each element to be investigated over a wide *T* range

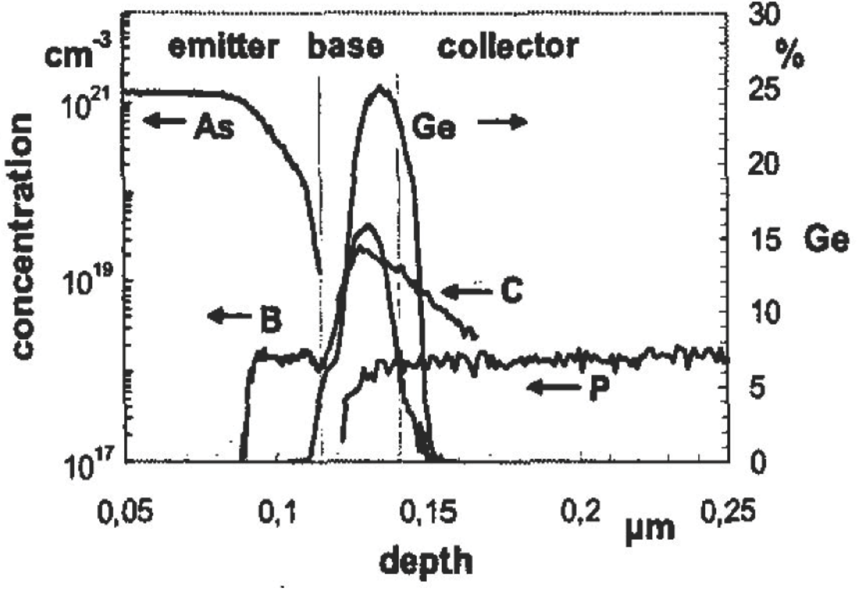
Investigated devices

- IHP SG13G2 as well as two variants => tunneling characterization
- IHP D7 prototyping technology => modeling
  - with (f_T, f_{max}) > (300, 500) GHz at room temperature
  - CBEBC configuration
  - $b_{E,drawn}$ = 0.13um, $l_{E,drawn}$ = 10.16um
- measurement results from 10 K to 473 K for HBT key characteristics
  - Forward, reverse gummel, output characteristics;
  - I_{BE}, I_{BC}
  - Cold S, Hot S parameter;
- all key characteristics shown for V_{BC} = 0V

SiGeC HBT technology

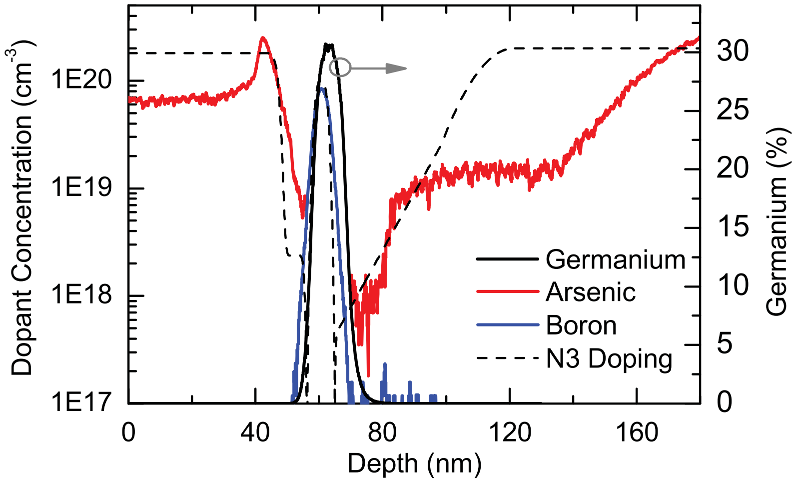
production technology

f_T = 200 GHz, f_{max} = 275 GHz [7]



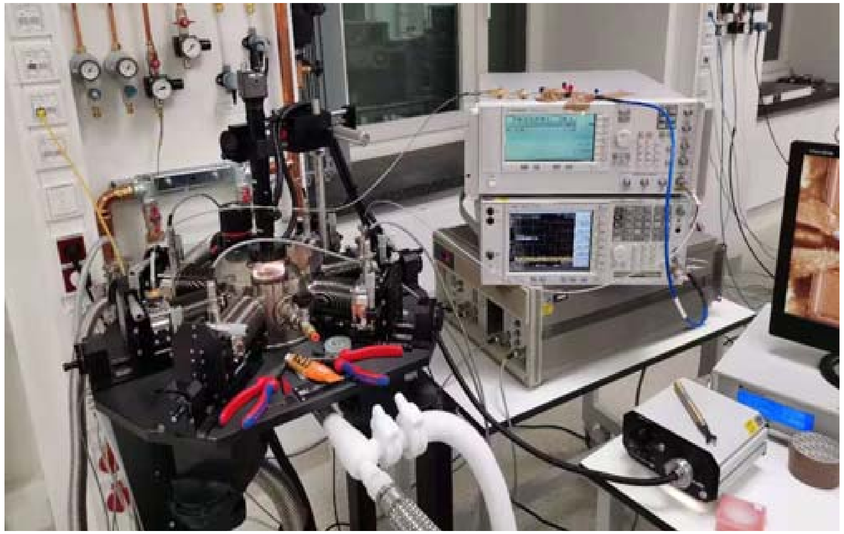
prototyping technology

f_T = 500 GHz, f_{max} = 700 GHz [8]



- doping concentrations
  - emitter, base, and buried layer highly doped => **no freeze-out**
  - internal collector: highly doped in high-speed HBTs => **no freeze-out**
  - internal collector: low/moderate in high-voltage HBTs, older technology => **partial freeze-out**
- base width: 25 nm ...12 nm => CE tunneling in advanced HBTs at low T

Measurement setup



- Electrical measurement equipment the same as at RT
- Differences compared to RT probe station:
  - vacuum chamber: $<10^{-5}$mbar, avoid air condensation, cryogenic probe station
  - vacuum pump: series connected diaphragm pump and turbo pump
  - cryogen, such as liquid helium (4 K) or liquid nitrogen (77 K)
  - dewar: container for cryogen
  - temperature controller: heat up the chuck
  - specialized DC and microwave probes

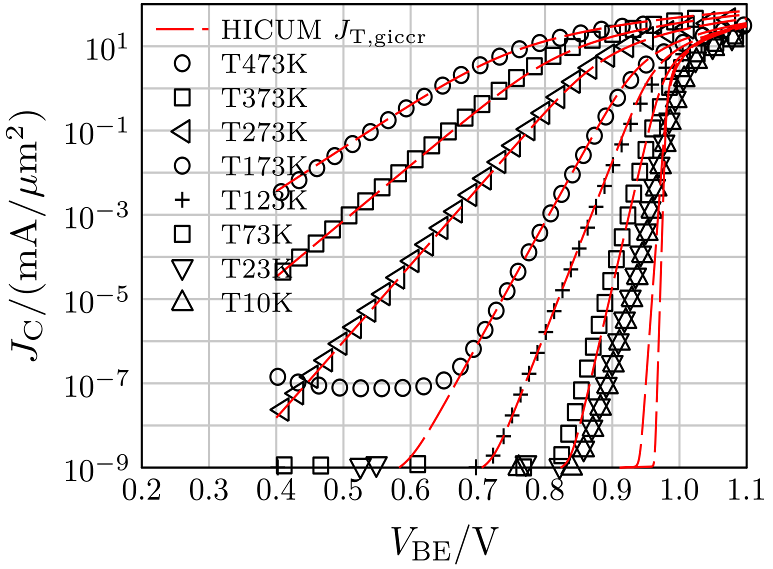
Transfer current at cryogenic temperature

Existing compact model vs. measurements

- Low-temperature reduces kinetic carrier energy => lower diffusivity
- *T* decreases -> bandgap increases -> larger BE barrier (V_{DE}) prevents diffusion of electrons from E to C

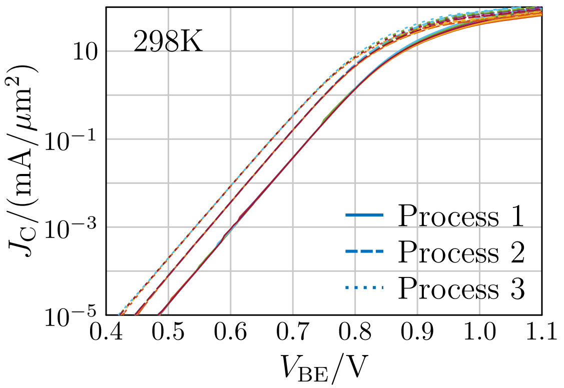
  => much lower drift-diffusion current as observed in measurements

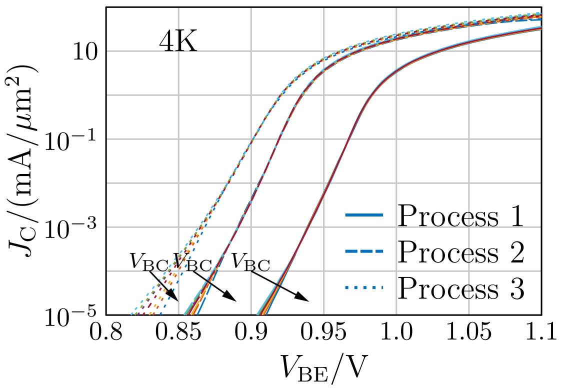
- GICCR (DD) vs. Meas
  - well agreement from 473 to 73 K
  - model underestimates meas. below 73 K
- Previous investigation (in base) for *T* < 73K:
  - low and medium current densities: tunneling [9]
  - high current densities: DD [10] or quasi-ballistic [11] transport => dispute lack of verification

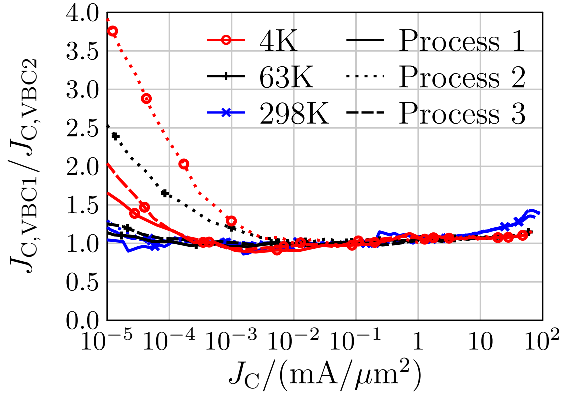


- *No* suitable physics-based tunneling current expression available for compact-models
  - only qualitative discussions of experimental results and/or device simulations

Characterization of tunneling current



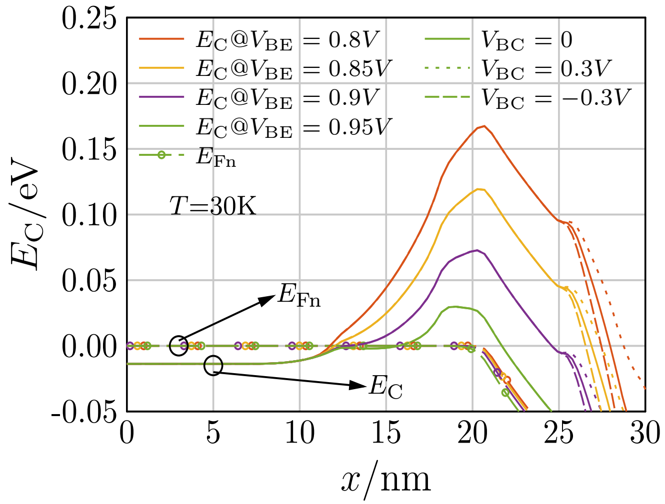


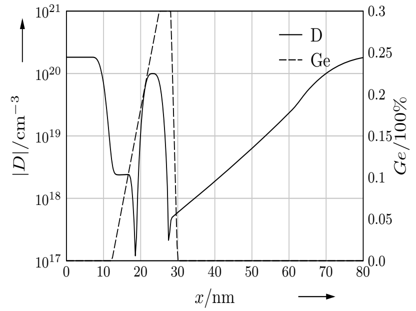


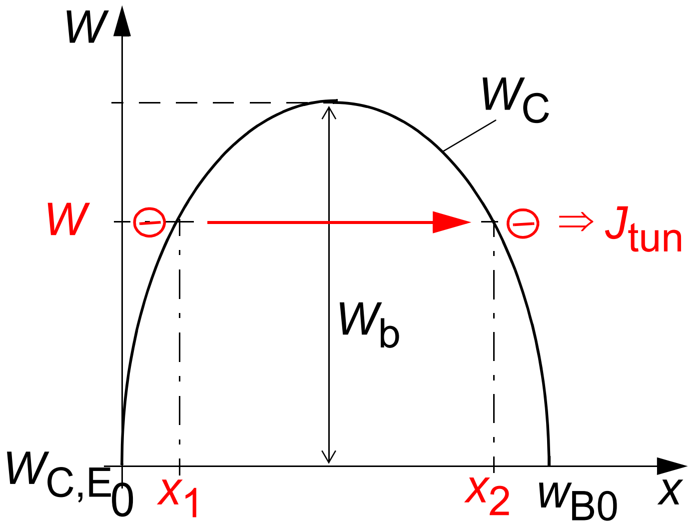
- Transfer characteristic (with different V_{BC} from -0.5 to 0.5 V) of three processes:
  - At 298 K (left figure), no obvious V_{BC} dependence of J_C at low and medium current densities;
  - At 4 K (medium figure), clear V_{BC} dependence of J_C at low and medium current densities due to tunneling current;
  - Ratio of J_C (right figure) with different V_{BC} shows the same trend:
    - At 298 K, ratio equals to 1
    - At CTs, ratio increases with reduced T
- Same process node (0.13um), but different tunneling current due to base doping concentration => different conduction barrier widths

$\Rightarrow$ tunneling current becomes significant at low and medium current densities at CTs

Potential barrier in base







- Left figure: Band diagram from TCAD simulation on similar profile at 30 K and different bias conditions
  - With increased V_{BE}, the conduction barrier in base becomes lower and narrower, which increases the tunneling probability
- Right figure: a schematic potential profile
  - Parabolic profile is used for analytical derivation of tunneling transmission factor

Compact model equation

- Transfer tunneling current is generally given by

$$J_{\mathrm{Ttu}} = \frac{2q}{h^3}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{0}^{p_{x2}} T_{\mathrm{tu}} f_{\mathrm{nE}}(1-f_{\mathrm{nC}}) v_{\mathrm{x}}\, dp_x dp_y dp_z ,$$

with $f_{\mathrm{nE}}(f_{\mathrm{nC}})$ as Fermi-function in the emitter (collector), and T_{tu} as tunneling transimission probability. Under several assumption

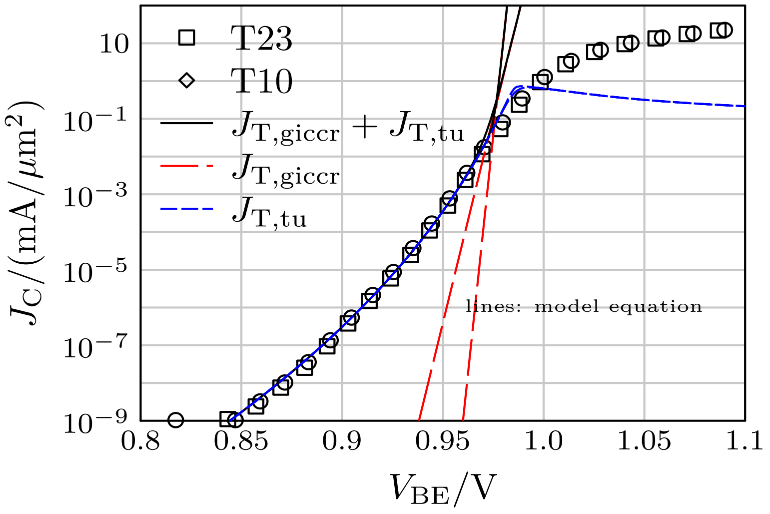
$$J_{\mathrm{Ttu}} = c_{\mathrm{Ttu,s}} \int_{W_{\mathrm{C,E}}}^{W_{\mathrm{Fn,E}}} T_{\mathrm{tu}}\, dW_{\mathrm{x}} \text{ for } W_{\mathrm{b}} \geq \Delta W_{\mathrm{E}} .$$

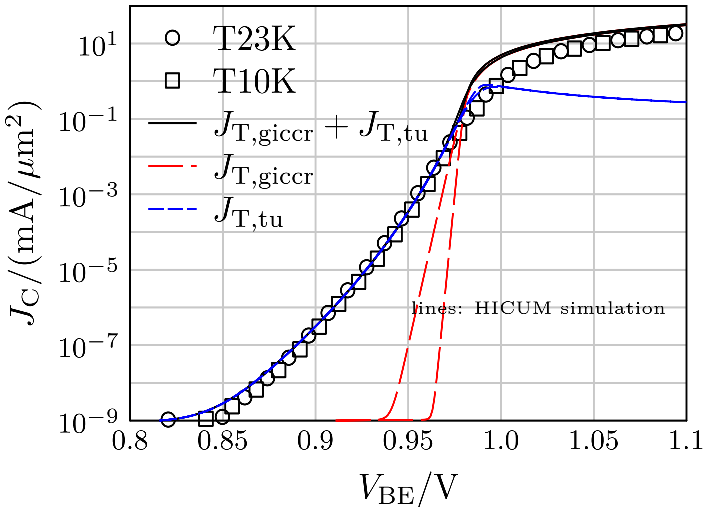
compact model equation

$$J_{\mathrm{Ttu}} = J_{\mathrm{TtuS}}\sqrt{v_{\mathrm{b}}}\exp(-a_{\mathrm{Ttu}}\sqrt{v_{\mathrm{b}}})\left[\exp\left(\left(\frac{v_{\mathrm{tuth}}(\Delta V_{\mathrm{E}})a_{\mathrm{Ttu}}}{\sqrt{v_{\mathrm{b}}}}\right)-1\right)\right],$$

Three model parameters required: J_{TtuS}, a_{Ttu} and ΔV_{E}, and vb is given by $v_{\mathrm{b}} = \frac{W_{\mathrm{b}}}{qV_{\mathrm{DEi}}} = 1 - \frac{V_{\mathrm{BE,intrinsic}}}{V_{\mathrm{DEi}}} = \left(\frac{C_{\mathrm{jEi}}}{C_{\mathrm{jEi0}}}\right)^{-\frac{1}{z_{Ei}}}$

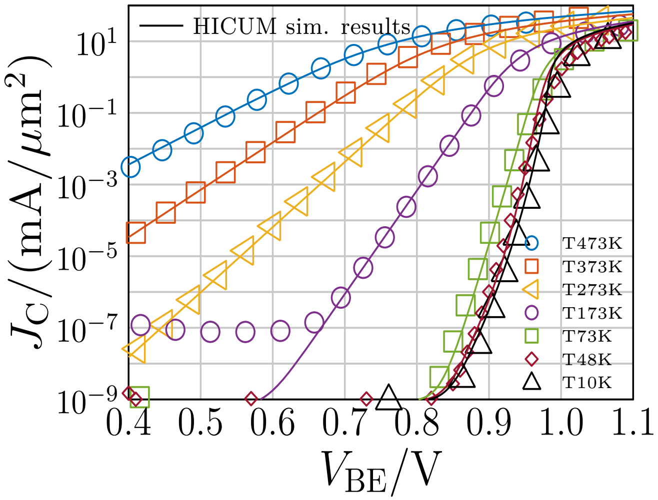
Comparison between compact model and measurements





- Lines:
  - Blue short dashed lines: only tunneling equation implemented;
  - Red long dashed lines: only GICCR equation implemented, only low current densities related parameters are considered here, such as qp0 and hjei;
  - Black solid lines: both tunneling and GICCR equations implemented.
- Left figure: only analytical equations are compared with the measurements.
- Right figure: equations are implemented in HICUM, and compact model simulation results are compared with measurements. High current effect and emitter resistance are considered.

Comparison between simulation and measurements



- With consideration of tunneling current, HICUM shows good agreement with measured values over a wide temperature range from 10 K to 473 K.
- Agreement shows strong physical background of HICUM.

Extraction tools: DMT and VerilogAE

DMT Introduction

- Modeling engineers rely on proprietary and difficult to extend tools, often use self-maintained scripts
  - Best practices, employed in the software industry for decades, often ignored (CI, automated testing, build systems, documentation)
  - Proprietary tools intrinsically difficult to extend and not freely available
- The issues inflicted by this practice include [12]:
  - Analysis/visualization/generation of data becomes difficult to reproduce;
  - Engineers work far from their maximum work-efficiency, as they are hindered instead of empowered, by their software infrastructure;
  - Knowledge built-up over decades may be lost when engineers leave a company or institution.

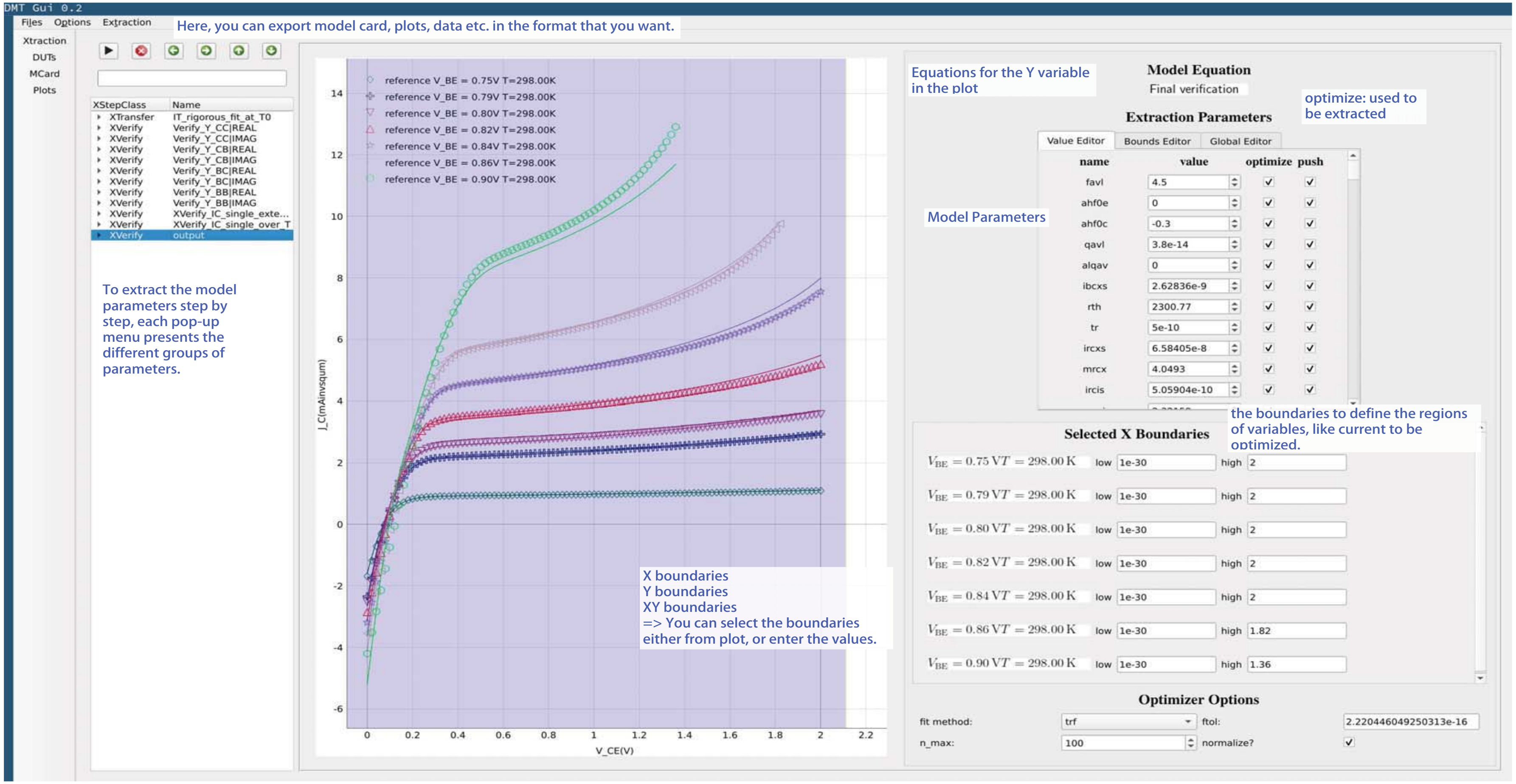
Features of DMT

- Device Modeling Toolkit (DMT) helps to solve these issues. DMT provides a Python library that offers [12]:
  - Classes and methods relevant to commonly used device engineering tasks
  - Abstract base classes for implementing interfaces to simulators; concrete implementations for open-source simulators Ngspice (Vogt, 2022), Xyce (Keiter et al., 2014) or Hdev (Müller et al., 2022) available
  - Bulk measurement data processing and reading routines
  - Handling of compact models and modelcards
- Git-project: https://gitlab.com/dmt-development/dmt-core
- Employs best practices principles used in the software industry:
  - Continuous integration (CI), including automated testing
  - Extensive documentation in code and also on separate website: https://dmt-development.gitlab.io/dmt-core/installation/install_dmt.html
- Interfaces to proprietary simulators and par. extraction GUI **not open-source at this time**, available for partners upon request

OpenVAF and VerilogAE

- VerilogAE provides a Python interface for Verilog A source files [13]:
  - Evaluate model equations
  - Analyze structure of model equations
  - Generate derivatives of model equations
  - Modelcard generation
- VerilogAE uses OpenVAF as back-end for Verilog-A compilation:
  - Directly generates executable machine code
  - Ultra fast compilation without the need for another compiler (gcc)
  - Implements the language standard in a clear and unified wayH
  - Has great ux (error messages)
  - GPL license, commercial partners can request commercial license, software integration services into circuit simulators and support from SemiMod
  - Very likely **the most advanced** Verilog-A compiler available today
- *All* CMC models can be compiled, currently being implemented it into Ngspice (release planed for end of 2022)
- Git project: https://man.sr.ht/~dspom/openvaf_doc/verilogae/

GUI of DMT



Here, you can export model card, plots, data etc. in the format that you want.

XStepClass	Name
XTransfer	IT_rigorous_fit_at_T0
XVerify	Verify_Y_CC|REAL
XVerify	Verify_Y_CC|IMAG
XVerify	Verify_Y_CB|REAL
XVerify	Verify_Y_CB|IMAG
XVerify	Verify_Y_BC|REAL
XVerify	Verify_Y_BC|IMAG
XVerify	Verify_Y_BB|REAL
XVerify	Verify_Y_BB|IMAG
XVerify	XVerify_IC_single_exte...
XVerify	XVerify_IC_single_over_T
XVerify	output

To extract the model parameters step by step, each pop-up menu presents the different groups of parameters.

X boundaries
Y boundaries
XY boundaries
=> You can select the boundaries either from plot, or enter the values.

Equations for the Y variable in the plot

Model Equation

Final verification

optimize: used to be extracted

Extraction Parameters

Model Parameters

name	value	optimize	push
favl	4.5	☑	☑
ahf0e	0	☑	☑
ahf0c	-0.3	☑	☑
qavl	3.8e-14	☑	☑
alqav	0	☑	☑
ibcxs	2.62836e-9	☑	☑
rth	2300.77	☑	☑
tr	5e-10	☑	☑
ircxs	6.58405e-8	☑	☑
mrcx	4.0493	☑	☑
ircis	5.05904e-10	☑	☑

the boundaries to define the regions of variables, like current to be optimized.

Selected X Boundaries

	low	high
$V_{BE} = 0.75\,V T = 298.00\,K$	1e-30	2
$V_{BE} = 0.79\,V T = 298.00\,K$	1e-30	2
$V_{BE} = 0.80\,V T = 298.00\,K$	1e-30	2
$V_{BE} = 0.82\,V T = 298.00\,K$	1e-30	2
$V_{BE} = 0.84\,V T = 298.00\,K$	1e-30	2
$V_{BE} = 0.86\,V T = 298.00\,K$	1e-30	1.82
$V_{BE} = 0.90\,V T = 298.00\,K$	1e-30	1.36

Optimizer Options

fit method: trf
ftol: 2.220446049250313e-16
n_max: 100
normalize? ☑

Conclusions

- Existing foundry PDK models unsuitable for cryogenic operation
- Standard HBT models need to be extended:
  - Capturing low-temperature physics
  - Mathematical conditioning of new formulations
  - Additional model parameters require parameter extraction (and extended methods)
- Physical-based compact formulation of tunneling current has been derived
  - Model verification on (preferably) a variety of HBT process technologies needs to be done
  - Requires (regular) cryogenic measurements at foundries!

⇒ clear direction for model development, but lot of work still ahead
first version of cryogenic HICUM/L2 has been delivered to foundries for cryogenic design applications

- DMT and VerilogAE have been used for parameter extraction.
  - Very efficient tools for parameter extraction
  - Extraction steps for various technologies have been implemented and applied:
    - **SiGe HBTs, III-V HBTs, FD SOI FETs** and passives
    - HEMTs and others FETs will be developed upon request
  - **Already applied to commercial processes technologies from Globalfoundries, Infineon**

Acknowledgments

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DFG SCHR695/14:
“Modeling of non-linear large-signal dynamic effects in SiGe heterojunction bipolar transistors”

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Thanks for your attention!

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