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On the performance of Hall cells integrated in a non-fully depleted SOI CMOS technological process. An overview

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OUTLINE

- Different Hall cells have been integrated in both regular bulk (XFAB CMOS XH 0.35 μm) and SOI CMOS technologies and analyzed in terms of their specific parameters.

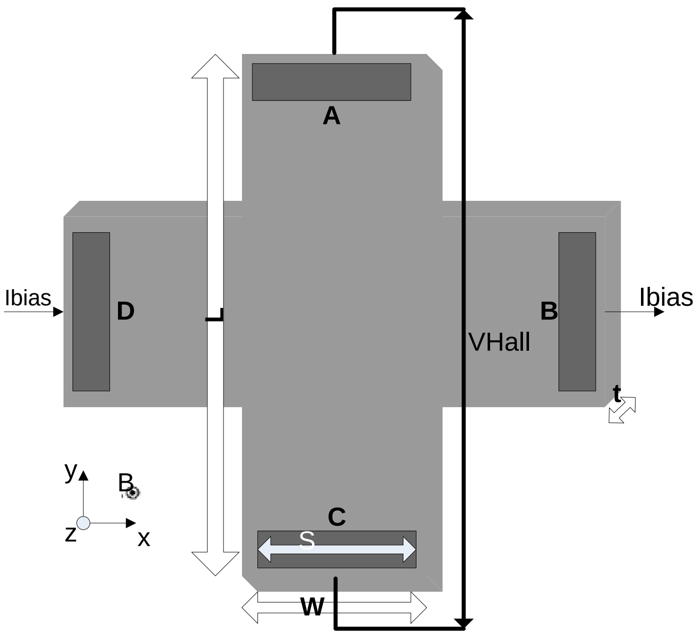
- This work offers an overview on Hall cells performance integrated in SOI technological process, i.e. XFAB SOI XI10 1 μm non-fully depleted.

- Geometry plays an important role in Hall cells performance. The focus of this study is on the Optimum Hall cell.

- The most important parameters of a specific Hall cell, based on SOI structure, are evaluated through three-dimensional physical simulations.

- Experimental results are also provided.

Hall Effect Sensors



(1) $$V_{HALL} = S_A B$$

(2) $$S_A = \frac{Gr_H}{nqt} I_{bias}$$

- low-power applications
- current sensing
- position detection & contactless switching

Hall Cells Design Selection

- Different 3D Hall sensors were integrated in both regular bulk and SOI CMOS.
- They are all symmetrical and orthogonal structures.
- The geometry plays an important role in the sensors performance.

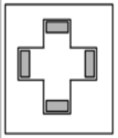
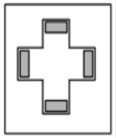
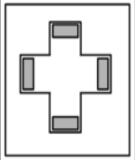
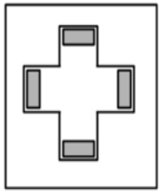
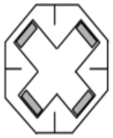
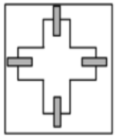
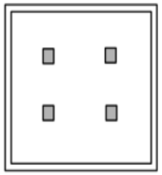
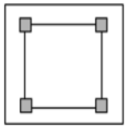
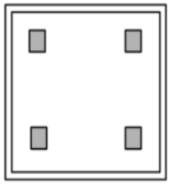
$$G \cong 1 - \frac{16}{\pi^2} \exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\left[1 - \frac{8}{9}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\right]\left(1 - \frac{\theta_H^2}{3}\right) \quad (3)$$

valid if $0.85 \leq L/W < \infty$ and $0 \leq \theta_H \leq 0.45$

Hall Effect Sensors Measurements

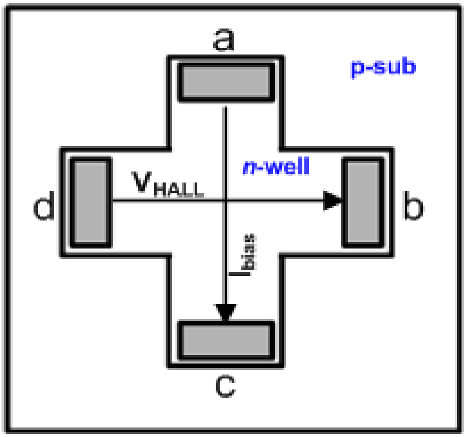
- Measurements results on nine different Hall Effect sensors in regular bulk CMOS
- Similar results expected soon for the SOI counterparts

Objectives: offset @ T=300 K **< ±30 μT** & *offset drift* < ±**0.3 μT/°C**

Geometry Type	*Basic*	*Low-doped*	*L*	*XL*	*45 Deg*	*Narrow Contacts*	*Borderless*	*Square*	*Optimum*
Integrated Shape (CMOS 0.35 μm)									
R_0(kΩ) @ T=300 K, B=0 T	2.3	5.6	2.2	2.2	2.1	2.5	1.3	4.9	1.5
S_A (V/T) @ I_{bias}=1 mA	0.0807	0.3392	0.0804	0.0806	0.0807	0.0822	0.0325	0.0884	0.0635
Offset drift (μT/°C) (4-phase current spinning)	0.409	0.067	0.264	0.039	0.373	0.344	0.526	0.082	0.328
L, W (μm) of the Active Area (N-well)	L=21.6	L=21.6	L=32.4	L=43.2	L=21.64	L=21.6	L=50	L=20	L=54
	W=11.8	W=11.8	W=17.8	W=22.6	W=11.8	W=9.5	W=50	W=20	W=54
L/W	1.83	1.83	1.82	1.91	1.83	2.27	1	1	1
s (μm) for Sensing Contacts	11	11	16	20.7	11	1.5	2.3	2.3	5.4
Geometrical Correction Factor (G)	0.913	0.913	0.912	0.924	0.913	0.87	0.76	0.73	0.74

Single Phase and Residual Offset

- Cell polarization and the corresponding phases



Greek-cross cell polarization

Phases	Ibias	V_{HALL}
Phase 1	a to c	b to d
Phase 2	d to b	a to c
Phase 3	c to a	d to b
Phase 4	b to d	c to a

- Single phase offset and residual offset

$$V_{out} = V_{HALL}(B) + V_{offset} \quad (4)$$

$$Offset_{residual\ (4\ phase)} = \frac{V_{P1} - V_{P2} + V_{P3} - V_{P4}}{4} \quad (5)$$

Regular bulk vs. SOI CMOS technology

The sensors fabricated in SOI (***S***ilicon ***O***n ***I***nsulator) technology have obvious benefits, with respect to the bulk Hall sensors.

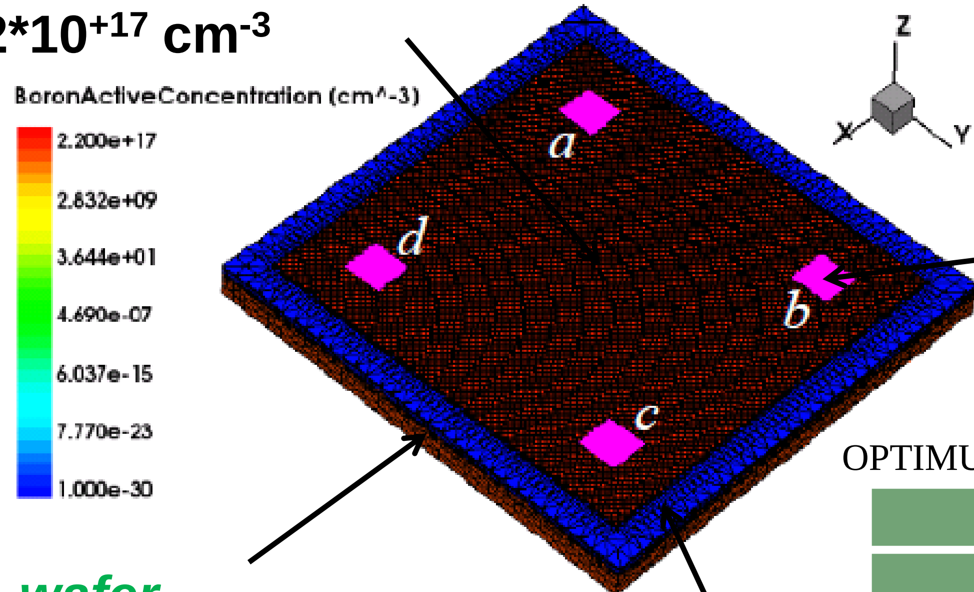
- higher magnetic sensitivity
- less noise generation
- possibility to use lower biasing voltage
- smaller leakage current through the dielectric
- enhanced radiation resistance etc.

The 3D Simulation of SOI Hall Cells

➢**The structure follows the SOI XFAB XI10 fabrication process.**

➢***active p-well region:*** **Boron doping**

- ✓ **Uniform profile implantation**
- ✓ **$2.2*10^{+17}$ cm^{-3}**



➢***electrical contacts***

➢***Handle wafer***

➢***p-substrate:*** **Boron doping**

- ✓ **Uniform profile implantation**
- ✓ **$6.5*10^{+14}$ cm^{-3}**

➢***SiO_2***

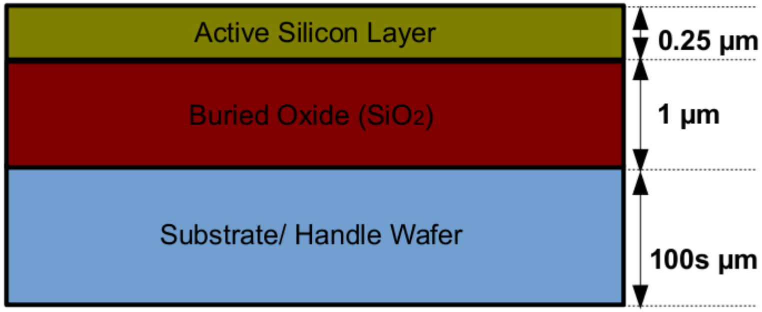
OPTIMUM HALL CELL DESIGN FEATURES

Parameter	Value
L (μm)	50
W (μm)	50
Contacts dimension s (μm)	4.7

The 3D model of SOI Optimum Hall cell

SOI CMOS technology

➢ The stacking of the layers, according to a SOI XFAB XI10 fabrication process.



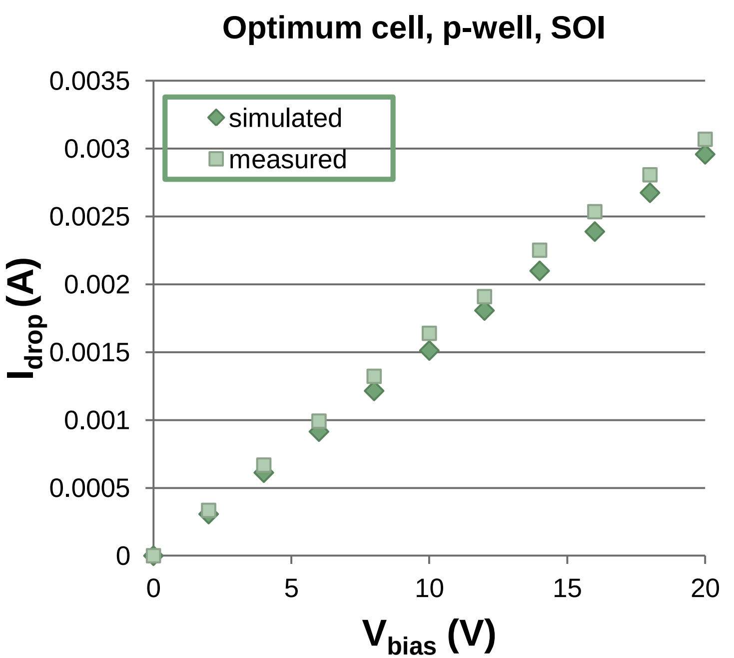
➢The active silicon layer is found on top of the dielectric buried silicon oxide (SiO_2) layer, which is in its turn found on the silicon substrate, or handle wafer.

DOPING CONCENTRATIONS IN THE SOI HALL CELL FABRICATION

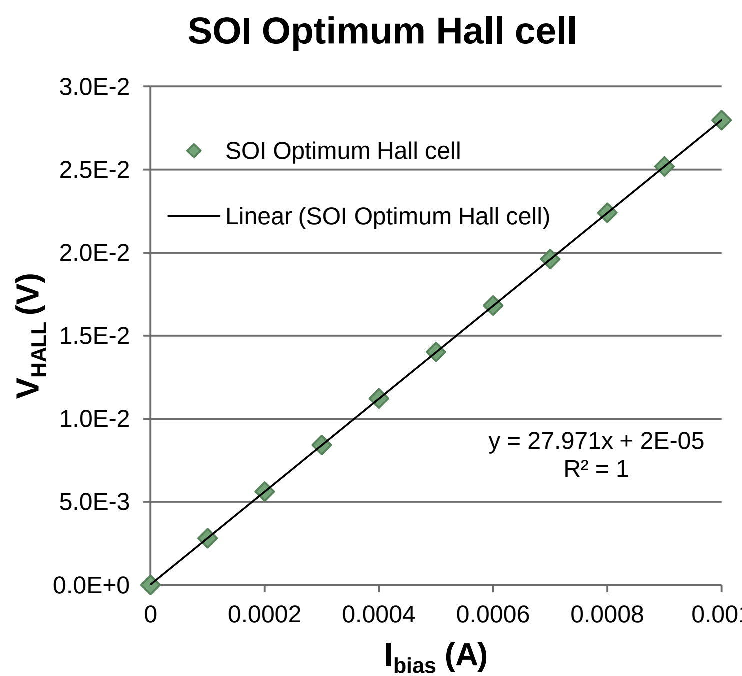
Layer	Type	Numerical value
Wafer (handle) substrate	Si, p-doped (Boron)	6.5 E+14 cm^{-3}
Dielectric	Buried Silicon Oxide, $Si0_2$	
p-substrate in active Silicon layer	Si, p-doped (Boron)	1E+15 cm^{-3}
n-well in active Silicon layer	Si, n-doped (Arsenic)	5E+16 cm^{-3}

3D Simulations results (I)

- **I-V characteristics**
- **V_{HALL} estimation**



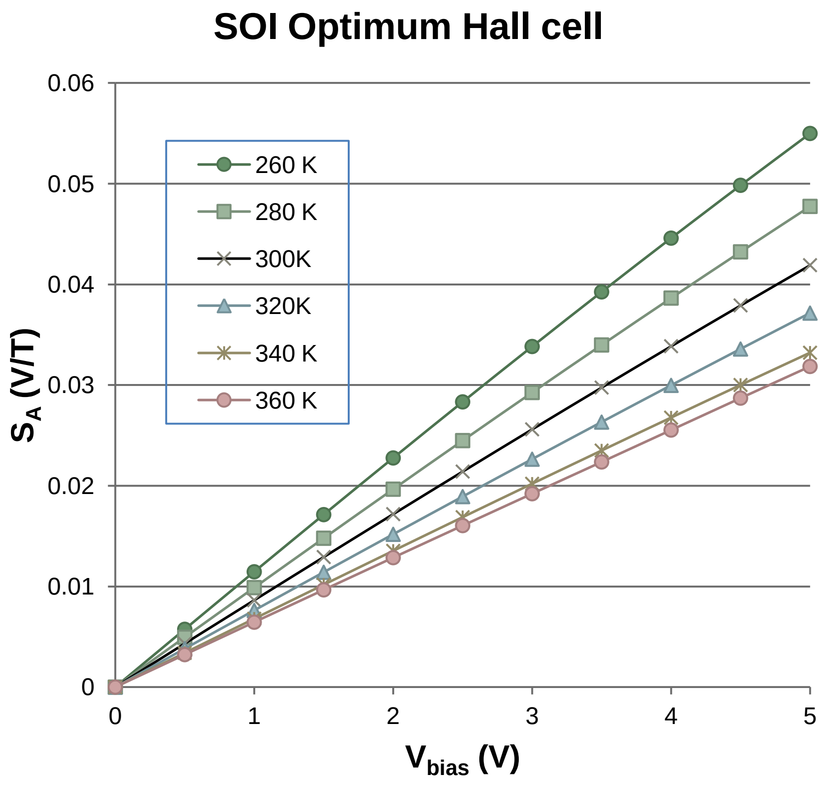
V-I characteristics of the SOI Optimum Hall cell



Hall voltage vs. biasing current for the SOI Optimum Hall cell

3D Simulations results (II)

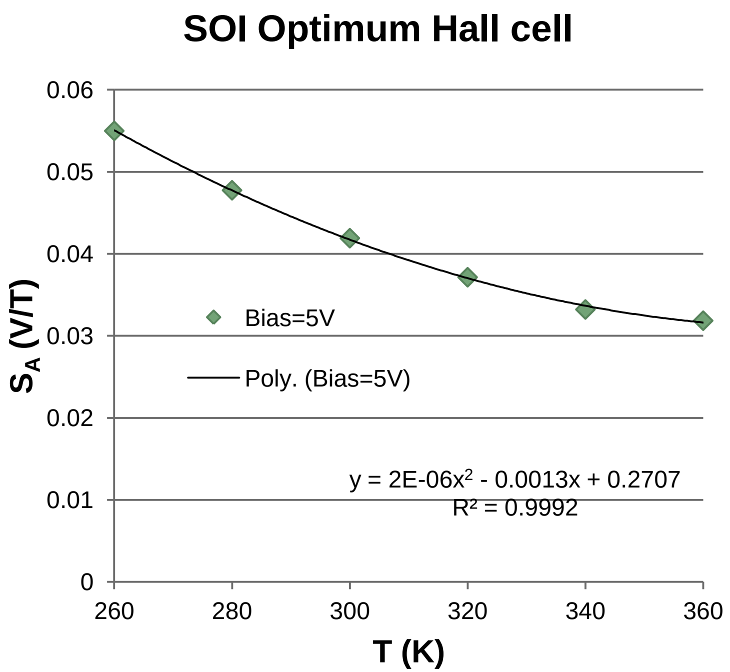
- **Sensitivity numerical estimation**
- **Temperature effects**



Simulated absolute sensitivity *vs.* V_{bias}, for different temperatures, for the SOI Optimum Hall cell

3D Simulations results (III)

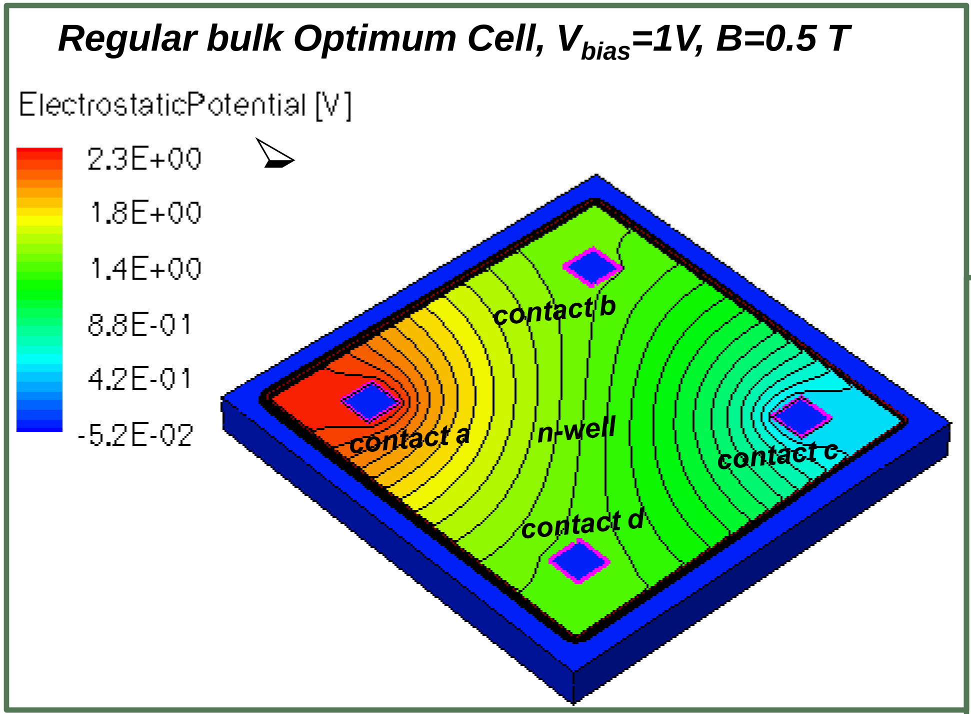
- **Sensitivity numerical estimation**
- **Temperature effects**
- **Investigation on the quadratic effect of S_A with temperature**

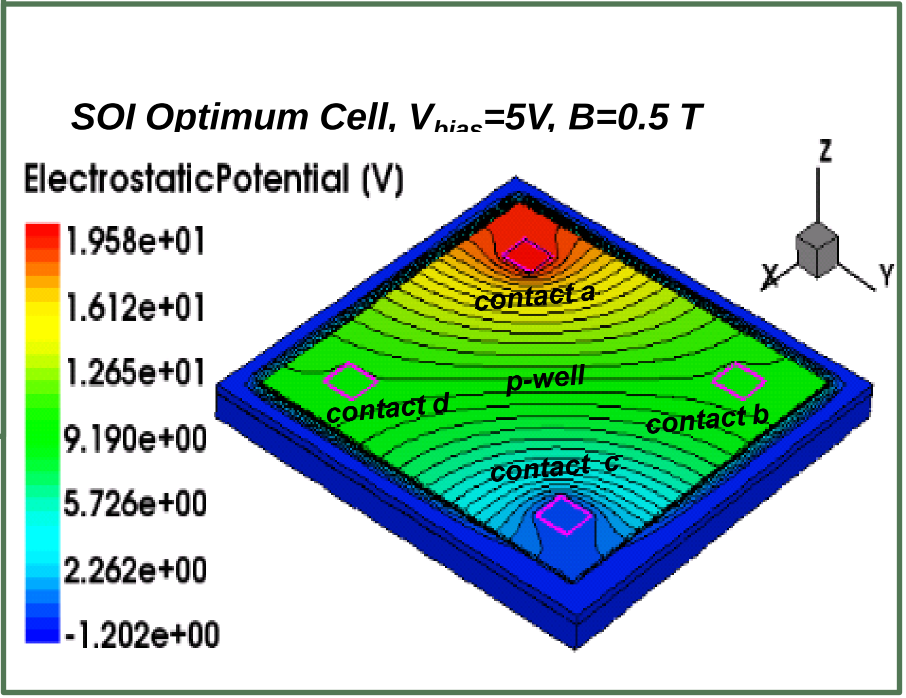


Simulated absolute sensitivity *vs.* V_{bias}, for different temperatures, for the SOI Optimum Hall cell

3D Simulations results (IV)

- The simulated Optimum Hall cell (bulk vs. SOI CMOS)
- Electrostatic potential distribution





3D Simulations results (V)

- Summary of the SOI Optimum Hall cell performance
- B=0.5 T and T=300 K
- SOI Optimum Hall cell in SOI technology provided for B=0.5 T, S_A=41 mV/T for V_{bias}= 5 V

CMOS SOI OPTIMUM HALL CELL PERFORMANCE SUMMARY

Parameters	**R_{input} (kΩ)**	**V_{HALL} (V), I_{bias}=1 mA**	**S_A (V/T), V_{bias}=5 V**
Values	6.47	2.8E-2	41E-3

Conclusions

- This work was intended to analyze the behaviour of the Optimum Hall cell in SOI CMOS fabrication process.
- A three-dimensional model of the SOI Optimum Hall cell, with p-well, was constructed.
- The Hall voltage, sensitivity, input resistance and electrostatic potential distribution were extracted through simulations.
- The temperature variation of the absolute sensitivity is also investigated for the considered Hall cell.

Experimental results are as well provided.

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[4] **Paun, M.A.,** Sallese, J.M., Kayal, M., "*Comparative Study on the Performance of Five Different Hall Effect Devices",* Sensors, ISSN 1424-8220, Vol. **13,** Issue 2, 2013, pp. 2093-2112.

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Thank you for your kind attention!