AUTOMICS: Pragmatic solution for parasitic-immune design of electronics ICs for automotive

Ehrenfried Seebacher
ams AG

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Outline

- Smart Power ICs in Automotive Applications.
- AUTOMICS Consortium
- Problem Definition
- Proposed Modeling Approach
- Preliminary Results

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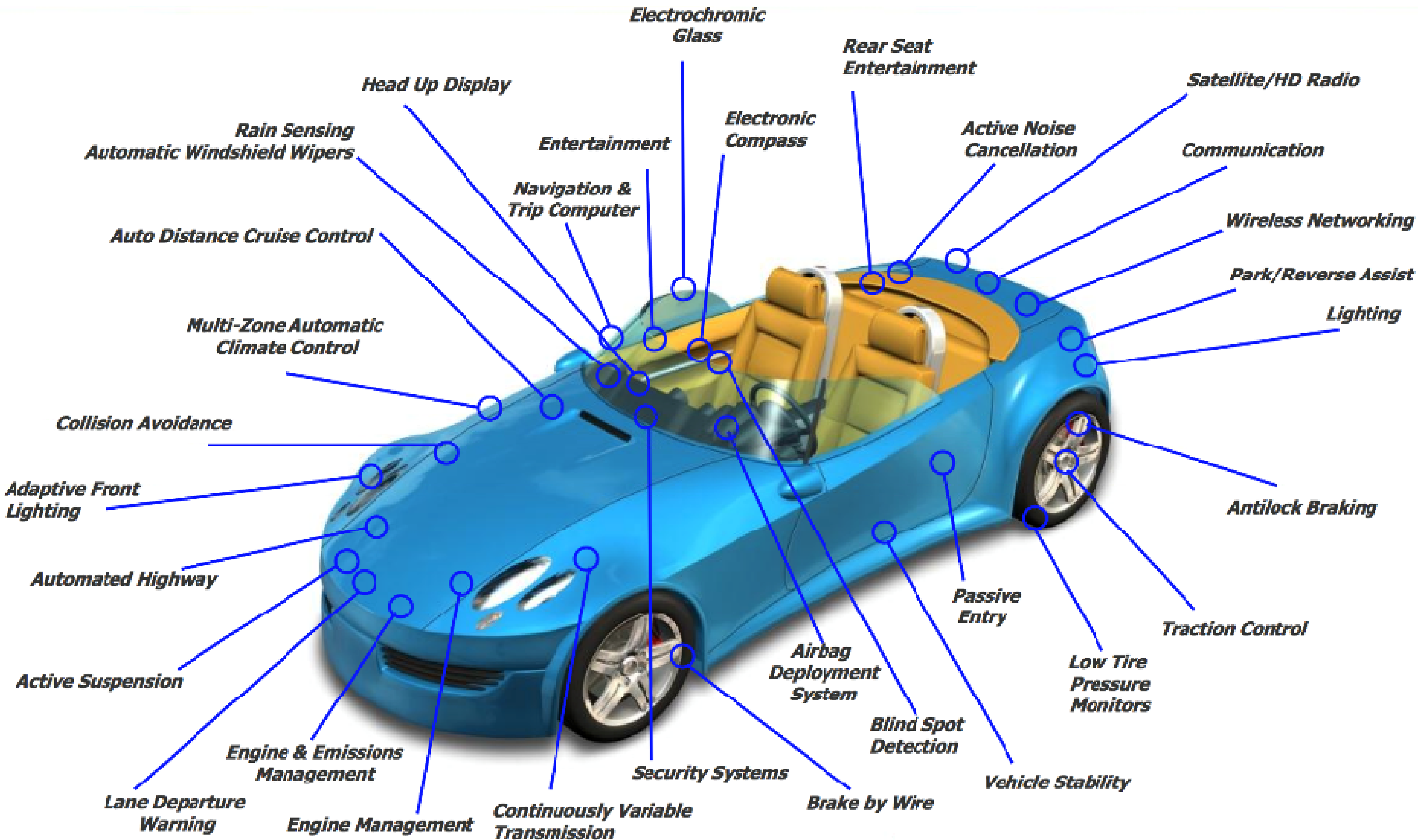
Smart Power ICs in Automotive Applications



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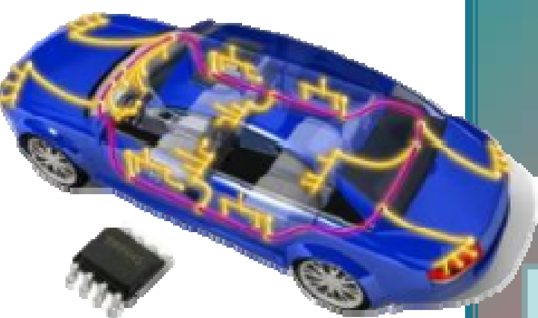
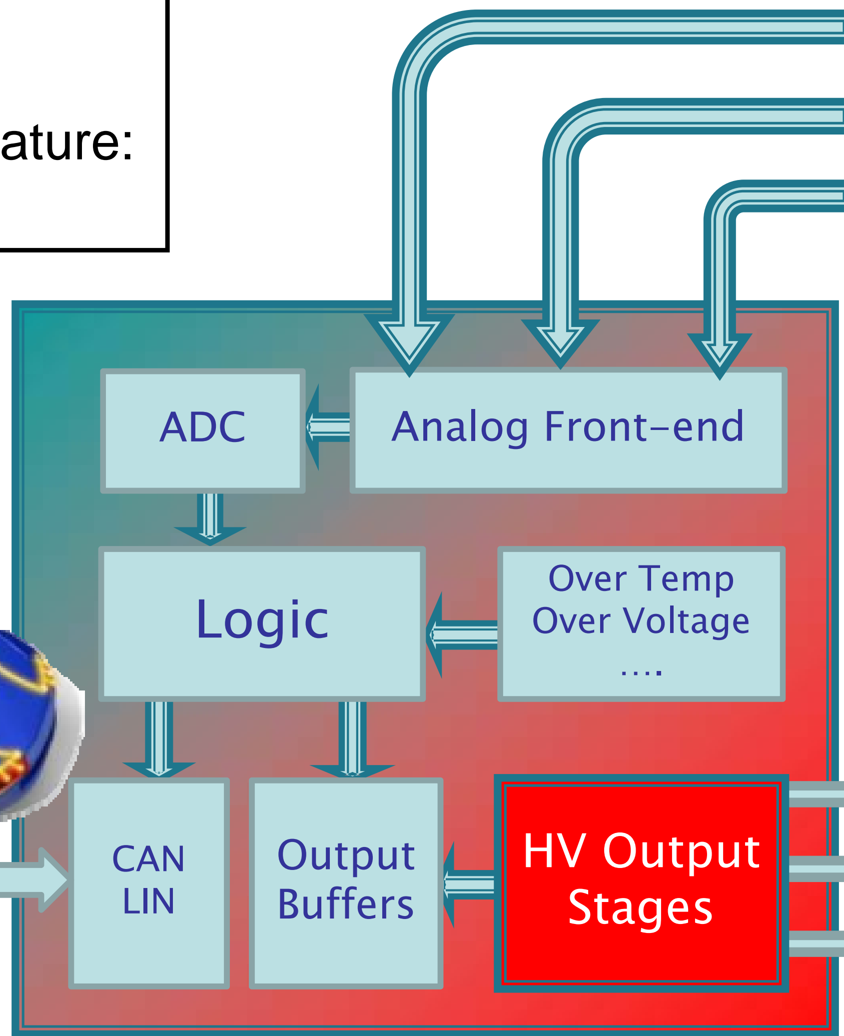
Block diagram of Smart Power ICs

Operating Voltage:
5 V to 400 V

Operating Temperature:
-40ºC to 180ºC





Typical Input:

- Torque
- Pressure
- Acceleration
- Speed
- Temperature

Typical Load:

- Motors (500mA-4A)
- Relays (50-200mA)
- Injector Coils (1A)
- Signaling (50-500mA)

Challenge

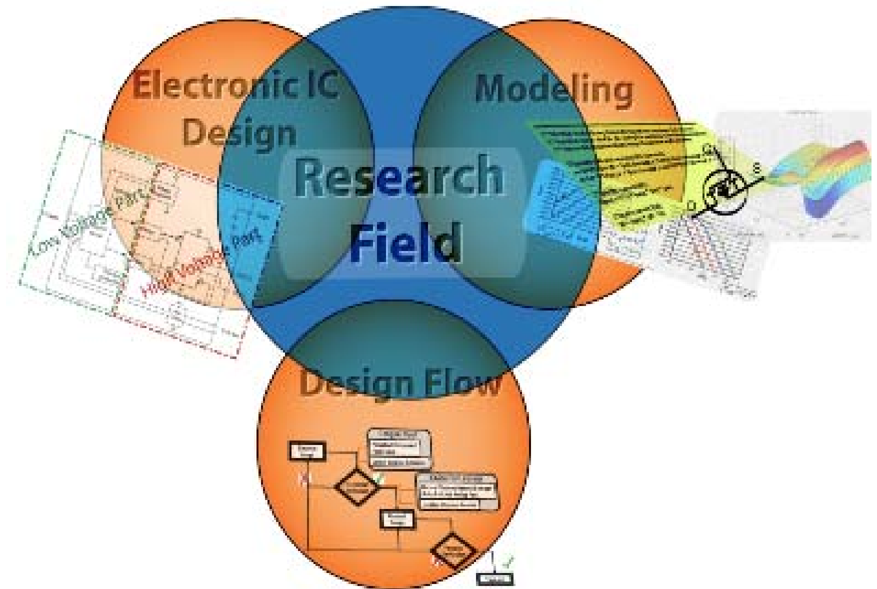
Substrate coupling through minority carrier injection due to switching of power stages.

AUTOMICS Objectives

- **AUTOMICS** stands for Automotive Integrated Circuits.

- AUTOMICS addresses the problem of safety, security, reliability and durability of FEV (Fully Electrical Vehicles)

- AUTOMICS objectives are:
  - Model the minority carriers injection in smart power ICs.
  - Predict the minority carrier injection effect on the Low and high voltage circuits integrated on the same Chip.
  - Develop a CAD tool to predict the minority carriers parasitic effects before fabrication
  - Investigate ESD Phenomena
  - Propose circuit protection to immune smart power integrated circuits.



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AUTOMICS Consortium

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STREP Project
EU Fund : 3.47M€
Started July 2012

Academic

Université Pierre et Marie Curie
UPMC, France
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Automotive Industry

Valeo Electrical Systems
VALEO, France

Continental Automotive France SAS
CONTI, France

EDA Industry

AdMOS Gmbh Advanced Modeling Solutions
ADMOS, Germany

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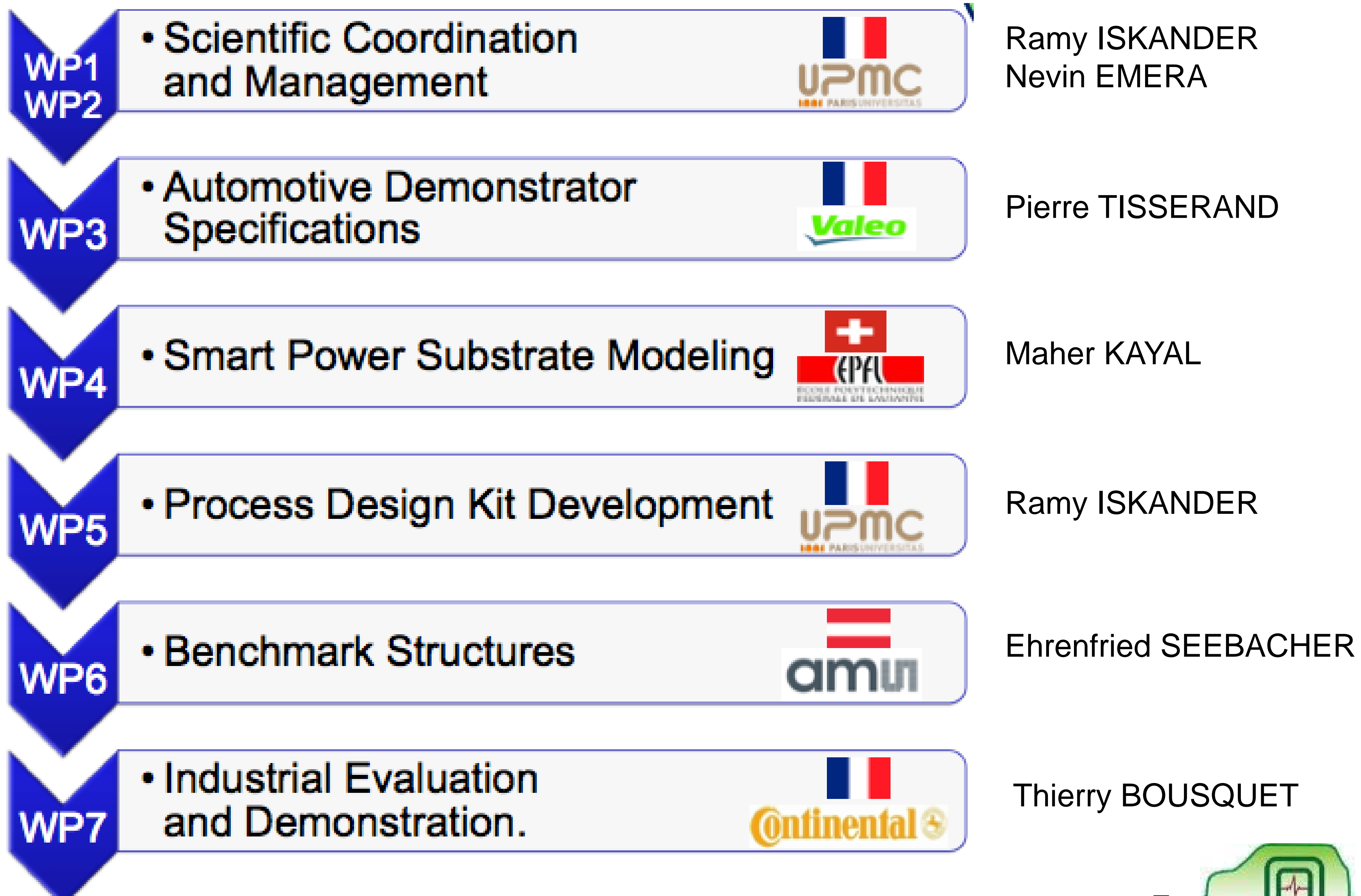
AUTOMICS Work-Packages



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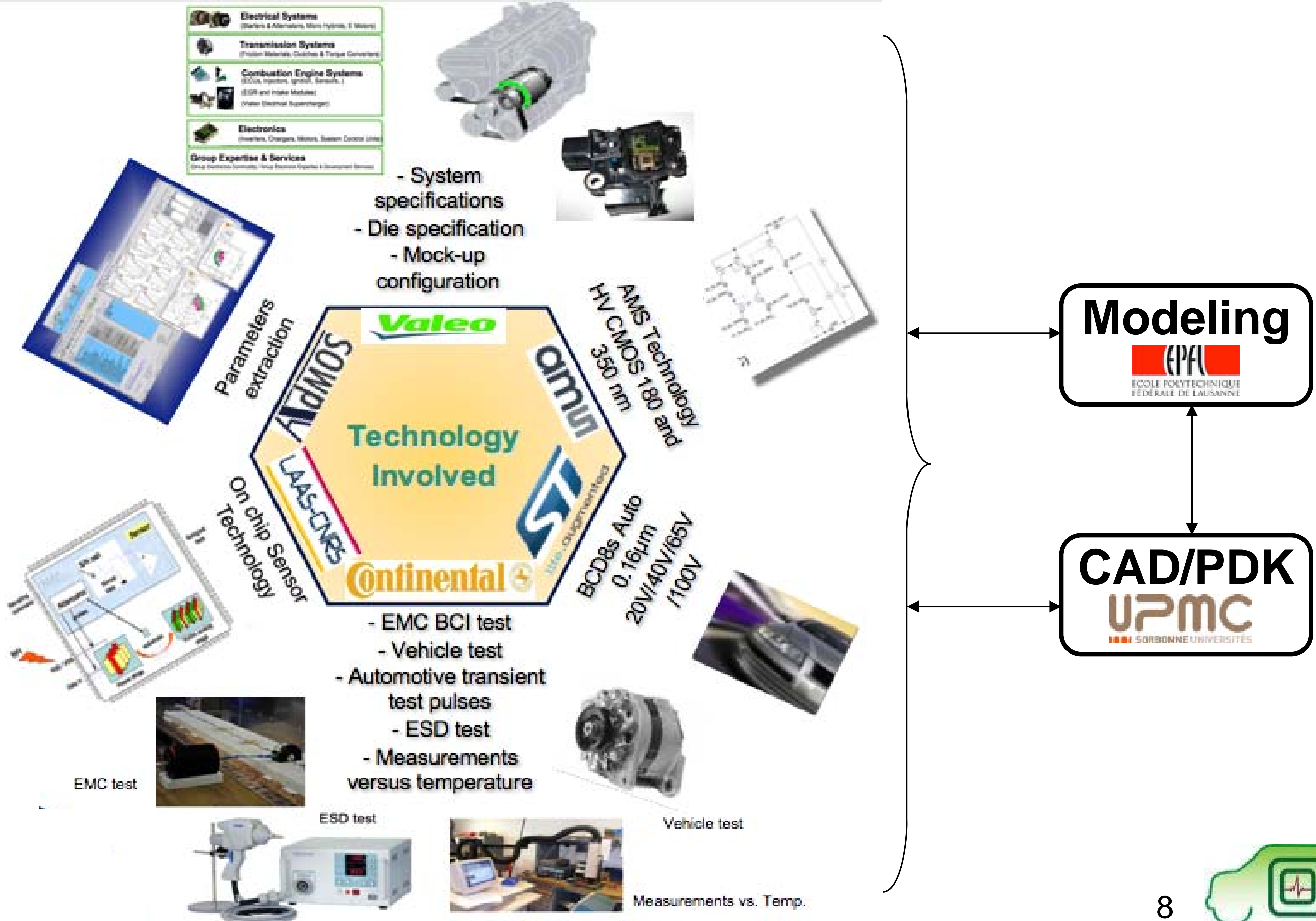
Responsibilities Per Partner



Modeling

EPFL ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

CAD/PDK

UPMC SORBONNE UNIVERSITÉS

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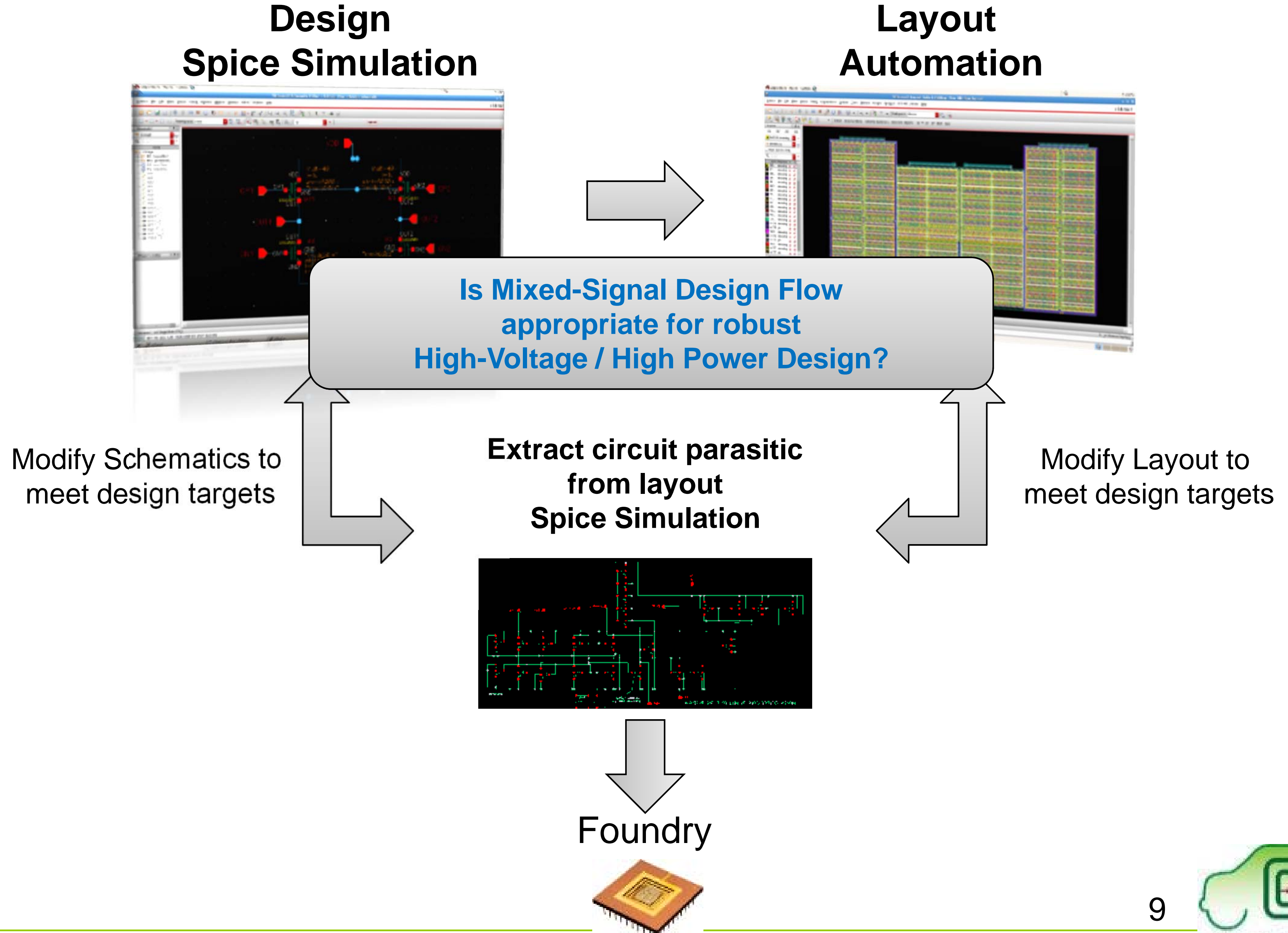
Problem Definition



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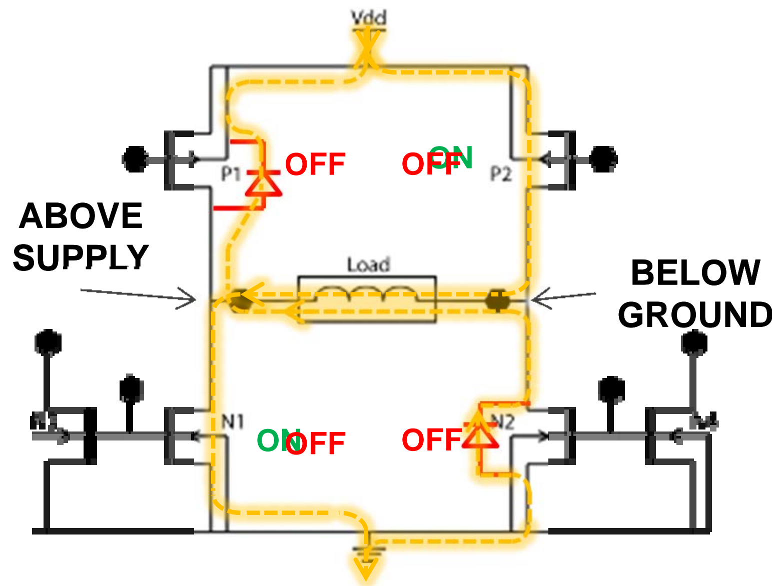
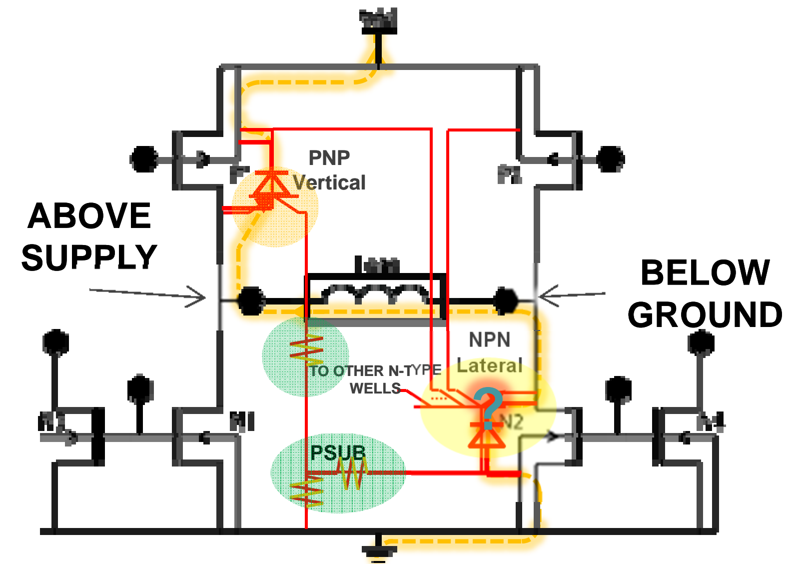
Problem Definition: HV-Bridge Circuit





An H-Bridge allows the control of current on both directions through an inductive load such as a motor.

When the H-Bridge is disabled or when the opposing voltage polarity is applied, the current flows through **the free-wheeling** diodes.

In **free wheeling** condition:

- High side **PNP current injection**
  - Voltage shift of the substrate
  - Low voltage transistor bulk modulation
  - Capacitive injection in sensitive circuit
- Low side **NPN current extraction**
  - Trigger a latch-up

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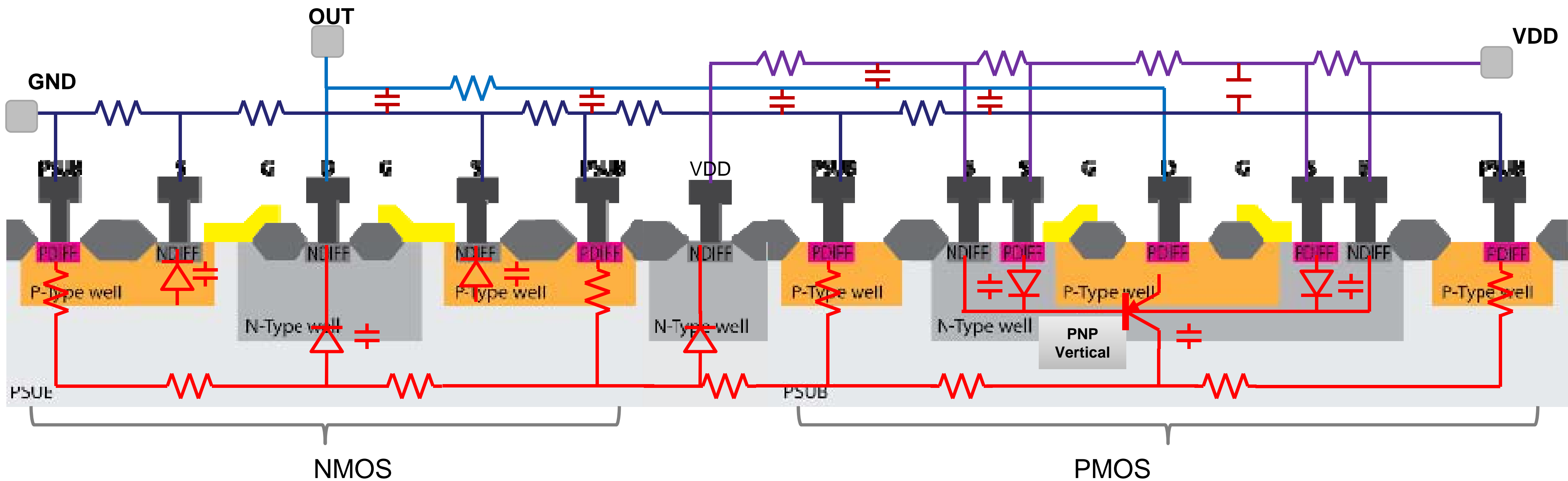
Problem Definition: Parasitic Extraction



Parasitic extraction is mandatory to analyze parasitic effects

Parasitics extracted for the **interconnect**

- Interconnect parasitic extraction is a must for Crosstalk and Power Analysis.

Parasitics extracted for the **substrate**

- Substrate is modeled by a RC-network taking into account **only** majority carriers.
- Analysis of RF IC circuits.

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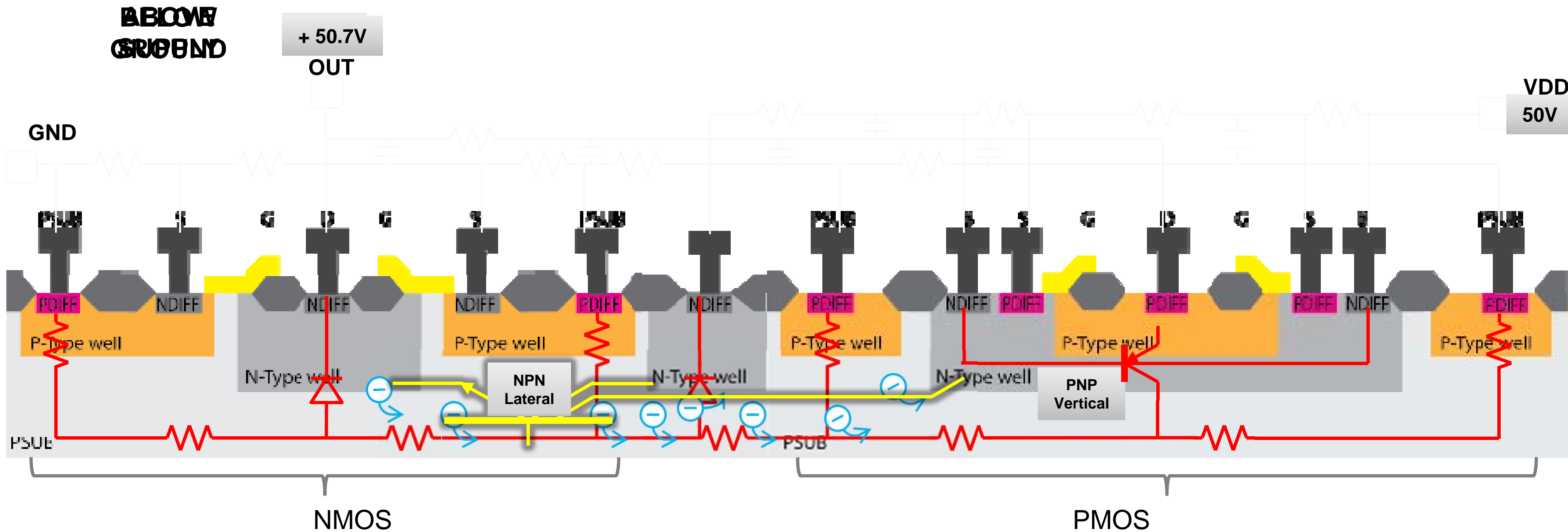
Problem Definition: Substrate Extracted Circuit



Substrate currents injected by parasitic **vertical PNPs** can be significant

- Potential shift in the whole substrate of several mV

Forward biased N-Type wells inject electrons in the substrate

- Minority carriers diffusion in the substrate can affect circuit performance or trigger a latch-up

Other N-Type wells collect these electrons

- **Lateral NPNs** can disturb circuits functionality

Electrical circuit simulator neglects minority carriers!

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Problem Definition: Device Splitting to Diodes

- Detect **multi-junction** parasitic current paths
- Eventual bipolar transistors **automatically** detected
- Parasitic network schematics after **layout**
- We have to take into account the **minority** carriers' propagation in the substrate

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Model Development

F. L. Conte, J.-M. Sallese, M. Pastre, F. Krummenacher and M. Kayal,
"A circuit-level substrate current model for smart-power ICs,"
Power Electronics, IEEE Transactions on, vol. 25, pp. 2433--2439, 2010

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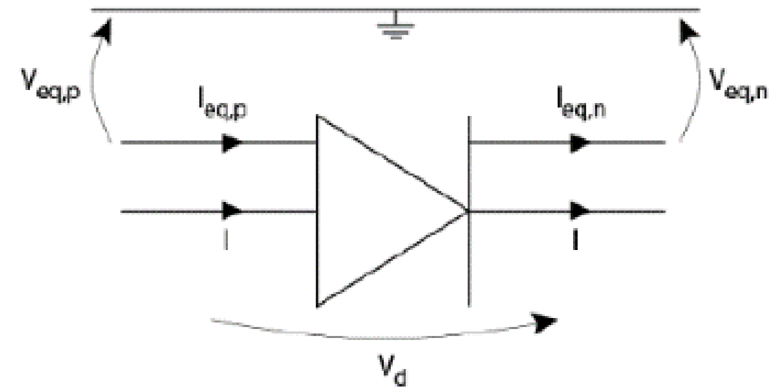
EPFL Substrate Model

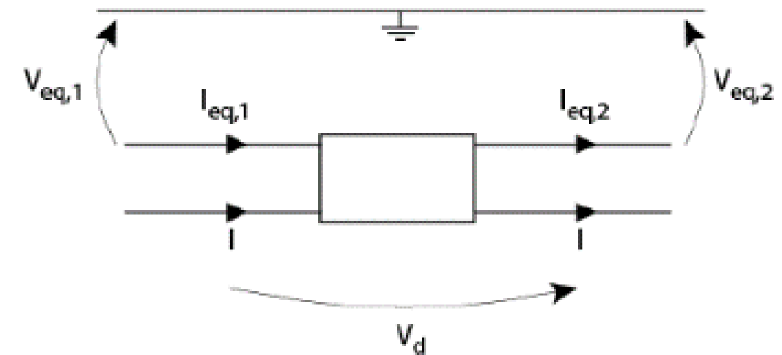
- **Physics** based model based on 1D drift-diffusion equation (**verilog-A**)
- 4-terminal devices: majority and **minority** carriers.
- Equivalent currents and voltages for minority carriers can be simulated at **circuit level**.
- Parasitic network extraction with a substrate **meshing** strategy.

Only diodes and resistors can simulate transistor effect!

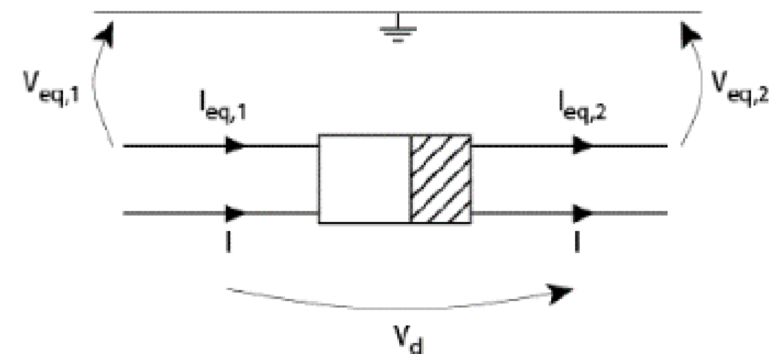
EPFL diode



EPFL resistance



EPFL contact



Model under validation in AMS HV 0.35 µm and ST BCD 0.18 µm technologies

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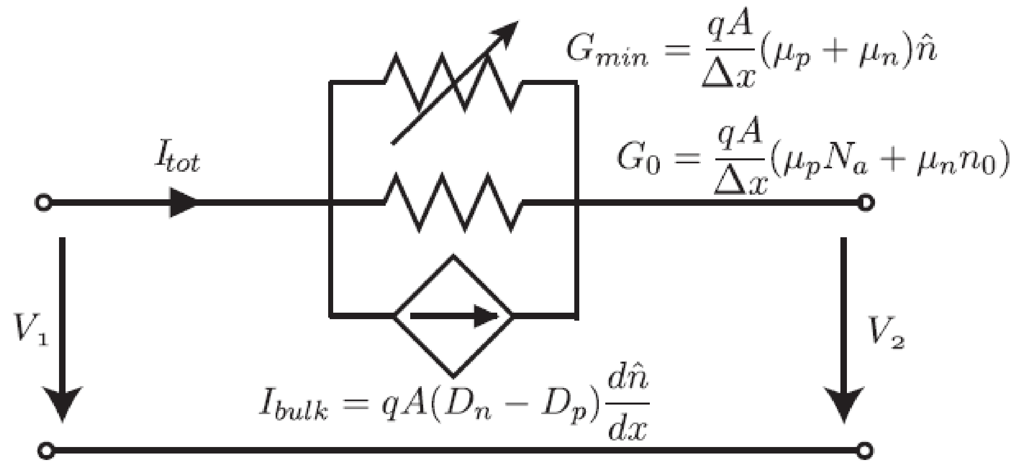
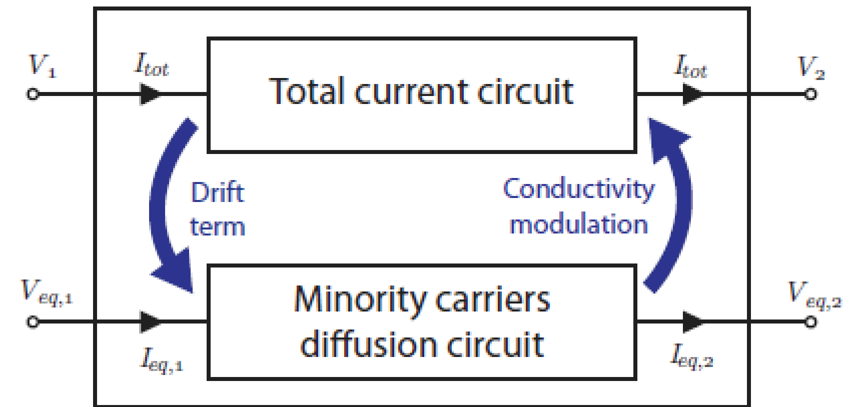
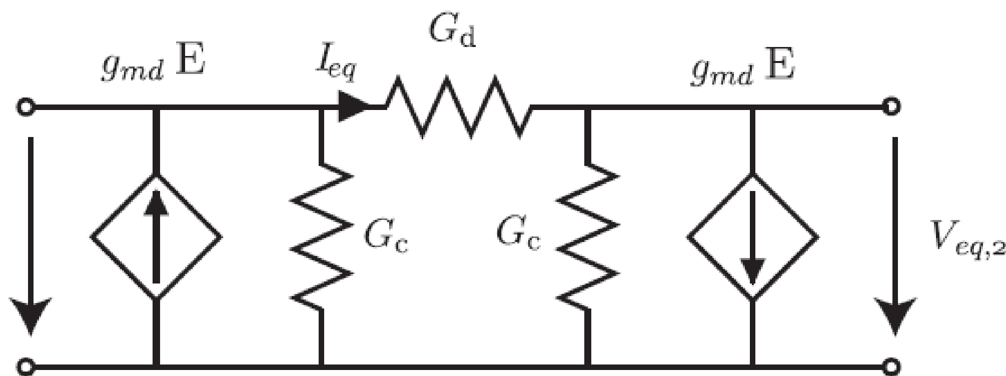
Model equivalent circuits







$$G_d = \frac{AD_n}{\Delta x} \quad G_c = \frac{A\Delta x}{2\tau_n} \quad g_{md} = A\mu_n \frac{V_{eq,1} + V_{eq,2}}{2}$$

- **TCC** (Total Current Circuit) and **MCC** (Minority Carrier Circuit) highly coupled to model substrate conductivity modulation
- Geometrical and technology (doping, lifetime…) input parameters for the model.

[3] C. Stefanucci et al., Solid State Electronics, 105, 21-19,2014
[4] P. Buccella et al., MIXDES, 2014

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Model Calibration

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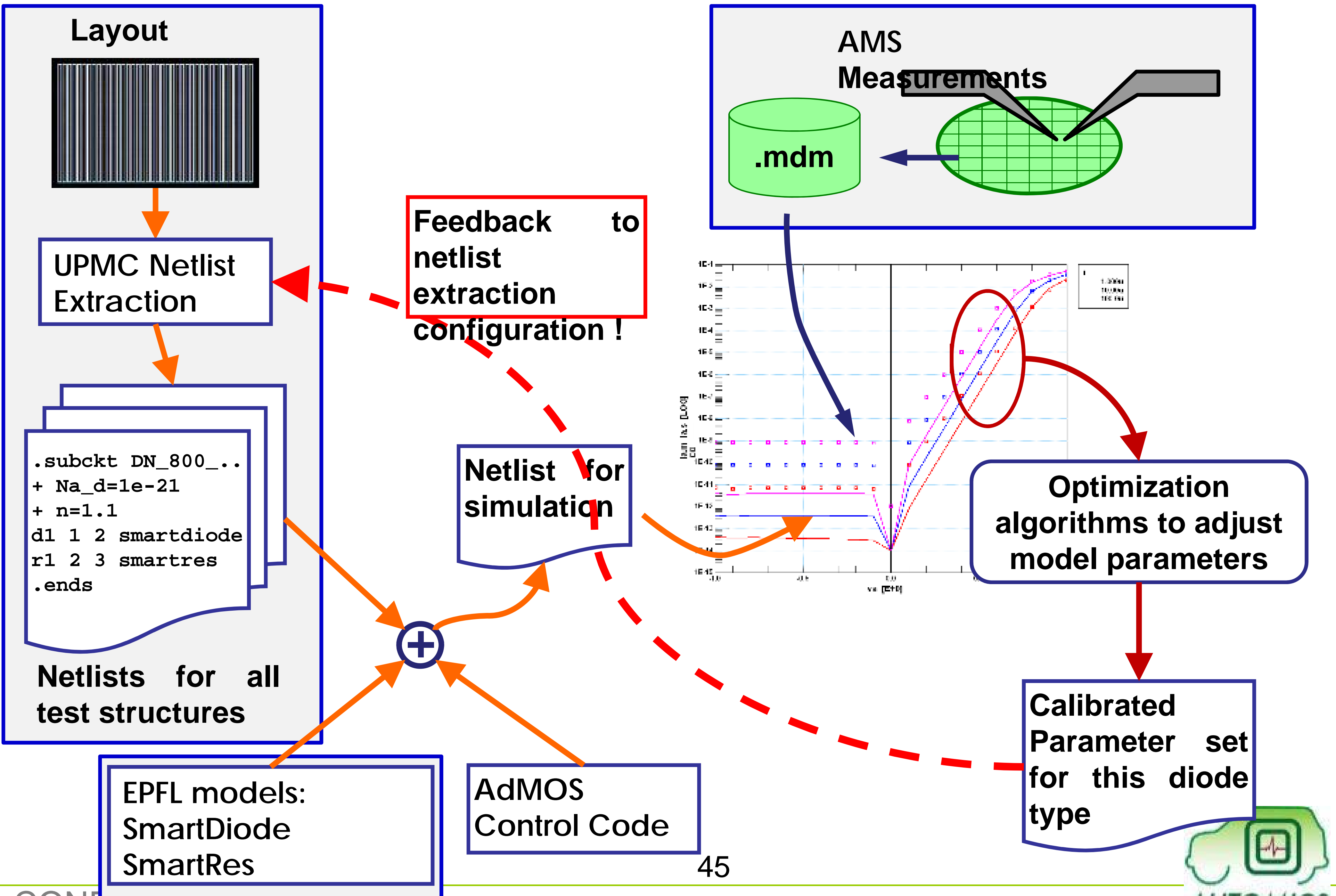
Principle flow of calibration



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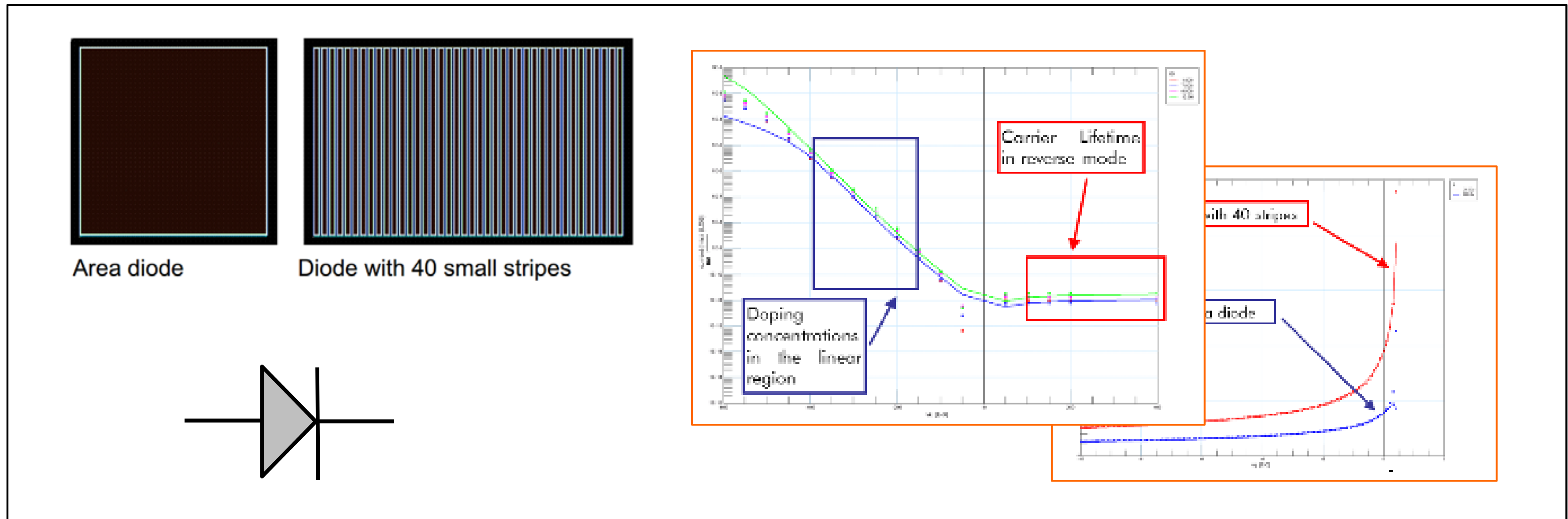
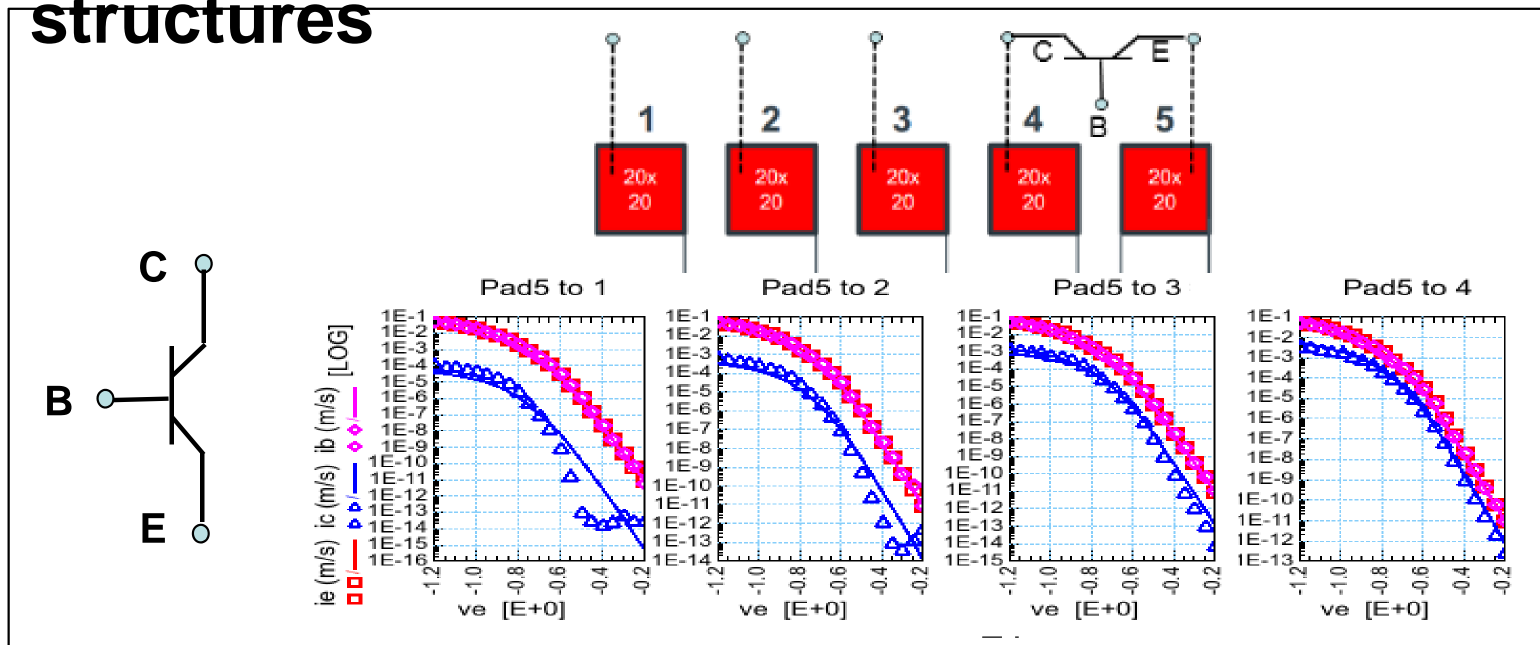
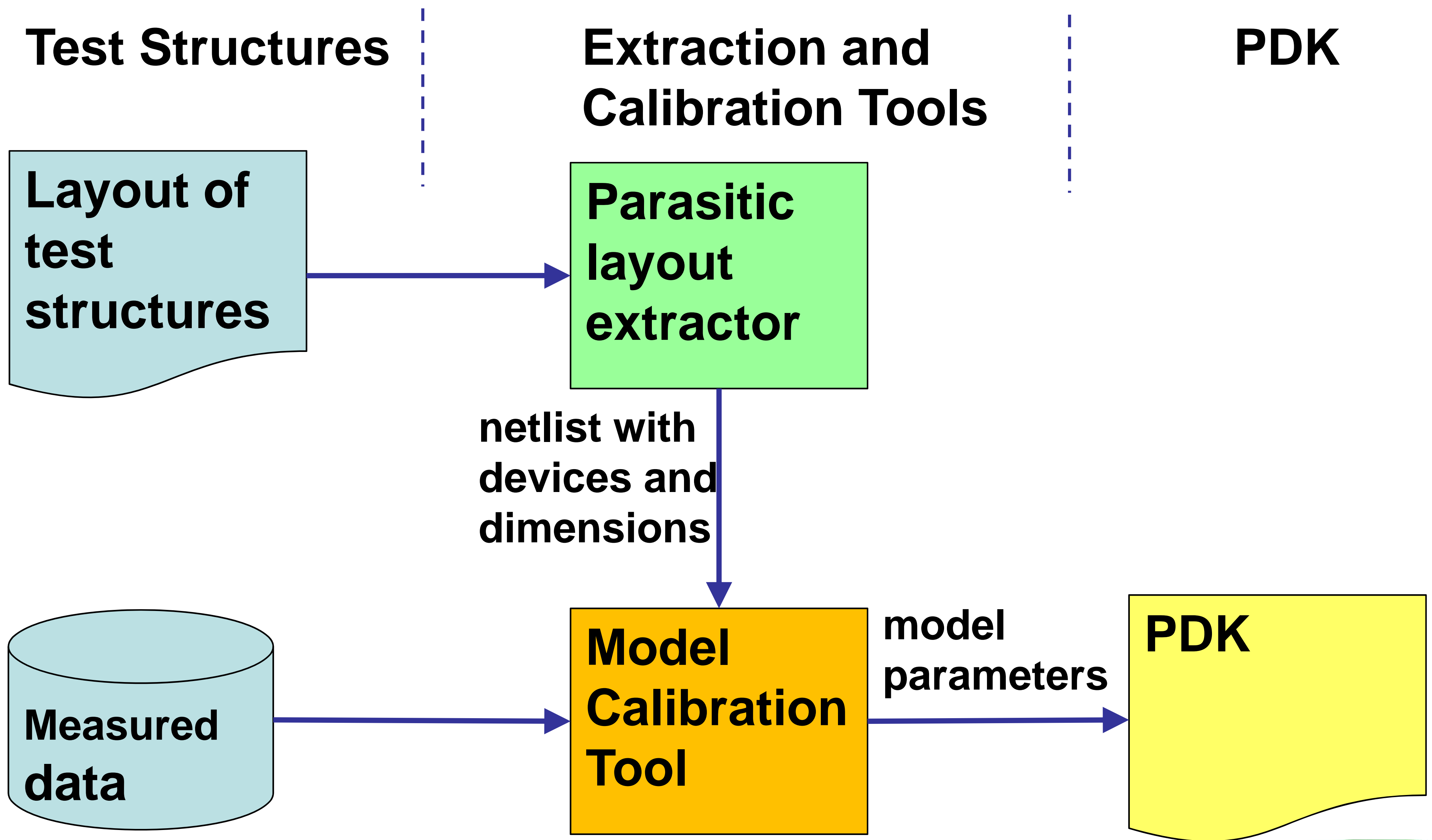
Example Calibration



Calibration on standard diodes and advanced test structures



Integration of calibration into the design flow



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Model Benchmarking

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Model Benchmarking

Benchmark structures Requirements / Project Goals

- State of the art automotive technologies
- Tool calibration and development
- Automotive design and product related
  - Voltages up to 120V
  - High temperature up to 200° C
  - High current injection
  - Large circuits investigation
  - ESD events.

Selected Technologies

- 0.16um BCD process of ST microelectronics.
- 0.35um HV CMOS process of ams AG

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Summary of selected benchmark structures

Benchmark Type	Defined Benchmark Structure	Process	
		ams HV CMOS	ST BCD
Calibration	Single Diodes	X	x
Simple test-structures	Bipolar devices	X	
	Distance structures	X	
	Shielding Structure	X	
	Spatial Orientation	X	
	Multiple Collector		X
Challenging structures	H-Bridge	X	
	DCDC Output Stage	X	
	PAD injection	X	
	Power Bridge		X
	On Chip Sensor	X	

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Benchmark Cases

Benchmark Case	Simple Benchmark	Challenging Structures
High Temperature	x	
High Voltage	x	x
Distance Variation	x	
Guard ring	x	
Multiple Collector	x	
Spatial orientation	x	
Transient pulses		x
Real World (Automotive Applications)		x

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Simple Benchmark Structures

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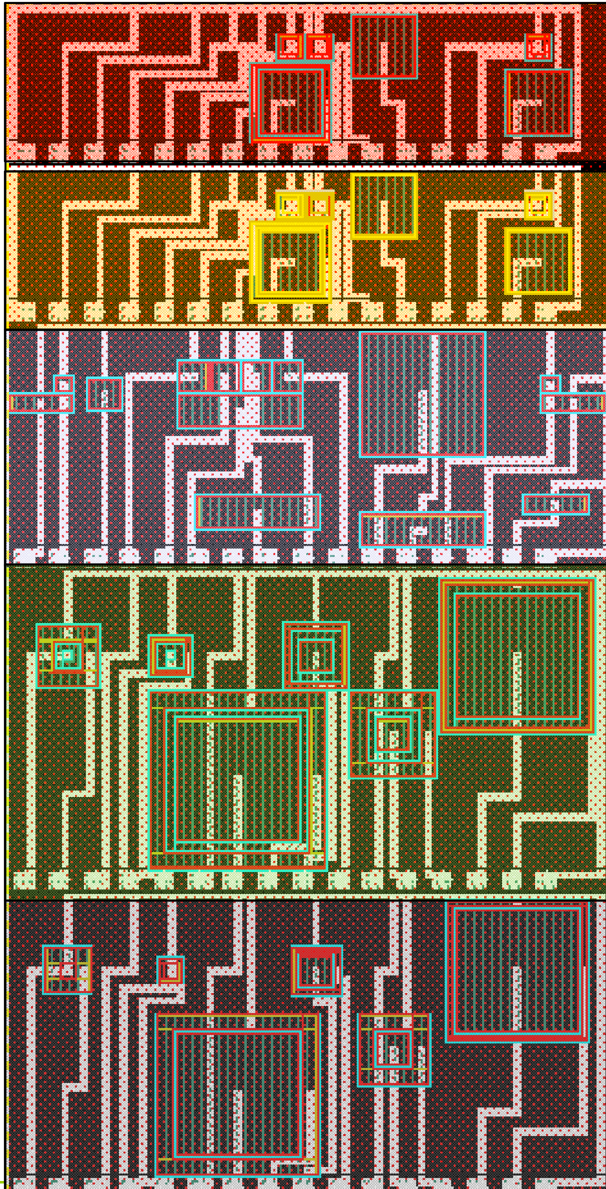
Simple Benchmark Structures

Layout Nwell and DNwell:



Test-chip for simple benchmark structures:

- five sub-chips developed for tool validation
- The test-chip is designed to provide automated measurement capabilities
- Key figures
  - Distance investigation
  - Spatial orientation
  - Shield influence
  - Voltage dependency
  - Temperature dependency
  - Different well doping
  - Different well sizing

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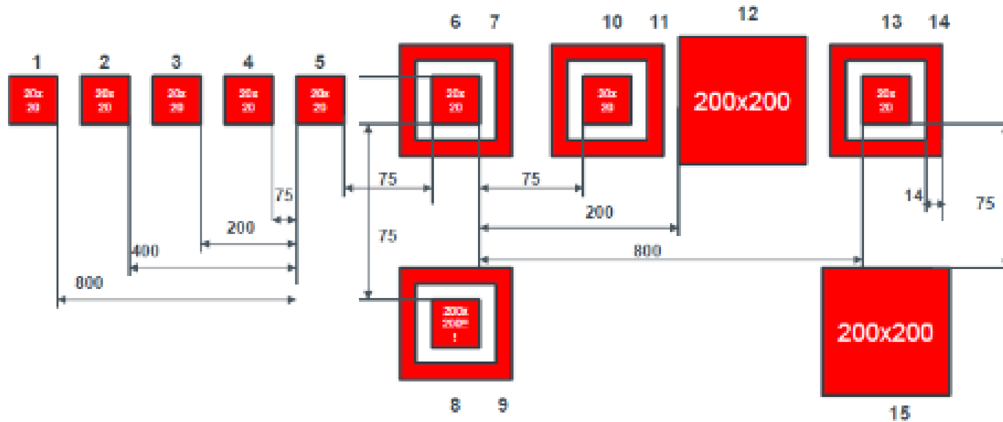
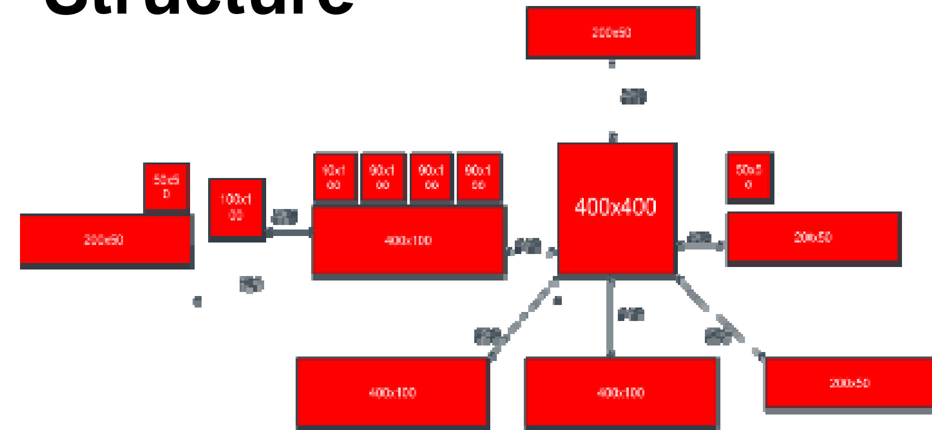
Simple Benchmark Structures

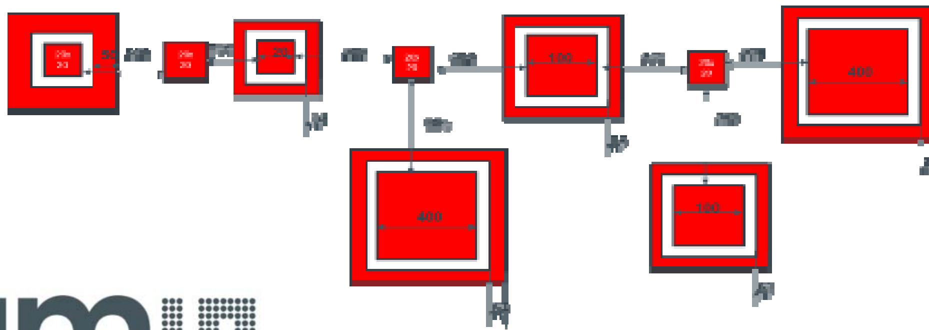
Distance Biasing Structure



Spatial orientation Structure



Shielding Structure



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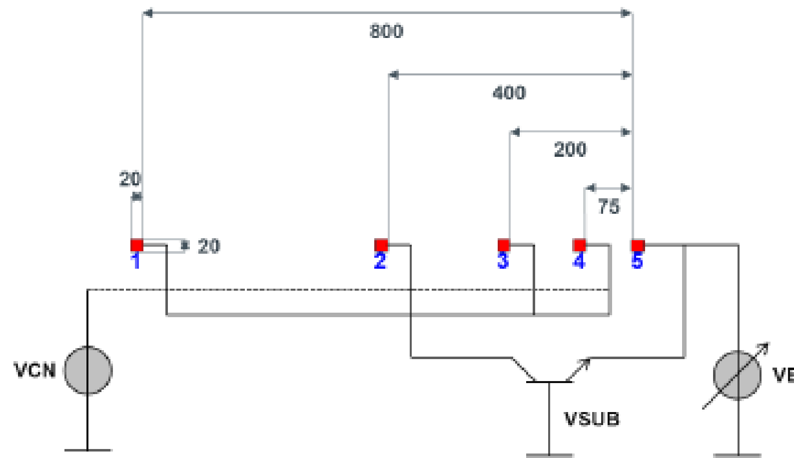
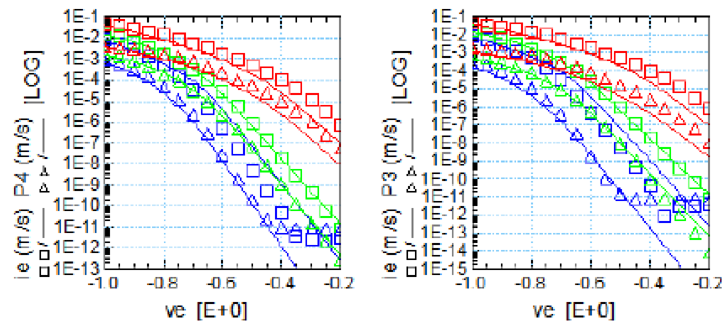
Distance Benchmark Case



Distance Benchmark for different Temperatures and voltages



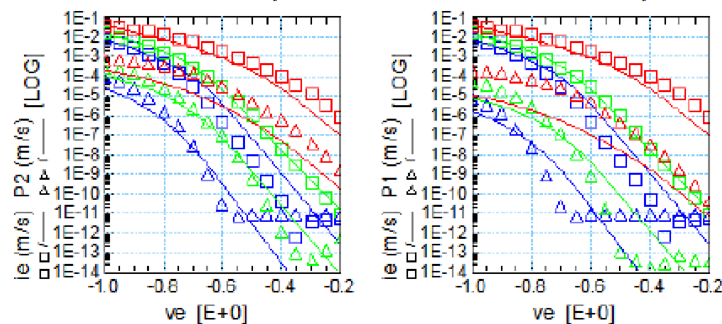
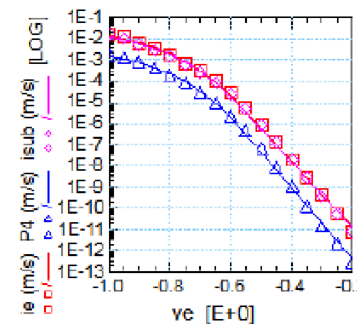
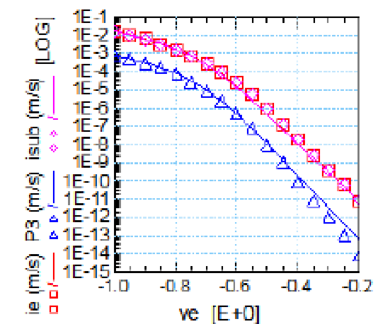
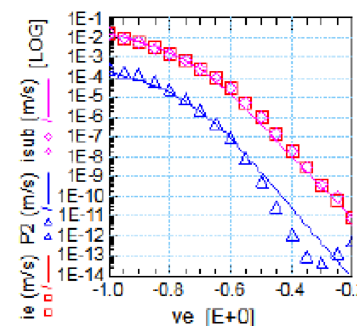


Figure 15: SUBC1T1, temperature dependency of emitter (ie) and collector current (ic) versus ve
25°C, 27°C, 125°C







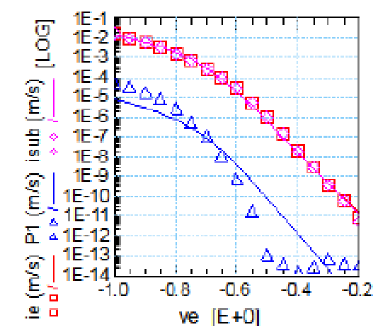


Figure 13: SUBC1T1, measured currents at the different Pads in dependency of emitter voltage

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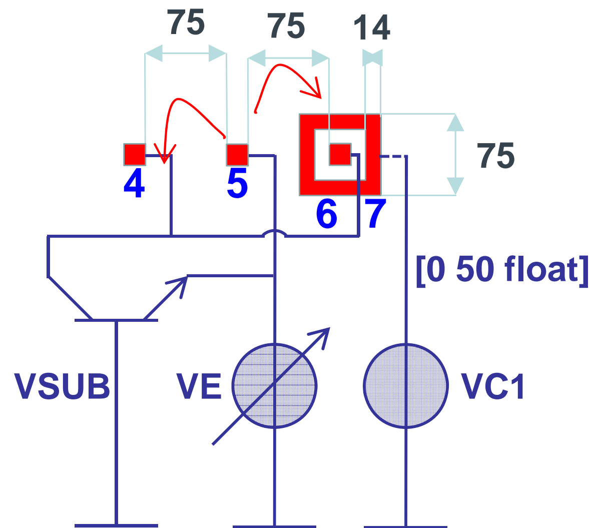
Guarding Benchmark Cases

Guard ring measurements – Emitter = 5 - IC/IE dependent on guard ring



VC1 optional @ Pad 7 [0 50 float]

Measurement Procedure:

- Pad 5 is emitter, 4 & 6 are connected to ground
- Pad7 (guard ring) is connected to a separate Voltage source or floating
- Investigate Pad 6 as function of VC1 (Guard ring influence) vs. Pad 4

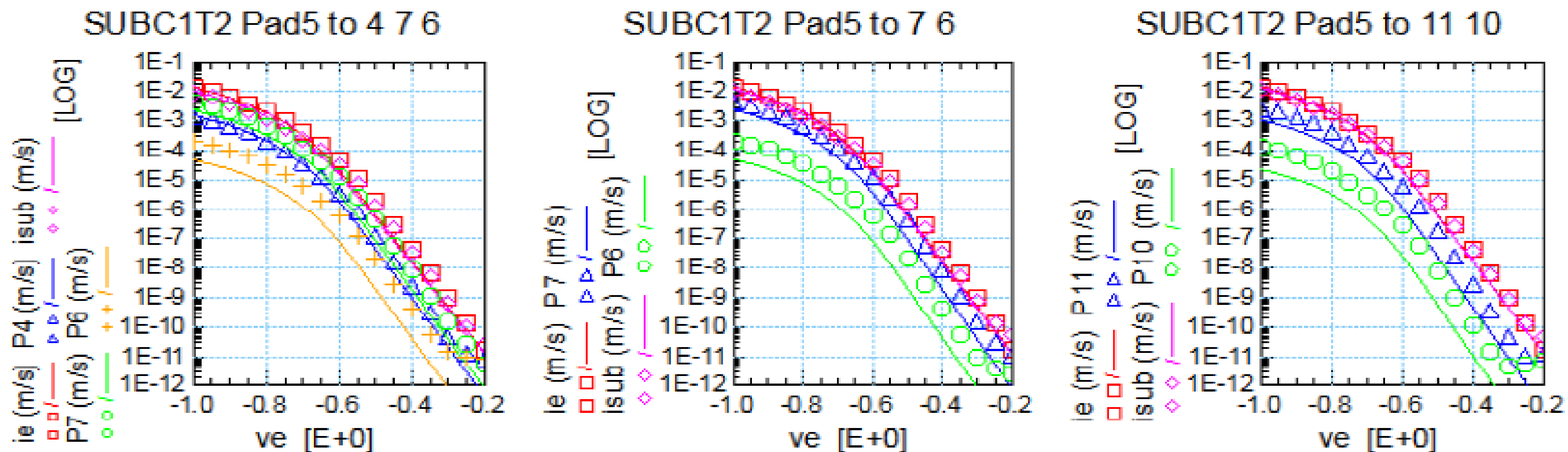


Figure 17: SUBC1T2, measured currents at the different Pads in dependency of emitter voltage

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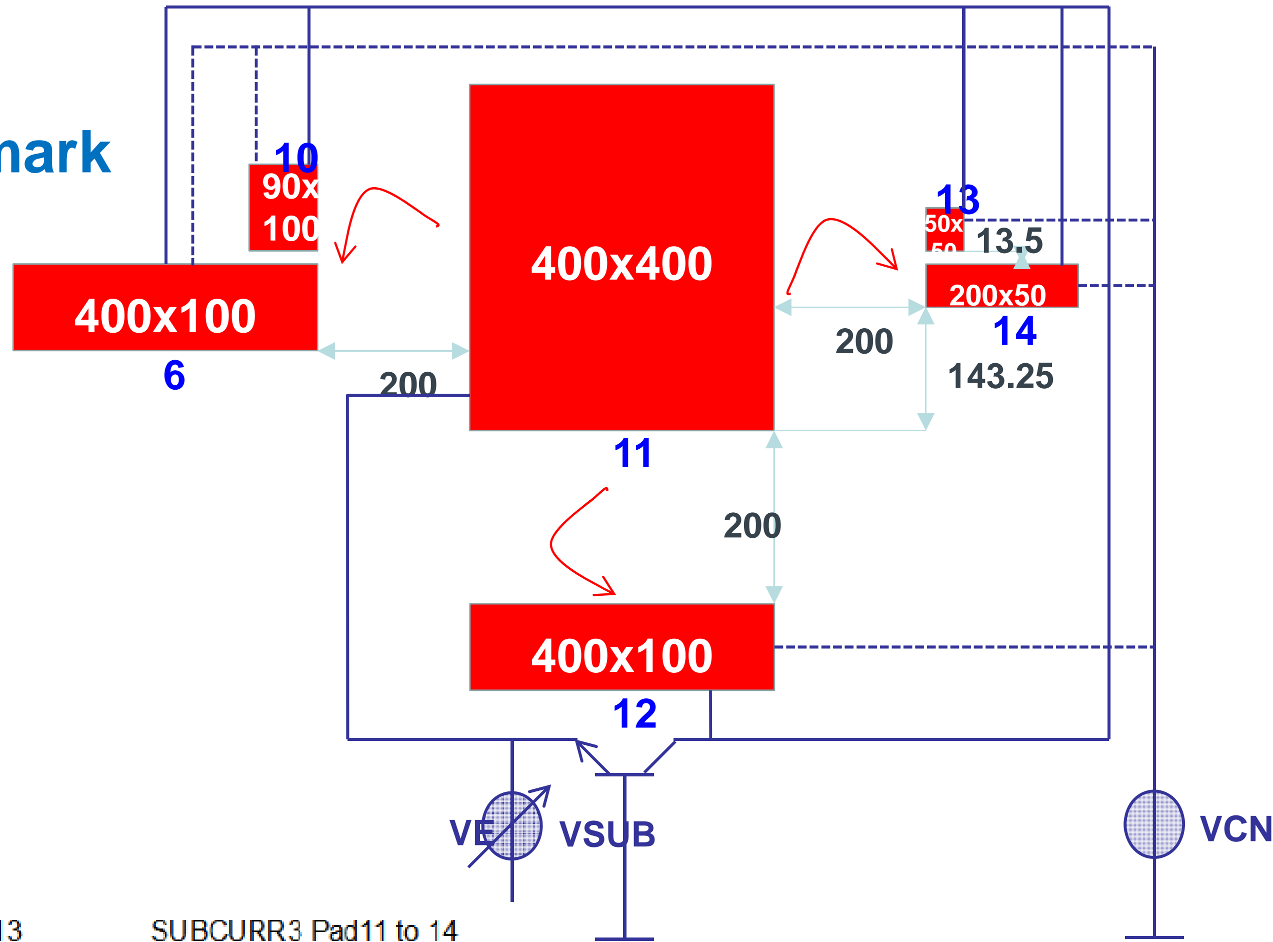
Size Benchmark Cases

Size vs. Orientation Benchmark



@ Pads 6,10,12,13,14

Description:

- IC/IE
- 1 collector connected
- All pads are 200µm away from the emitter

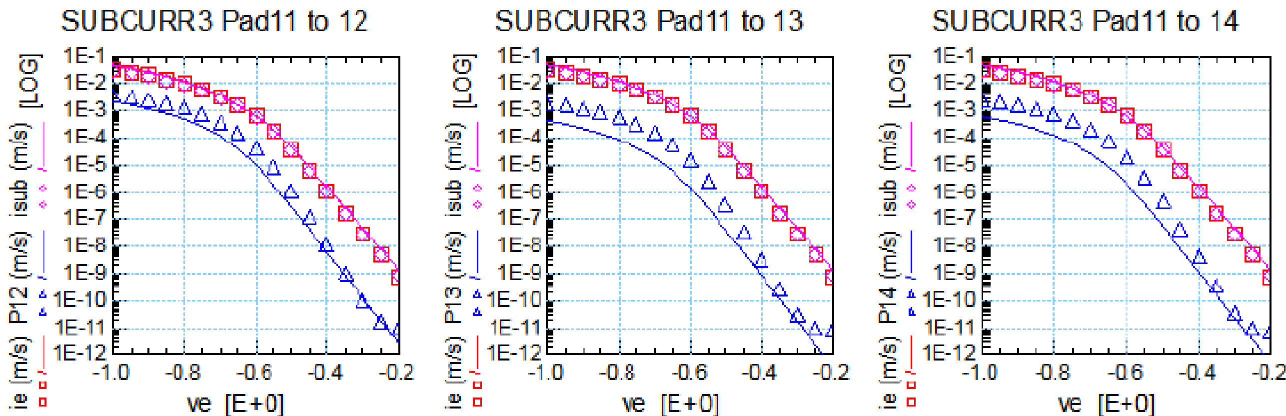


Figure 31: SUBCURR3 case 2, measured currents at the different Pads in dependency of emitter voltage

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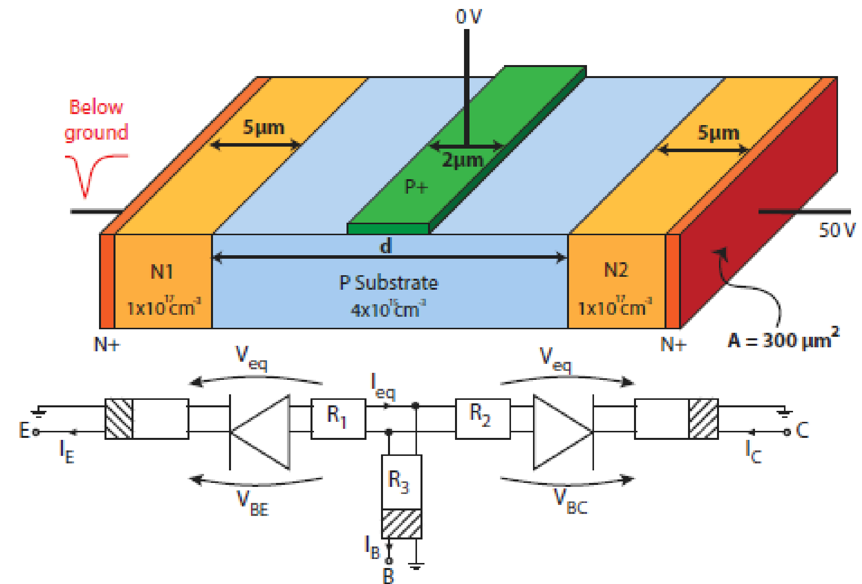
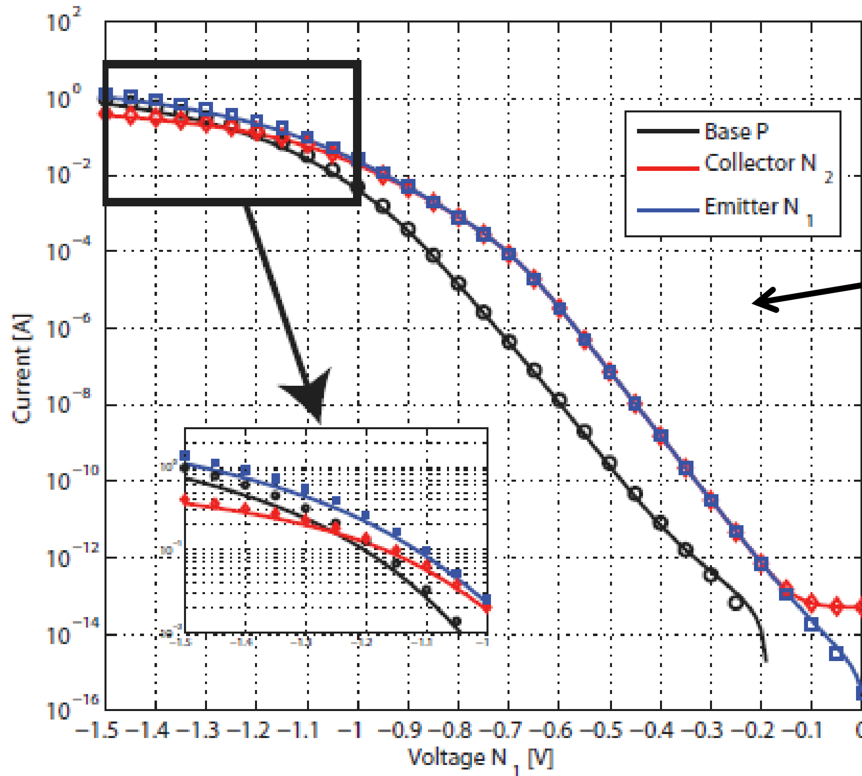
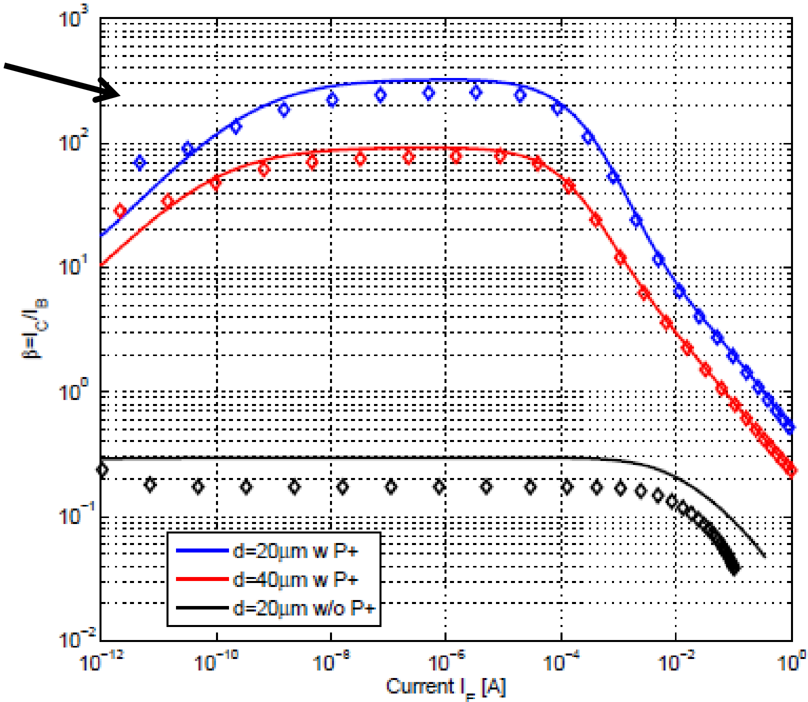
DC Parasitic BJT

Temperature **dependencies are included as well in the model**





TCAD



C. Stefanucci et al., PRIME, 2014

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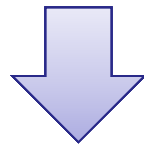
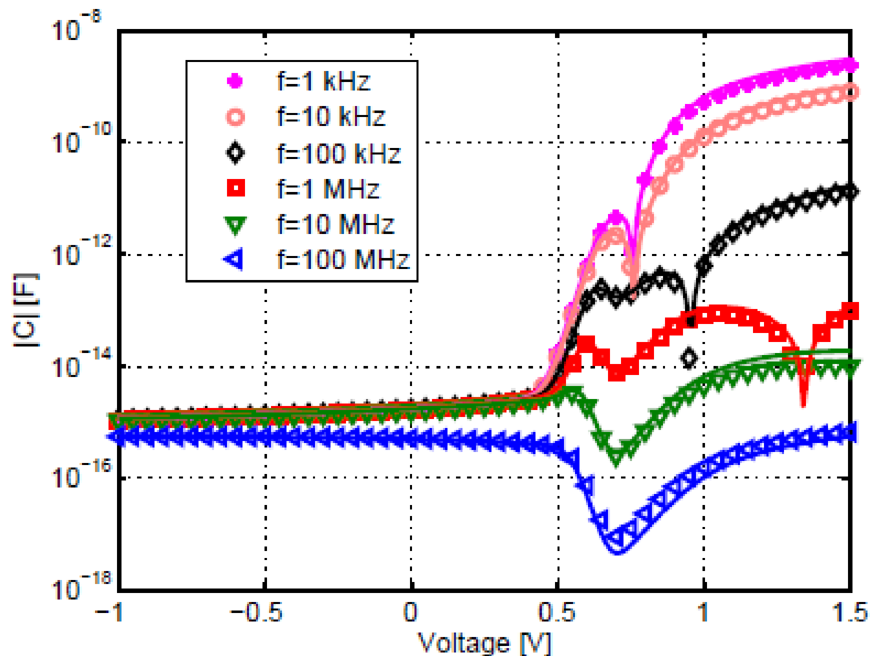
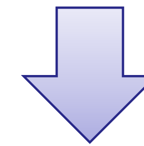
AC selected examples

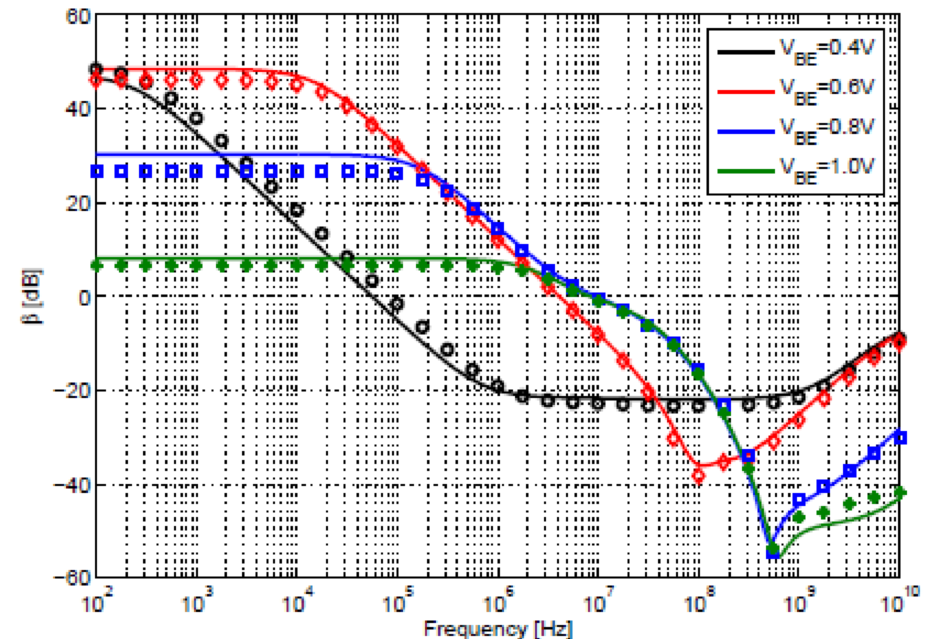
Diode capacitance (and inductance) can be efficiently simulated





BJT cut-off frequency and frequency degradation of beta can be simulated





Spice simulation time 9 min – TCAD simulation time 10 hours

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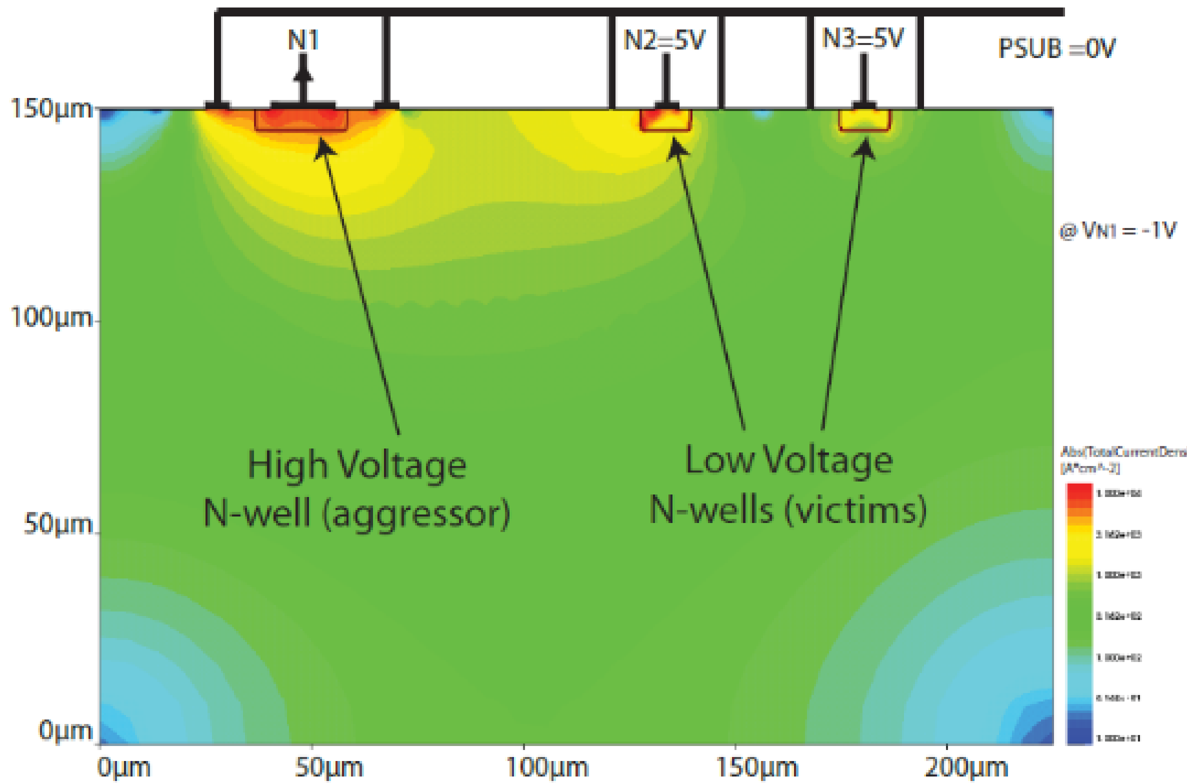
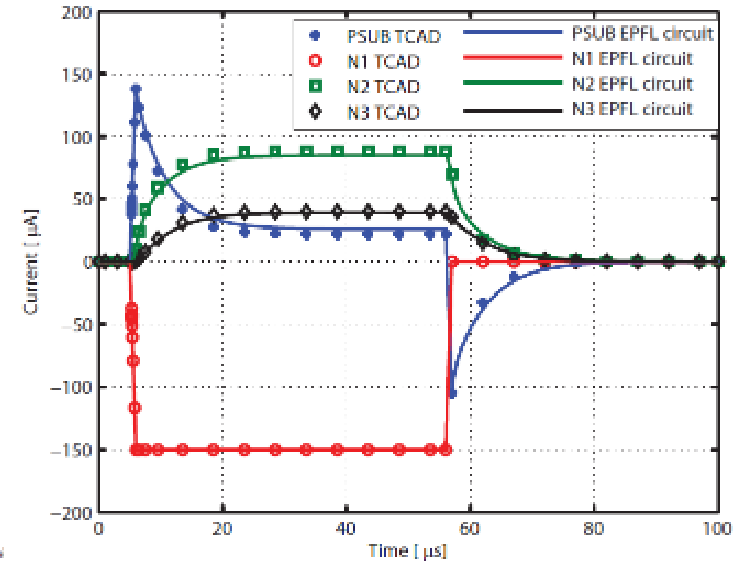
Transient simulations

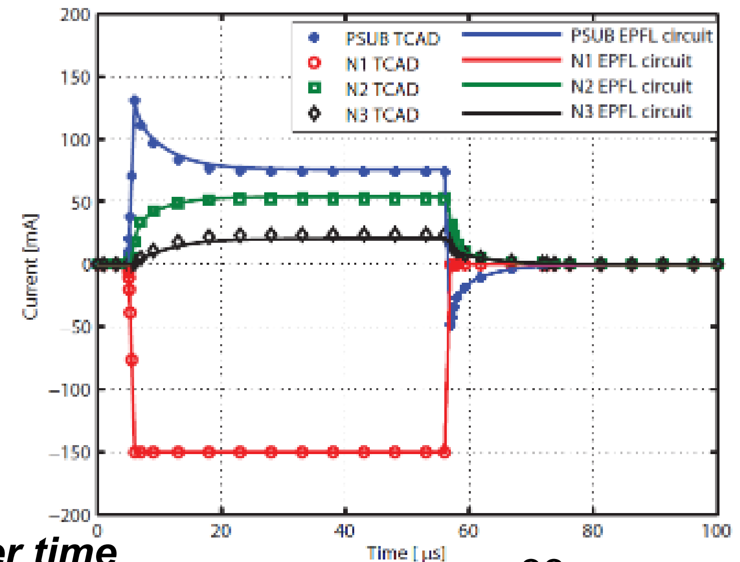
Aggressor-victims



Low-injection



High-injection



- **Transient study of coupling phenomena is different in low and high injection regime**

Spice netlist (128 nodes) 10ms – TCAD 15s per time step

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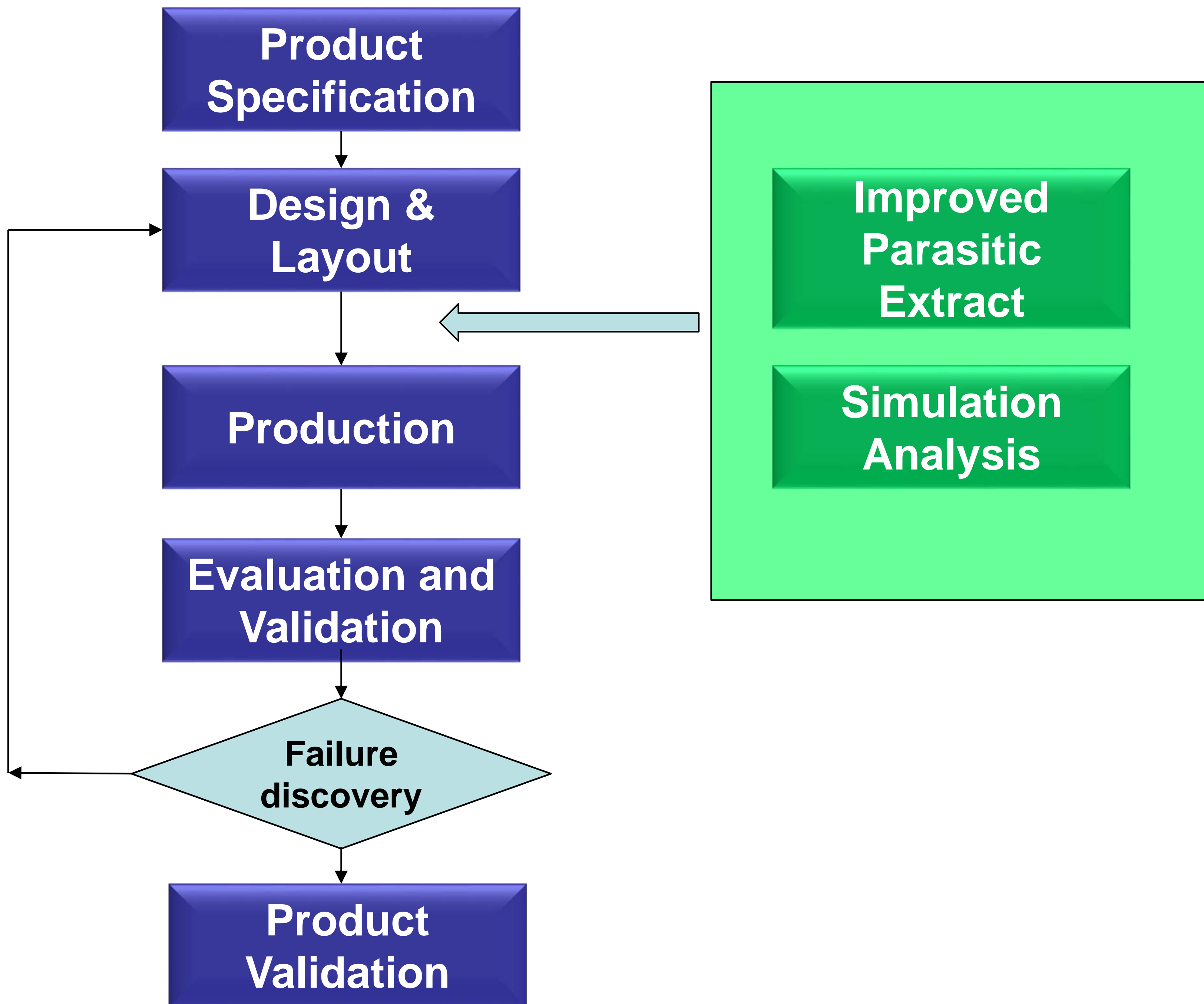
AUTOMICS Design Flow



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Outlook

Industrial Implementation of new design flow

- **Improved model convergence**
- **Automated/adapted grid generation**
- **Model order reduction for large circuits**
- **Parameter extraction standardization and automation**
- **PDK implementation**

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European FP7 - AUTOMICS Project

Scientific Coordination

European FP7 - AUTOMICS Project

Smart Power ICs are extensively used in automotive embedded systems due to their unique capabilities to merge low power and high voltage devices on the same chip, at competitive cost. In such devices, induced electrical coupling noise due to switching of the power stages, when integrating such high voltage (HV) devices with low voltage (LV) functions, is a big issue. During switching, parasitic voltages and currents, consisting of electrons and holes, lead to a local shift of the substrate potential that can reach hundreds of millivolts. This electrical coupling noise can severely disturb low voltage circuits. Such parasitic signals are known to represent the major cause of failure and costly circuit redesign in power integrated circuits. Furthermore, parasitic carrier injections are considerably increased under high temperature operation such as those encountered in automotive applications where this problem is even more severe since these dedicated IC's need to be highly reliable and stable with time. Most solutions are layout dependent and are thus difficult to optimize using available electrical simulator software. The lack for a model strategy that would enable to simulate accurately the injection of minority carriers in the substrate as part of the HV model, as well as its propagation in the substrate, is one of the main reasons for this critical situation. This lack for a design methodology prohibits an efficient design strategy and fails at giving clear predictions of perturbations in high voltage integrated circuits. This picture motivates this project proposal where all these aspects are addressed to create a link between circuit design, modeling and implementation in innovative computer aided design tools. This concerns smart power IC's dedicated to automotive applications requiring co-integration of high voltage power stages with low voltage analog/digital blocks on the same chip, still being reliable when operating at high temperature.

Scientific Coordination

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Thank You For Your Kind Attention.

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Any Questions ?