GaNScan: Modeling of GaN HEMTs on Silicon Substrate

Sayed Ali Albahrani[1)], Joachim Burghartz[2)], Mahimna Dwivedi[3)], Thomas Gneiting[3)], Lars Heuken[2)]

[1)]Fraunhofer-Institut für Angewandte Festkörperphysik IAF, Freiburg, Germany
[2)]IMS Chips, Stuttgart, Germany
[3)]AdMOS GmbH, Frickenhausen, Germany

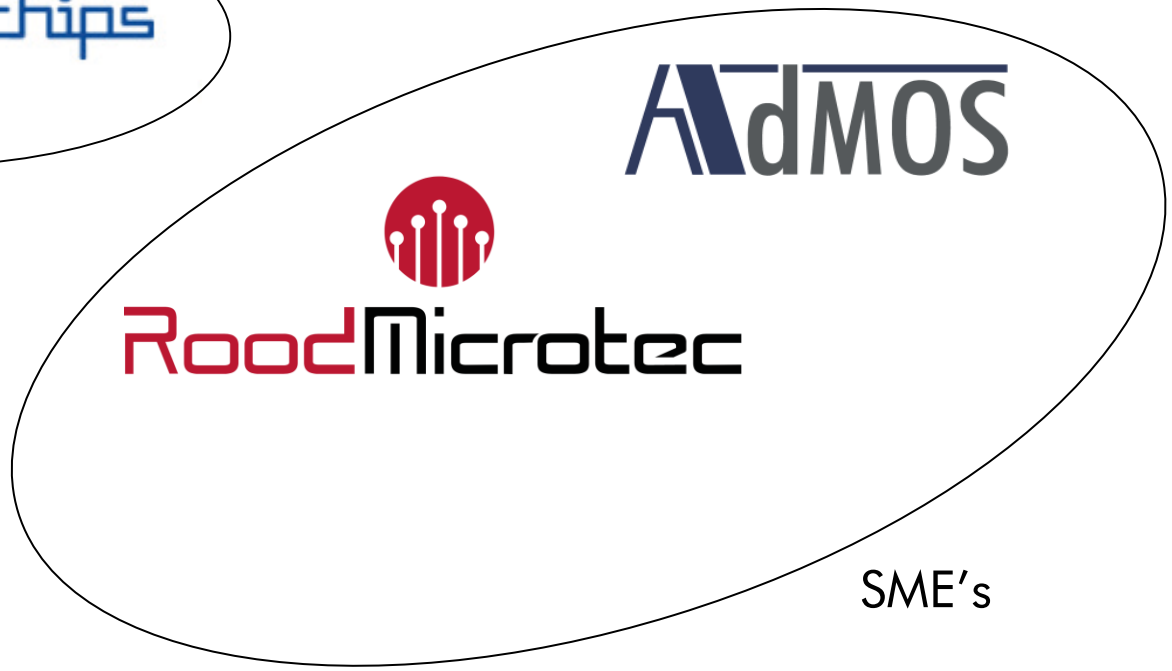
thomas.gneiting@admos.de

Content

- Joint project GaNScan
- IMS Chips:
  - production of GaN/Si Wafers
  - characterisation
- AdMOS:
  - Applying the ASM HEMT model
  - Extending ASM HEMT for different applications
    - Geometrical scaling
    - Extreme high temperatures
    - Gate current improvements
  - Applying AdMOS' software for model parameter extraction
- Summary

GaNScan Joint Project

Research institute



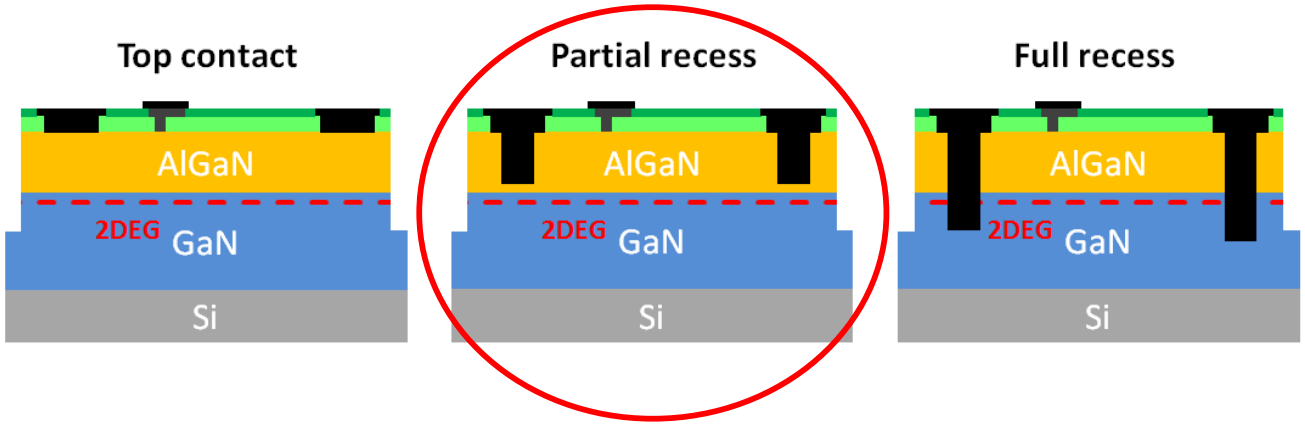
SME's

SPONSORED BY THE
Federal Ministry of Education and Research

This work was supported by the German Federal Ministry of Education and Research through the framework of the Project GaNScan under Grant 16ES0746 (KMU Innovativ).

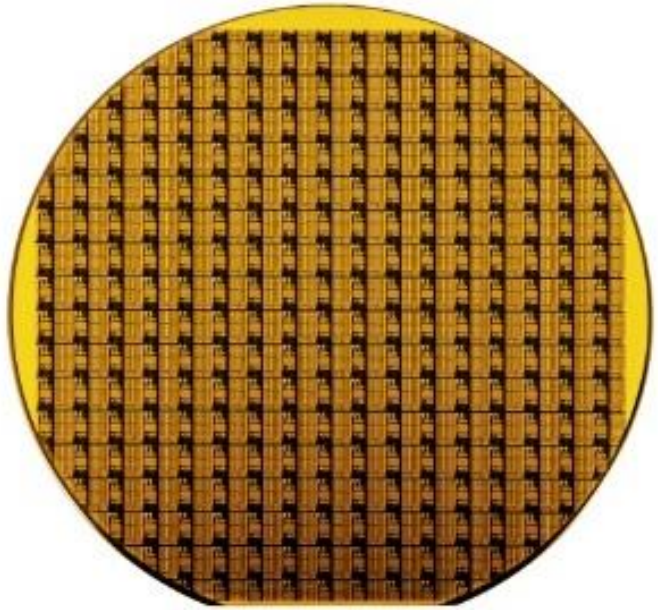
Fabrication of GaN/Si Wafers at IMS Chips

IMS Chips evaluated different concepts for producing an ohmic contact for GaN devices on Si



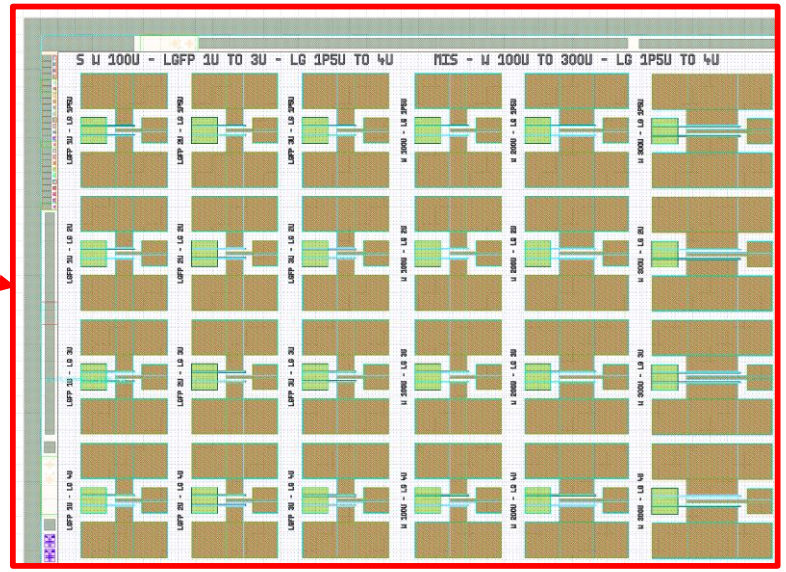
- The concepts "top contact" and "full recess" showed only non-linear I-V characteristics or very high contact resistances during optimization.
- Therefore, the concept of partial recess was pursued further. The optimization showed that a remaining barrier thickness of approx. 8 nm in combination with a Ti/Al metallization and an annealing step at 450 °C for 10 min provides optimal results.

The project partners Rood Microtech and AdMOS could use typical 150 mm GaN/Si HEMT wafer for their own experiments:



GaN Test Chip from IMS Chips

Testchip on Wafer E8326

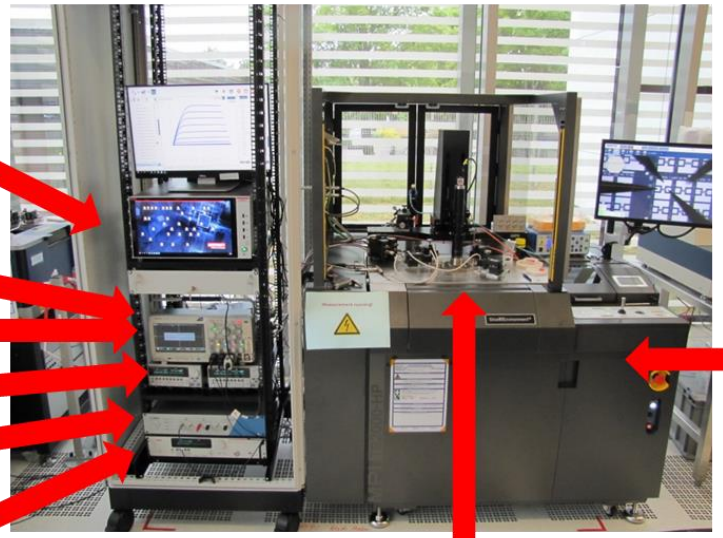


Area with Schottky and MIS Transistors:

- Schottky:
  W=100um, LG=1.5-4um, LGFP= 1-3um
- MIS:
  W=100-300um, LG=1.5-4um

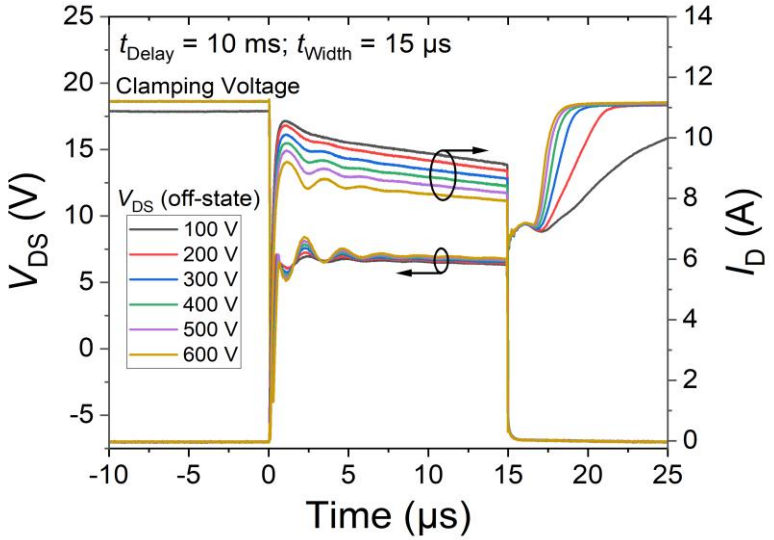
Cooperation AdMOS – IMS for pulsed measurement techniques

- I-V
- C-V
- Pulsed
- Reliability



New installed probe station at IMS Chips for the automated test of GaN/Si wafers up to a diameter of 200 mm.

Drain-source voltage and drain current of a typical multi-finger power transistor (W=17 mm) as a function of time during a pulsed experiment to extract the on-resistance In the off-state of the power transistor a stress voltage of 100 to 600 V was applied.



Work on the GaN ASM HEMT model code

During the GaNScan project, the following work on the GaN ASM HEMT model was done by AdMOS:

- **Geometrical scaling.**
  The model already includes some basic dependency of the transistor behavior versus design dimensions like gate length or gate width. However, all experiments done on devices from various fabs showed, that this built-in dependency is not sufficient to achieve an accurate simulated behavior. Therefore, an extension is quite important.
- **Temperature behavior at extremely high temperatures**.
  While standard commercial applications are mostly specified for temperature ranges of e.g. -55 to 15°C, there are specialized requirements for e.g. automotives, turbine engines or space applications significantly above 200°C. We could do modeling up to 500°C.
- **Gate leakage**
  A new formulation of **gate leakage current** as a typical indicator for long term reliability was proposed.

  All the results were discussed and shared with the model development team at Macquarie University (Prof. Khandelwal) to allow an integration into the official AMS model code.

Geometrical scaling: Testchip from RWTH Aachen

- AdMOS received first GaN wafer fabricated by RWTH Aachen.
- Successful DC-CV measurements were conducted.
- Three devices with different gate length(Lg) were chosen for modeling.
- The focus of the project during this period was to define basic ASM-HEMT device model and to prepare for extensions of the model code in Verilog-A.

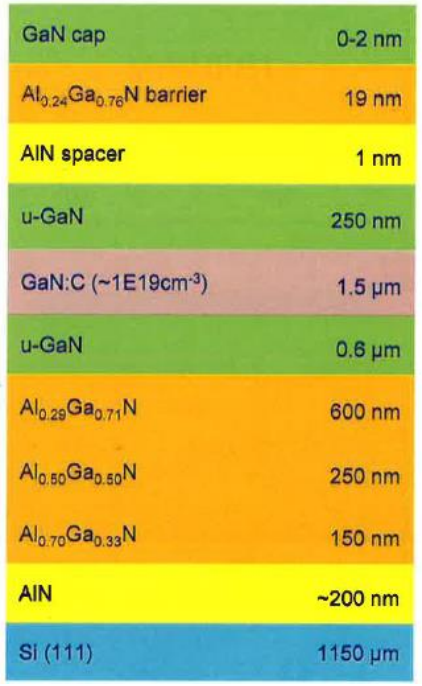


Fig. 1 Wafer Information

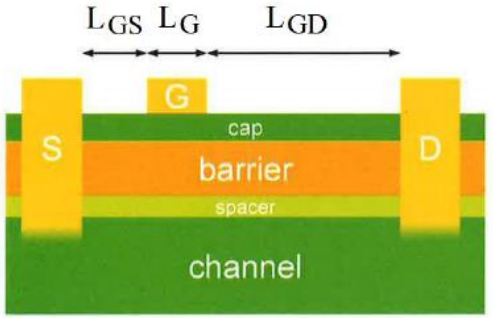


Fig. 2 Schematic Information Of AlGaN/GaN HEMT device

Geometrical scaling: modeling results

Device	L_{GS}	L_G	L_{GD}	W (Width)
D1	1.5μm	2.5μm	2.5μm	50μm
D2	1.5μm	5μm	2.5μm	50μm
D3	1.5μm	10μm	2.5μm	50μm

Table 1: The Geometries associated with the measured devices

- For each device, a seperate model card was generated starting with the shortest length (D1)
- To fit the second device (D2, D3) only dedicated parameter were changed (see next page)
- Drawback: measurements were done under normal DC conditions containing a significant part of self heating.

D1, L=2.5um

D2 L=5um

D3 L=10um

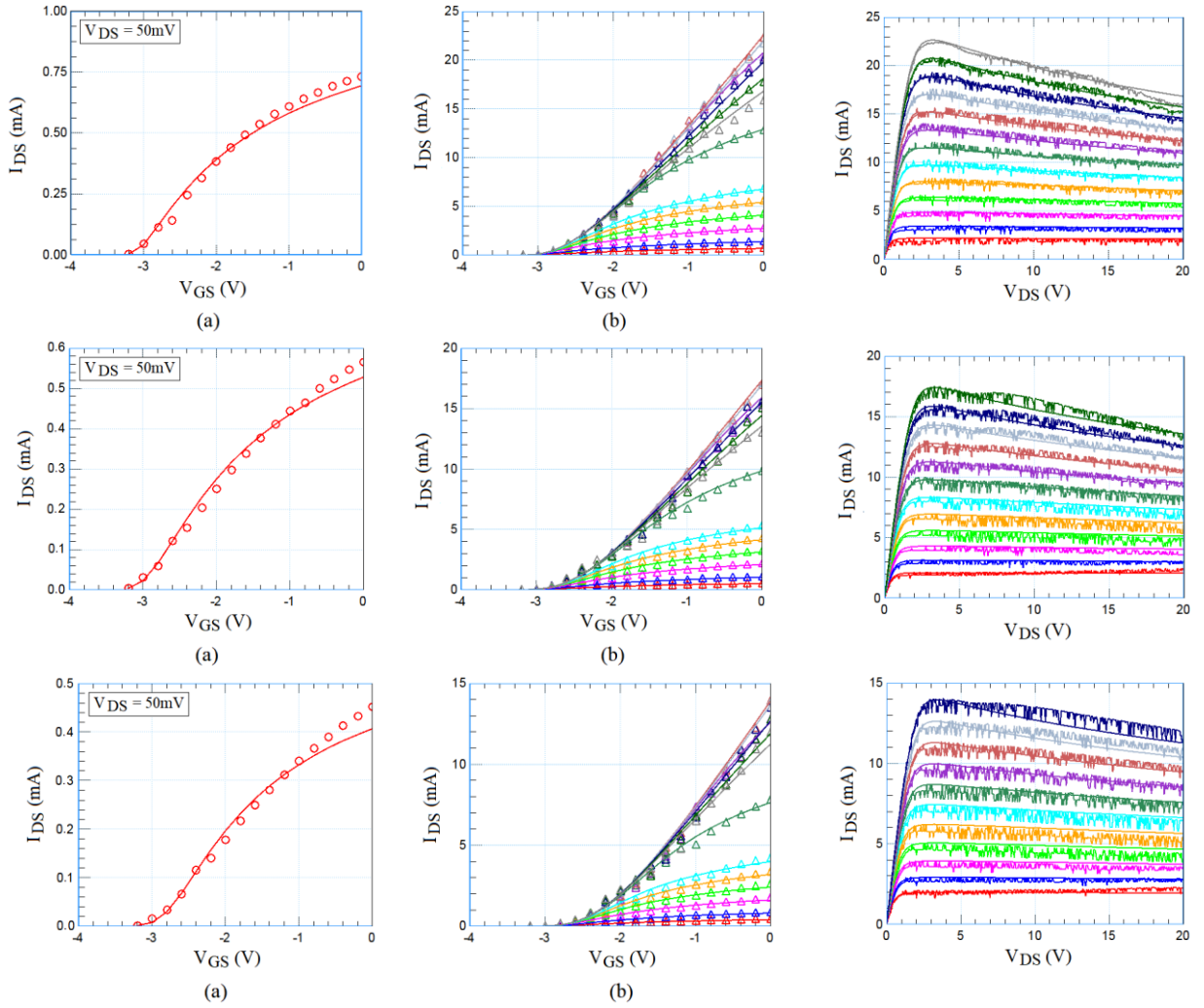


Fig. 3 Modeling Results for D1(2.5 μm),D2(5 μm),D3(10 μm)

Effect of gate length on different parameters

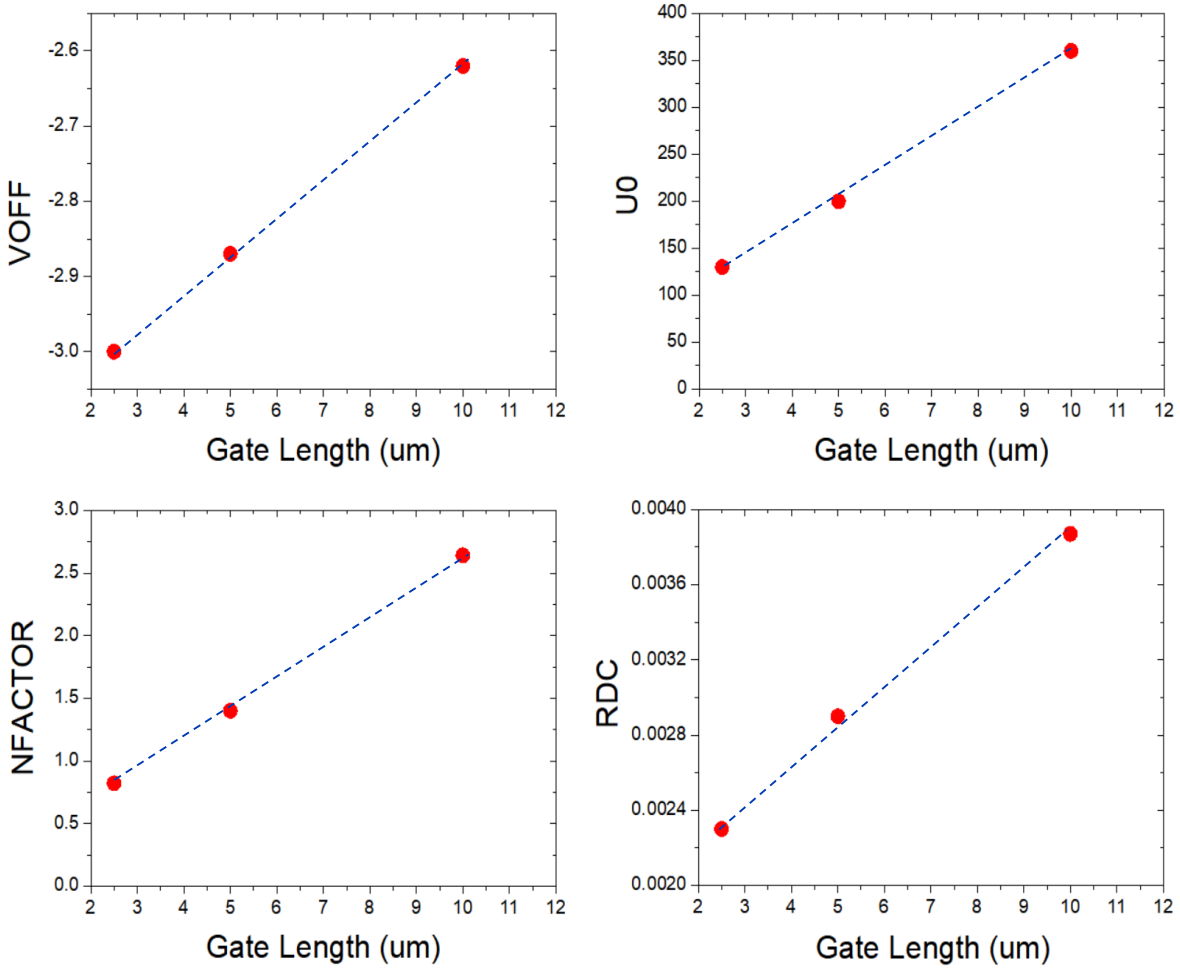


Fig. 4 Change in Model Parameters as a Function of Gate Length

- All 4 parameters show a nearly perfect linear fitting behavior versus gate length.
- Therefore, the following scaling behavior was implemented in the SPICE modelcard:

$$P_{eff} = P0 + PL \cdot L$$

Peff: effective parameter values
P0: basic parameter value
PL: length dependent parameter change

example RDC:

$$RDC = RDC0 + RDCL \cdot L$$

Geometrical scaling: advanced pulsed measurement from IMS Chips

- Using the new established measurement equipment at IMS Chips, it was possible to perform measurements with very short pulses around 1us pulse width to exclude self-heating and trapping effects.

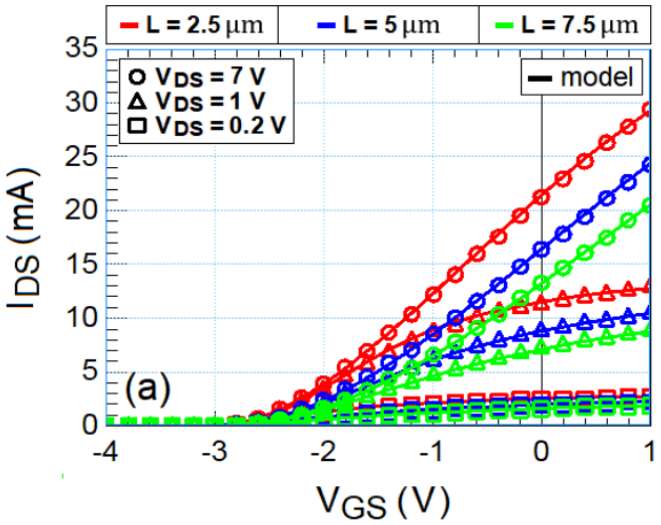


Fig. 5 Transfer Characteristics

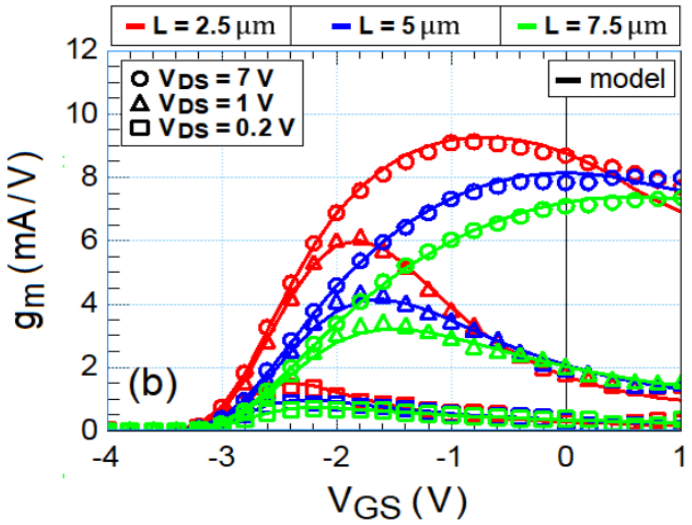


Fig. 6 Transconductance change with VGS

- Diagrams above show the adjusted model with the previously showed scaling equations.[1]

[1] S. A. Albahrani, J. Hodges, L. Heuken, D. Schwantuschke, T. Gneiting, J. G. Burghartz and S. Khandelwal, "Validation of the Industry-Standard ASM-GaN Model for Gate-Length Scaling", in Fourth Australian Microwave Symposium (AMS'20)

Extreme temperatures: test data from Stanford University

- Due to a cooperation between Maquarie University (former employer of Sayed Albahrani) and Stanford University, it was possible to contribute to the modeling of the GaN HEMT device for operations in extreme temperature environments up to 500°C.
- For this purpose, measurement data received from Stanford University's XLab of AlGaN-GaN HEMT devices on Si substrate were used with the following properties:

1) AlGaN-barrier thickness, *T*BAR = 30 nm.
2) Gate length, *L* = 3 μm.
3) Gate width, *W* = 20 μm.
4) Length of the gate–source access region, *LSG* = 7 μm.
5) Length of the gate–source access region, *LDG* = 7 μm.
6) Number of gate fingers, NF = 1.
7) Temperature range RT – 500°C

Temperature model extension

- The equation for the temperature dependency of model parameters VOFF and NS0ACC were newly derived from the normalized steady-state trap potential $\overline{\overline{v}}$ to the potential Vx

$$\overline{\overline{v}} = \overline{v} / V_x$$

$$\mathrm{VOFF}_x = \mathrm{VOFF}(1 + \mathrm{K_{T1X}}\overline{\overline{v}}_X)$$

$$\mathrm{NS0ACC}_x = \mathrm{NS0ACC}(1 + \mathrm{K_{NS0X}}\overline{\overline{v}}_X)$$

$$\mathrm{VOFF}_t = \mathrm{VOFF}_x(1 - \mathrm{K_{T1}}\Delta\overline{T})$$

$$\mathrm{NS0ACC}_t = \mathrm{NS0ACC}_x(1 + \mathrm{K_{NS0}}\Delta\overline{T}).$$

- The diagrams on the right hand shows the „native“ fitting of the new equations above versus extracted parameters for different temperatures even without using the dedicated temperature parameter

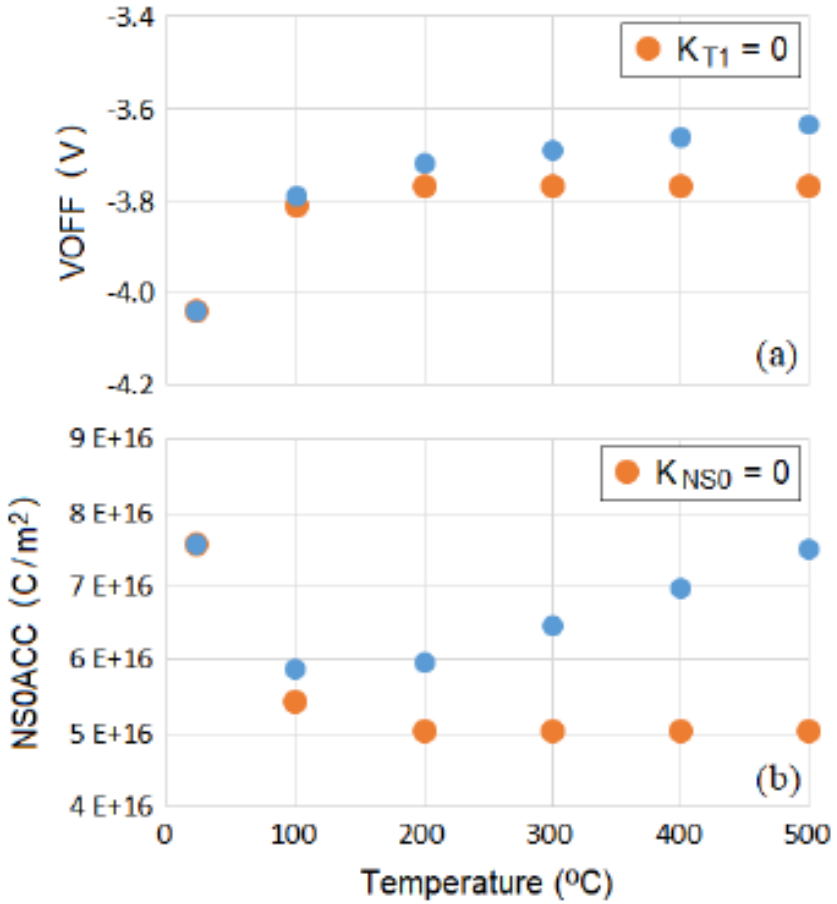


Fig. 9 Non-Linear Model Parameters Variations of HEMT Device from 22° C to 500° C

Test data from Stanford University

- Simulation results versus temperature

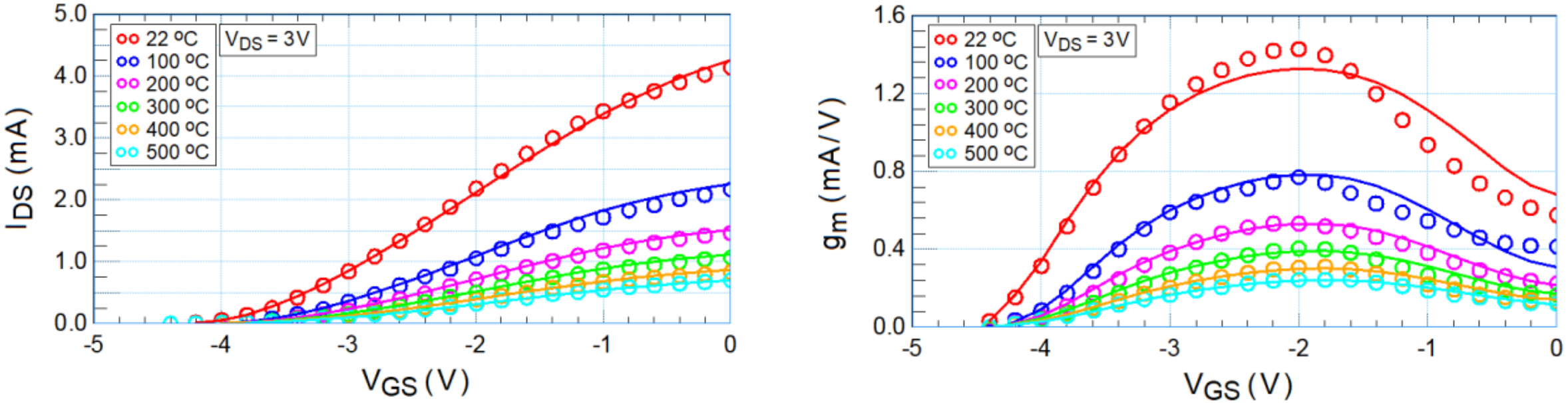
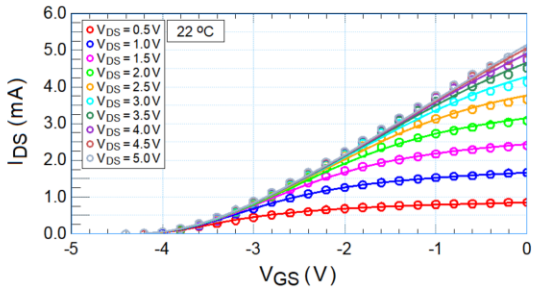


Fig. 7 Modeling of Transfer Characteristics and Transconductance of HEMT Device from 22° C to 500° C [2]

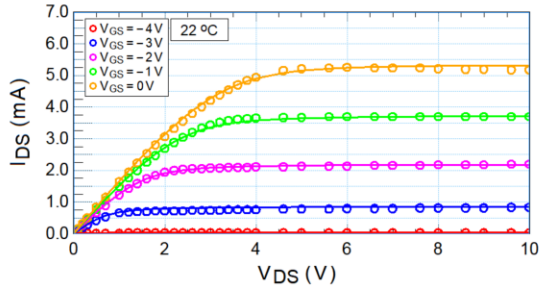
Test data from Stanford University

- Explicit simulation results versus measurement at different temperatures
- Transconductance and output behavior.
- Improvements in the model equations are proposed to be included in the standard ASM HEMT model.
- Work resulted in a paper [2]

T=22°C

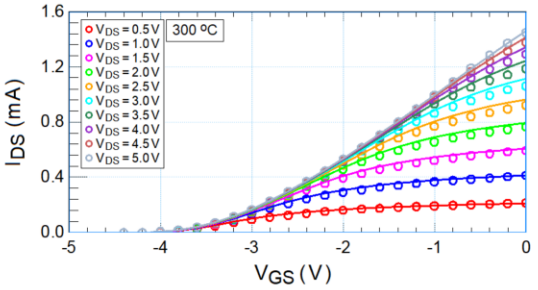


(a)

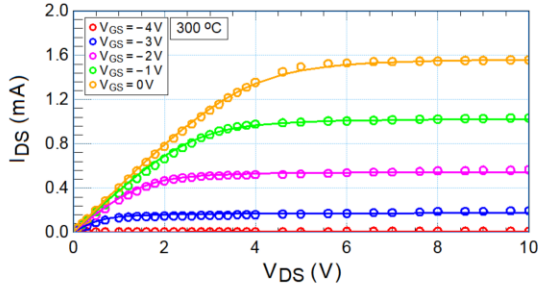


(a)

T=300°C

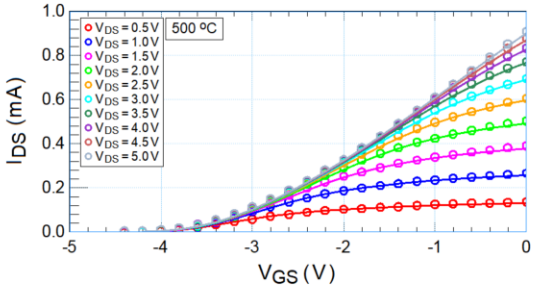


(b)

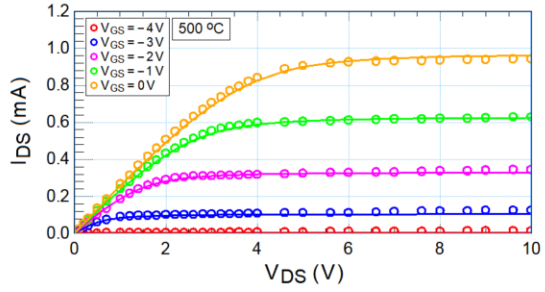


(b)

T=500°C



(c)

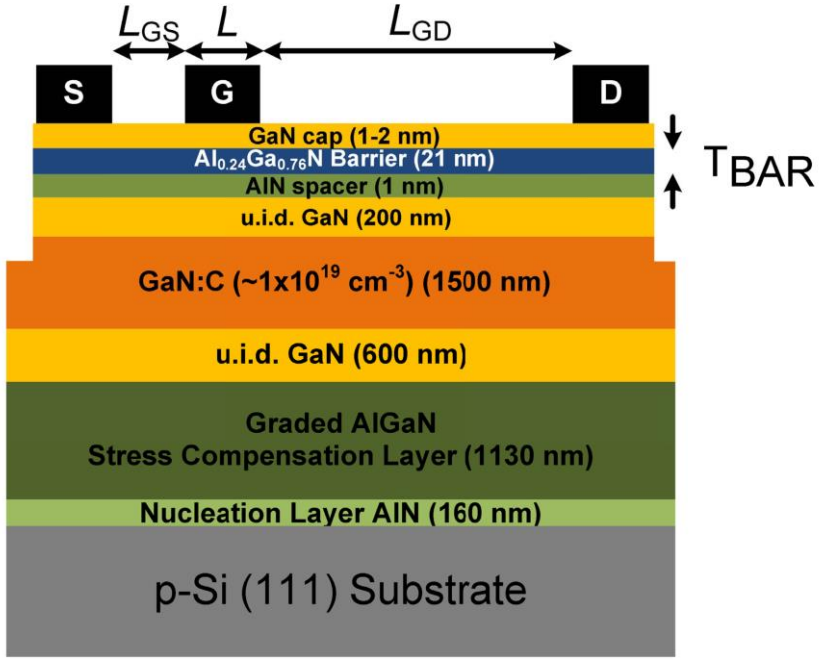


(c)

[2] S. A. Albahrani, D. Mahajan, S. Kargarrazi, D. Schwantuschke, T. Gneiting, D. G. Senesky, and S. Khandelwal, "Extreme Temperature Modeling of AlGaN/GaN HEMTs", IEEE Trans. Electron Devices, Vol. 67, no. 2, Feb. 2020

Gate current modeling

- For the experiment of gate modeling, the following 2 devices have been used and have been completely measured at AdMOS laboratory.
- Wafers were provided by IMS Chips which purchased them.
- AlGaN/GaN Schottky HEMTs grown on 200-mm p-Si substrates by MOCVD, with no applied surface passivation, with the following geometries:
  1) gate lengths *L* of 5 and 2.5μm;
  2) gate width $W = 50\mu$m;
  3) thickness *T*BAR of the AlGaN layer = 21 nm;
  4) length *L*GS of the gate–source access region = 2 μm;
  5) length *L*GD of the gate–drain access region = 2.5μm;
  6) number of gate fingers NF = 2.



Gate current modeling

- The forward and backward gate current is modeled by taking into account Thermal Emissions, the Poole-Frenkel emissions and the Fowler-Nordheim tunnel effect.
- This model has been validated with the experimental data for different temperature conditions and gate & drain voltages and for a different device gate length. [3]

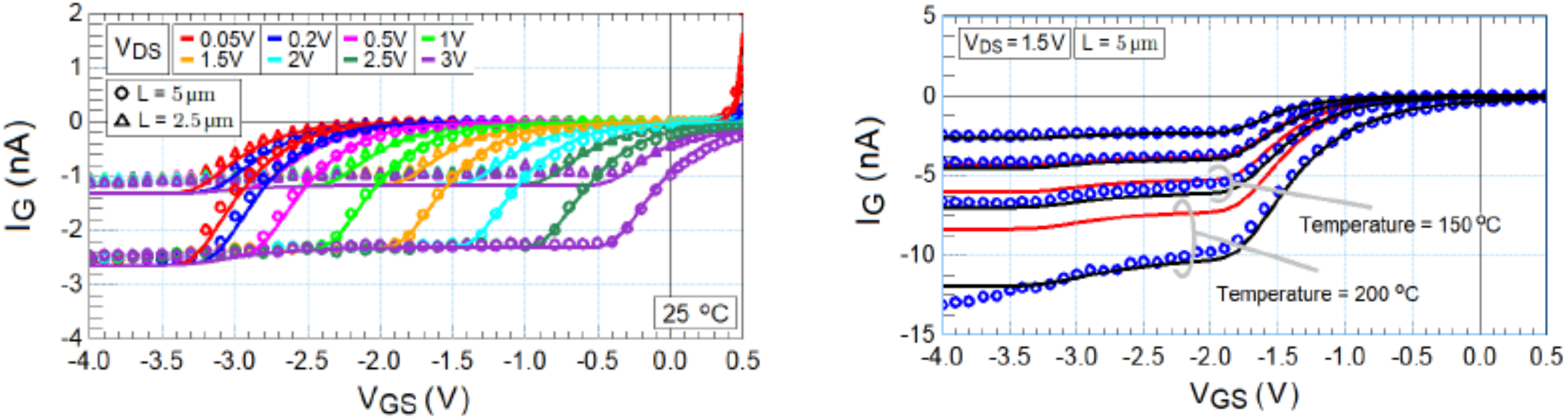


Fig. 10 Gate Current Model with Length and Temperature Variation[3]

[3] S. A. Albahrani, L. Heuken, D. Schwantuschke, T. Gneiting, J. G. Burghartz and S. Khandelwal, "Consistent Surface-Potential-Based Modeling of Drain and Gate Currents in AlGaN/GaN HEMTs", IEEE Trans. Electron Devices, Vol. 67, no. 2, Feb. 2020

Implementation in AdMOS „ModelCal“

- The software "ModelCal" was initially developed within the scope of a ZIM project with the focus on substrate modeling.
- After the end of the ZIM funding phase of the basic components of the software, the other commercially important components (licensing etc.) are currently being implemented to make the product ready for the market.
- GaNScan was the ideal example to test and refine functions of the software:
  - User-specific functions for the determination of parameter parameters (Vtlin, GMMAX, ..)
  - Refining the extraction and optimization options
  - Performance improvement of the interface to the simulator (Spectre)
  - Display of diagrams and scalable displays
  - …

ModelCal: Circuit definition and model parameter management

Definition new Modellparameters

Integration of scaling equations

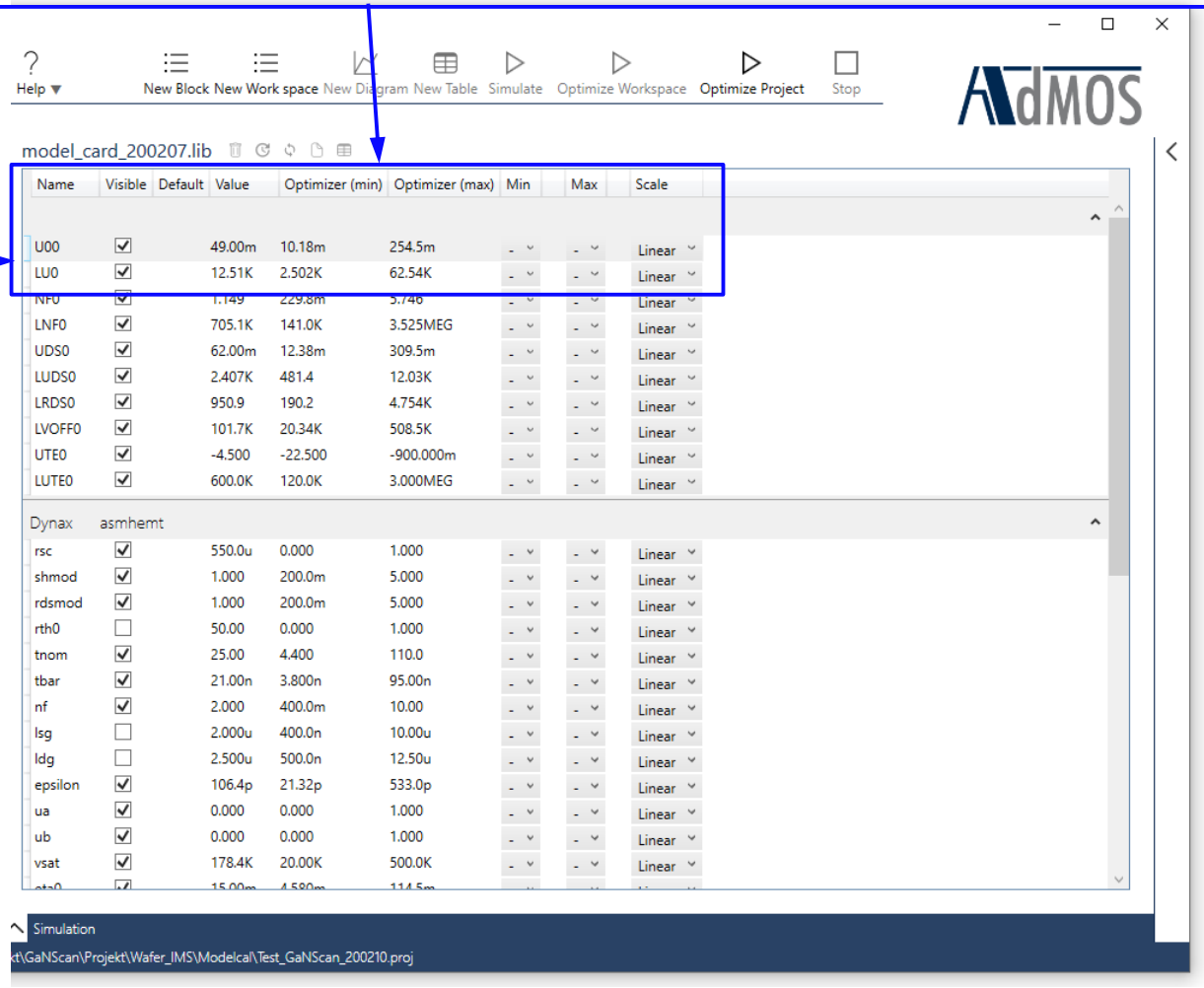
model_card_200207.lib

```
subckt Dynax_sub(D G S B DT)
parameters lfp1=1u l=1.5u w=100u
parameters U00 = 0.0509
parameters LU0 = 12508
parameters NF0 =  1.1492
parameters LNF0 = 705085
parameters UDS0 =  0.0619
parameters LUDS0 = 2406.8
parameters RDS0 =  - 0.0007
parameters LRDS0 = 950.85
parameters VOFF0 =  - 2.9169
parameters LVOFF0 = 101695
parameters UTE0 =  -4.5
parameters LUTE0 = 100000

M1 (D G S B DT) Dynax  lfp1=lfp1 l=l w=w

model Dynax asmhemt
+ voff         = VOFF0 + LVOFF0 * l
+ u0           = U00 + LU0 * l
+ u0accs       = UDS0 + LUDS0 * l
+ u0accd       = UDS0 + LUDS0 * l
+ ute=UTE0 + LUTE0 * l
+ nfactor      = NF0 + LNF0 * l
+ rsc          = 0
+ rdc          = RDS0 + LRDS0 * l
+ shmod       =  1
+ rdsmod       = 1
+ rth0        =  0
+ tnom         = 22.0
+ tbar         = 19e-9
+ nf           = 2
+ lsg          = 2e-6
+ ldg          = 2.5e-6
+ epsilon      = 106.6e-12
+ ua           = 0
+ ub           = 0
+ vsat         = 100e+3
+ eta0         = 22.9e-3
+ vdscale      = 4
+ cdscd        = 0
+ lambda       = 0
+ vsataccs     = 100e+3
```

Specification of: parameter limits, optimizer boundaries and scaling for manual tuning.



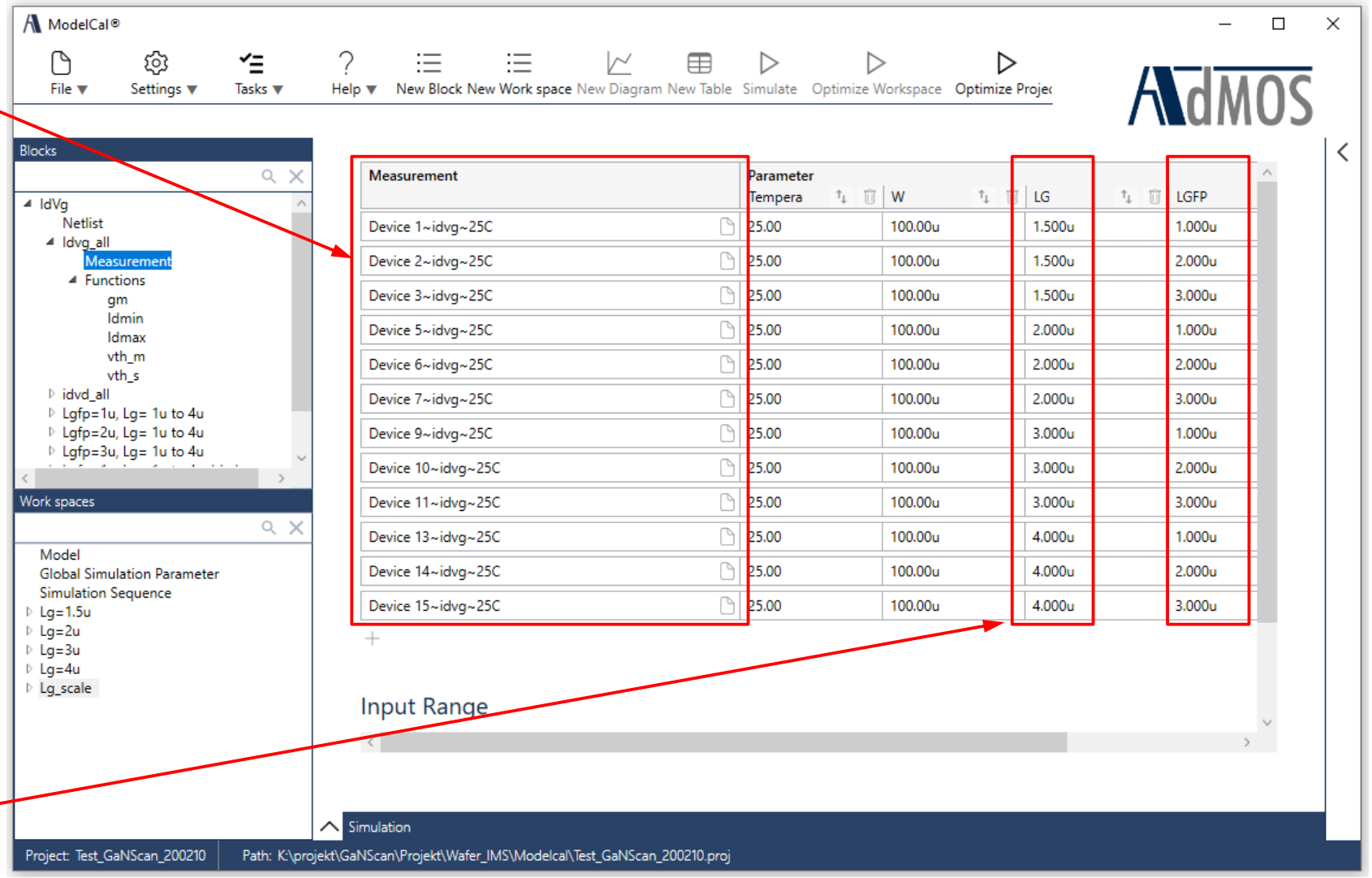
ModelCal: Data management

Data files of different transistors

Data handling capability:

- Data can be merged from different geometries or temperatures.
- Curves can be cut out of this data.

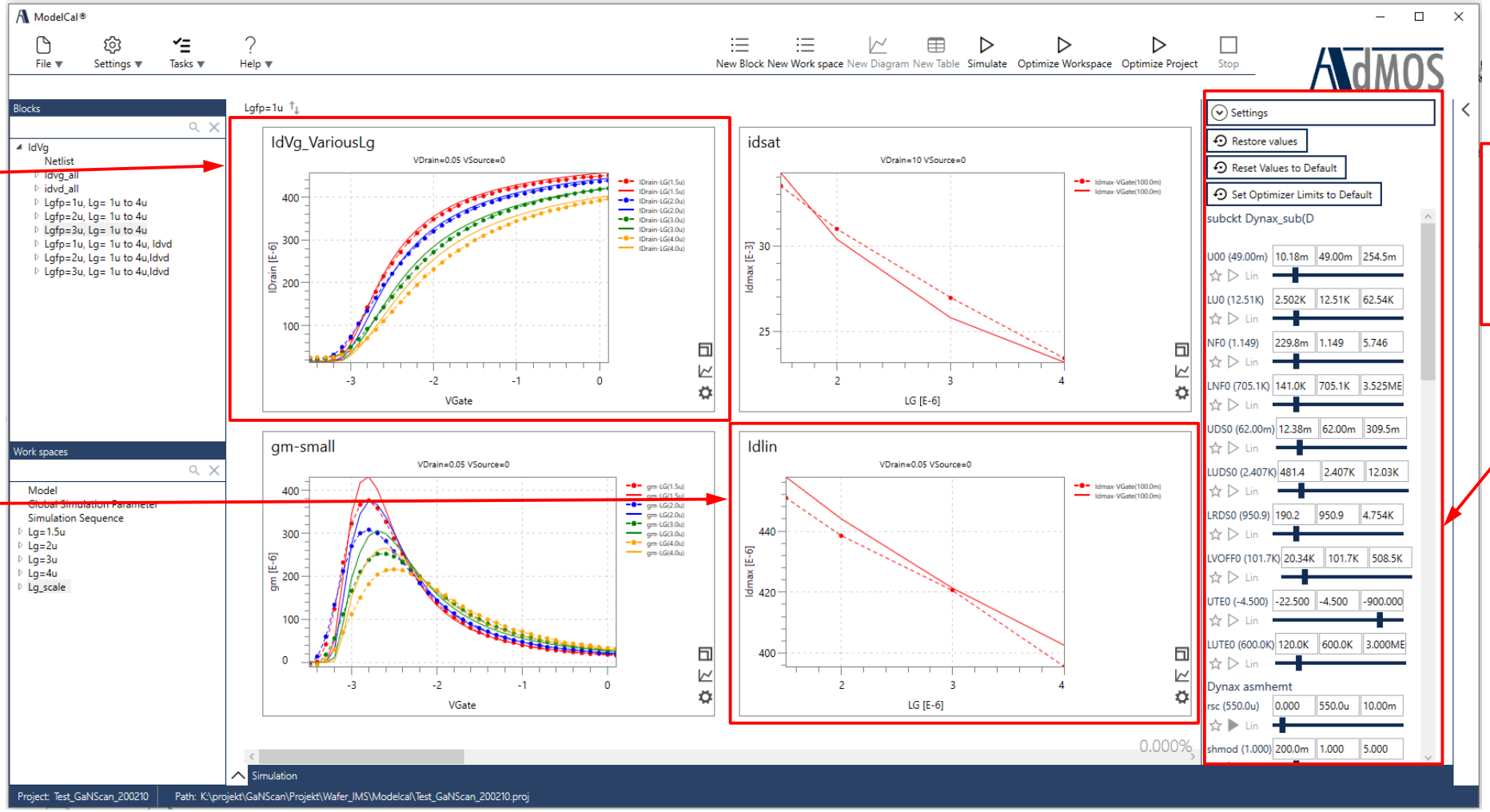
Different geometries (LG, LGFP)



ModelCal: Tuning / Optimisation

Automatic display of the curves of different transistors in one diagram

Scaling of parameters (Idsat) via geometry (LG)

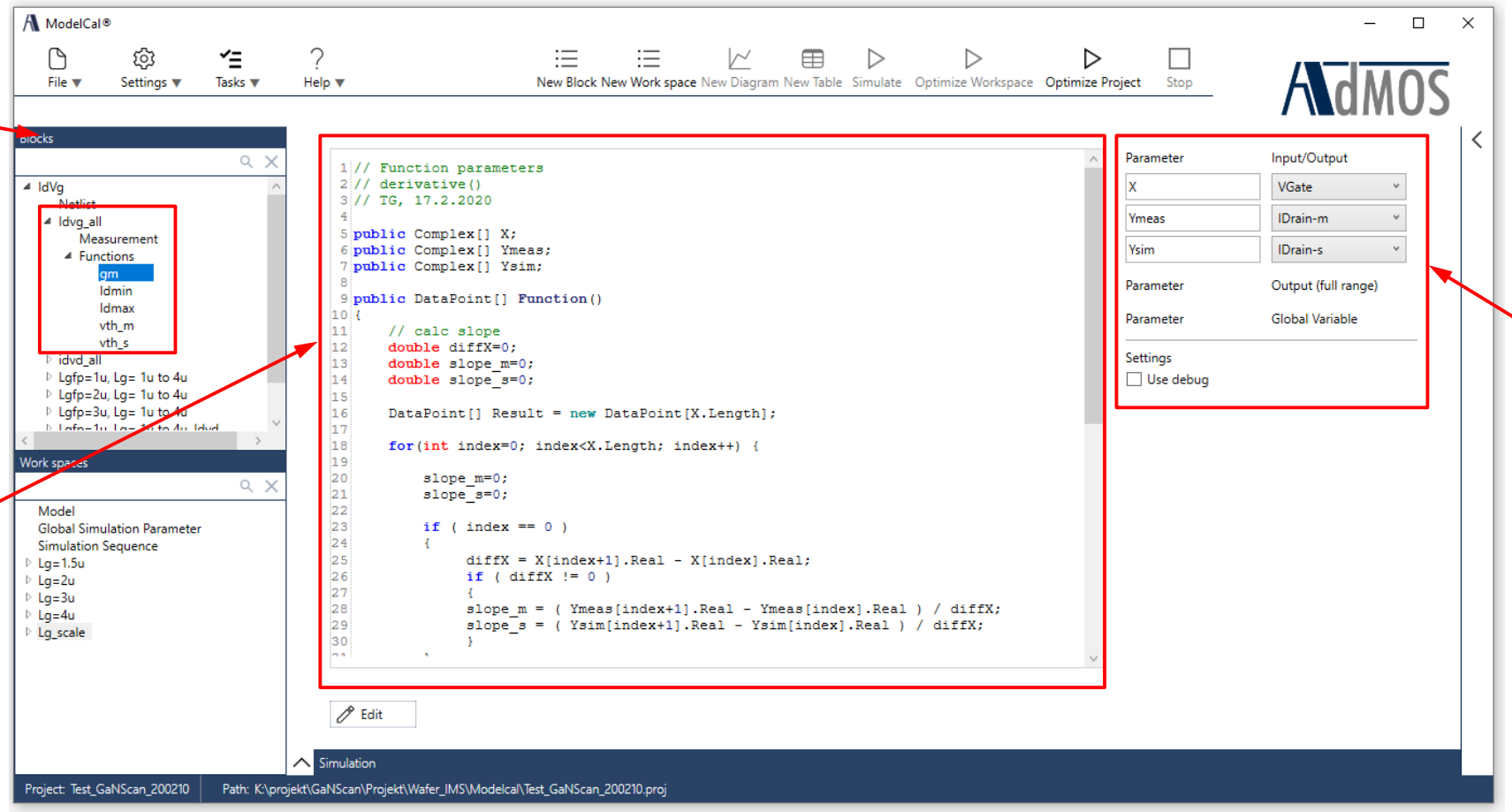


Control of the optimizer and manual tune function

ModelCal: User definied Functions

List of user-defined functions

C# code with own object definition for access to data



Simple definition of the transfer parameters

Summary

- GaNScan as a joint project between IMS Chips, Rood Microtec and AdMOS was presented.
- A test chip, the lab environment and process technology at IMS Chips were briefly introduced.
- AdMOS could gain a significant experience in both, measurement technologies and modeling principles for GaN devices.
- Three improvements for the ASM HEMT model were proposed to the model development team.
- A new software platform for parameter extraction was tested with the GaN devices.

References

[1] S. A. Albahrani, J. Hodges, L. Heuken, D. Schwantuschke, T. Gneiting, J. G. Burghartz and S. Khandelwal, “Validation of the Industry-Standard ASM-GaN Model for Gate-Length Scaling”, in Fourth Australian Microwave Symposium (AMS'20)

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