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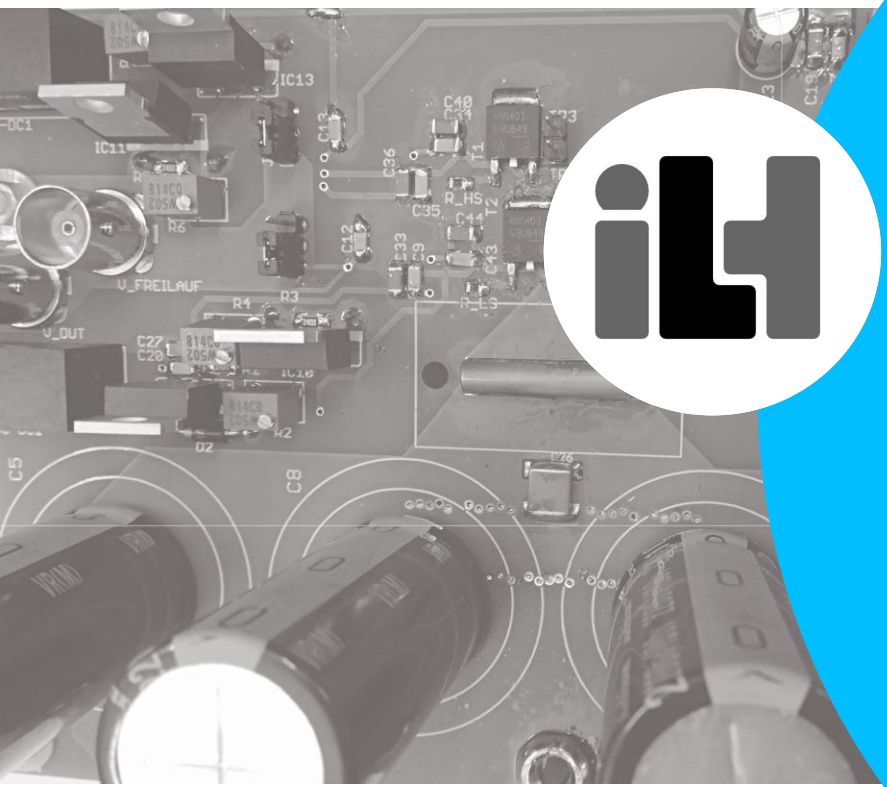


MOS-AK Workshop Sept 29.-Oct 1. 2020

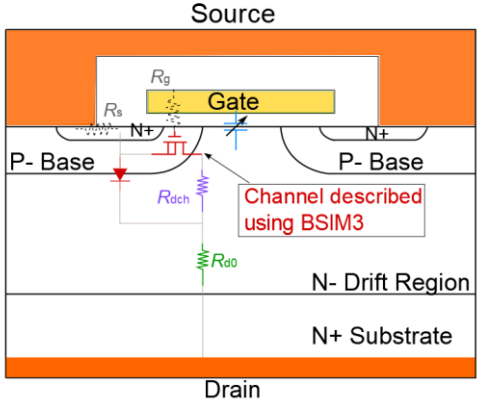
Adopting the industry-standard CMOS models for Si Vertical Power MOSFETs

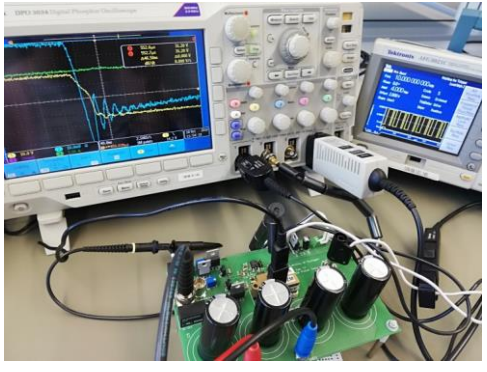
Lixi Yan, Ingmar Kallfass

29. Sept. 2020

Outline

- Background and Motivation
- Model Analysis
- Model description
  - IV characteristics
  - Capacitance model
  - Thermal model
- Parameter extraction
  - Device characterization
  - Parameter extraction result
  - Transient simulation
- Conclusion and Outlook





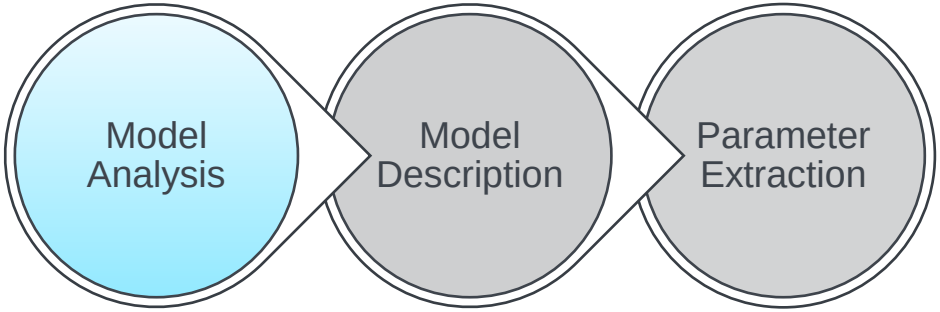
Background and Motivation

- Vertical power MOSFETs are widely used in switch mode power supplies which provide high power efficiency, but currently power MOSFETs lack the precise, robust and standardized compact models for circuit simulation.
- The custom models provided by device vendor often suffer from convergence problems and are often not compatible with all CAD simulation platforms.
- Operation conditions in switched-mode converters impose special requirements on model convergence.
- For CMOS logic devices, standard models exist, which proven to be accurate and robust.
- Conventional models cannot be directly applied to the specifics of vertical power MOSFETs.

[1]

Outline

- Background and Motivation



- Standard models overview
- Requirement Analysis

- IV characteristics
- CV characteristics
- Thermal model

- Device Characterization
- Parameter extraction result
- Transient simulation

- Conclusion and Outlook

Standard model overview

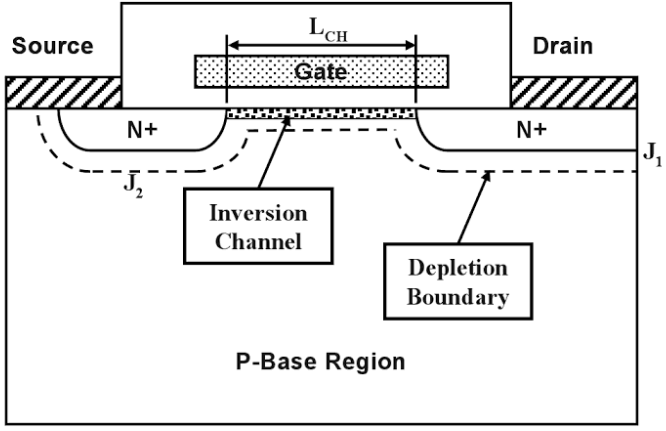
- BSIM3

- Published by the University of California at Berkeley
- Threshold based model
- Scalible with dependencies of important device dimensions and process parameters
- Public model
- Industry-standard MOSFET model
- Developed for deep-submicron digital and analog circuit designs

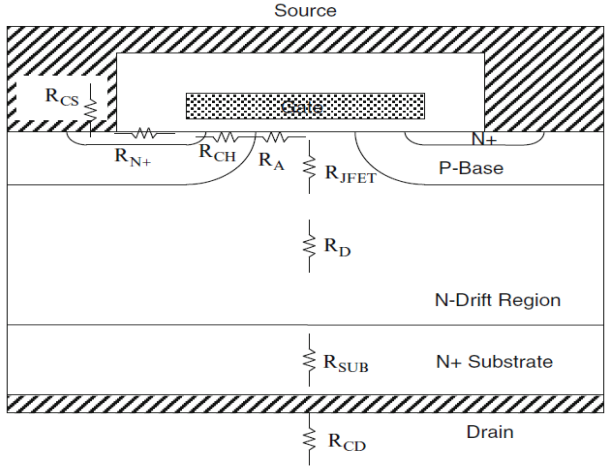
- EKV2.6

- Initialized by CEH (Centre Electronique Horloger, now CSEM) and EPFL
- Charge-based model
- Scalable compact model derived from fundamental physical properties of the MOS device structure.
- Available as in FOSS tool coded in Verilog-A
- De-facto MOSFET standard model
- Dedicated to the analog/RF IC designs using submicron CMOS technologies

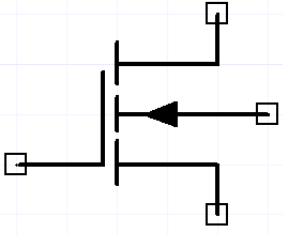
Power MOSFET Model Requirement



Lateral MOSFET structure



Power VD-MOSFET structure with internal resistance [2]

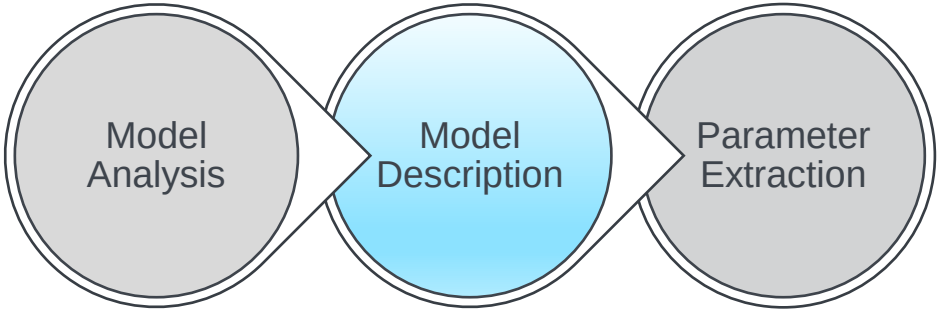


- Industry standard model
- Physics-Based derivation
- Unified I-V expression

- Some special extensional settings need to be developed considering the specific structure of power MOSFETs.
- Some standard model parameters need to be deactivated to account for the different behavior of power devices.
- The significant advantages for which standard models were designed should be preserved

Outline

- Background and Motivation



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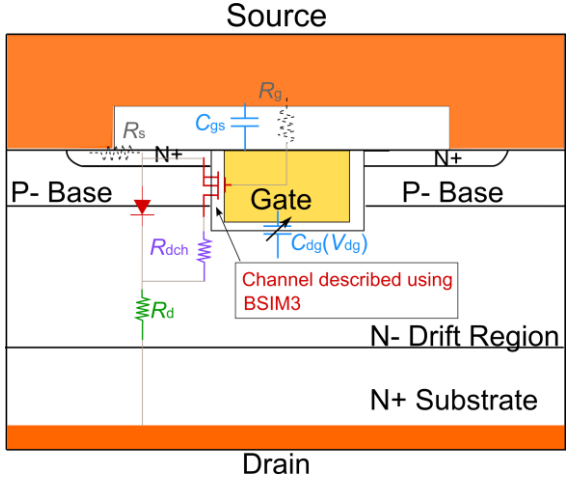
IV characteristics

Adopting BSIM 3 model



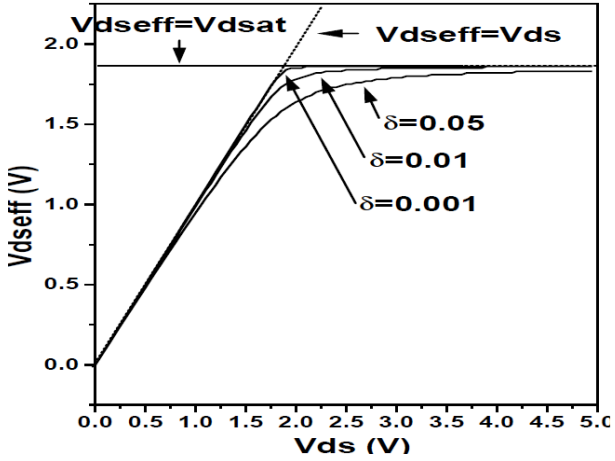
The structure of a vertical trench power MOSFET with the extended model structure [3]

- Considering the resistance coming from the drift region for the current going through the channel and via the junction can be different owing to their different current paths, an individual drift resistor R_{dbd} is defined for the body-diode which is different from the drift resistance R_{dch} for the channel current.
- The parameter extraction result shows that the individual drift resistance is able to describe the reverse current well.

- In BSIM3 a smoothing function Vdseff is used to link the linear region and saturation region with an extracted parameter δ.

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

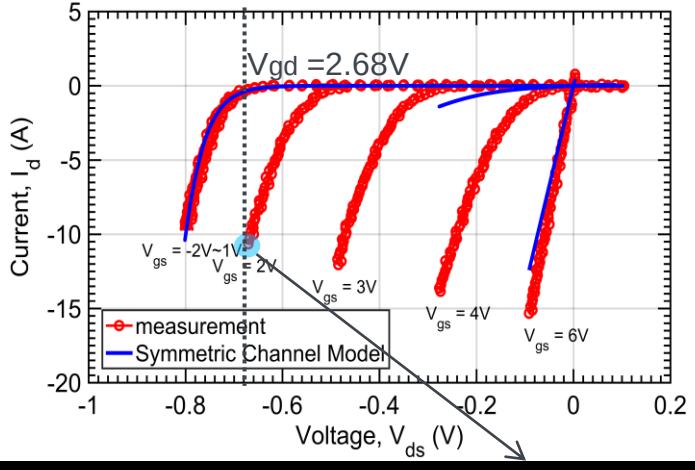
- When the value of δ increases, it is able to describe the drift resistance behavior of power devices.

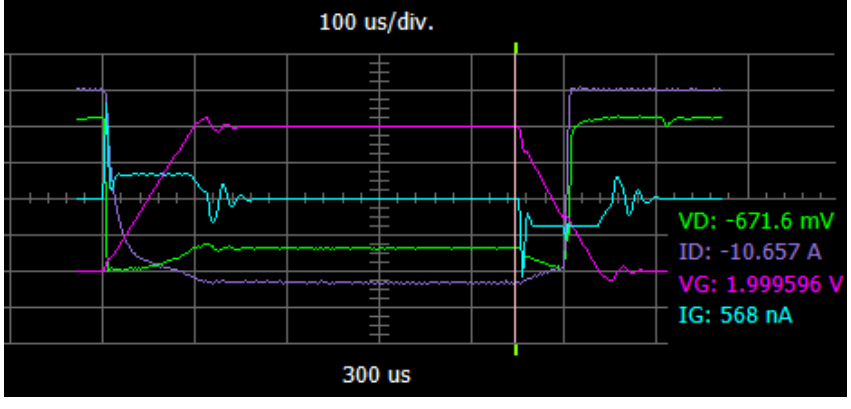


Effect of parameter δ [4]

IV characteristics in reverse operation

Adopting BSIM 3 model





- The body bias effects need to be defined in power MOSFET models

- Threshold voltage definition in BSIM3:

$$V_{bs}=0$$

In vertical structure

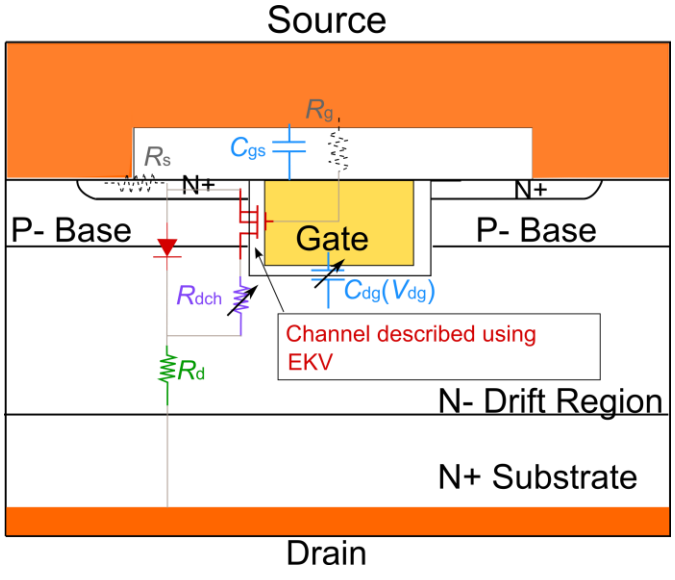
$$V_{th} = V_{th0} + k1\left(\sqrt{\Phi_S - V_{bs}} - \sqrt{\Phi_S}\right) - K_2 V_{bs}$$

Vds<0

$$V_{bs} => V_{bd} \qquad V_{bd} \neq 0$$

IV characteristics

Adopting EKV 2.6 model



The structure of a vertical trench power MOSFET with the extended EKV2.6 model structure

- For power MOSFETs, EKV 2.6 model is used to describe the intrinsic channel behavior. A drift resistance model simplified from the EKV-HV [5] model needs to be used for the nonlinear drift region.

$$R_{\text{drift}} = R_0 \cdot \left(1 + \left(\frac{V_{\text{drift}}}{VSAT}\right)^{\alpha_{vsat}}\right)$$

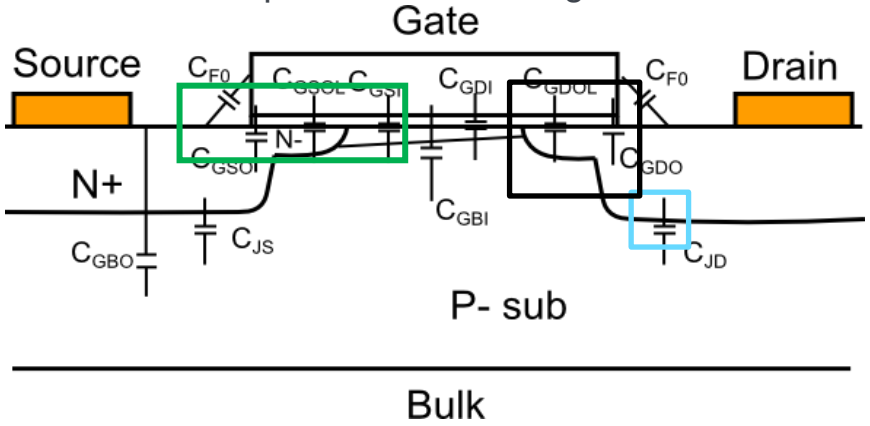
- This phenomenon can be described by using the body effect parameter GAMMA and the bulk Fermi potential PHI introduce the substrate potential effect on the threshold voltage in reverse operation.

$$VTH = \text{VTO}_a + \Delta V_{RSCE} + \gamma' \cdot \sqrt{V'_S} - \text{GAMMA}_a \cdot \sqrt{\text{PHI}}$$

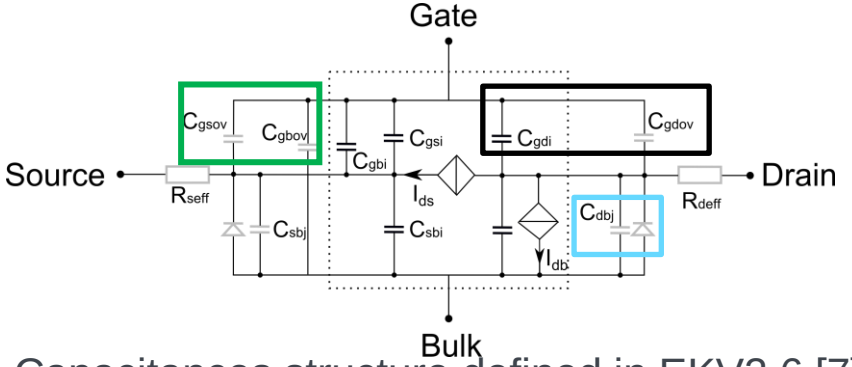
Capacitance model

CV characteristics

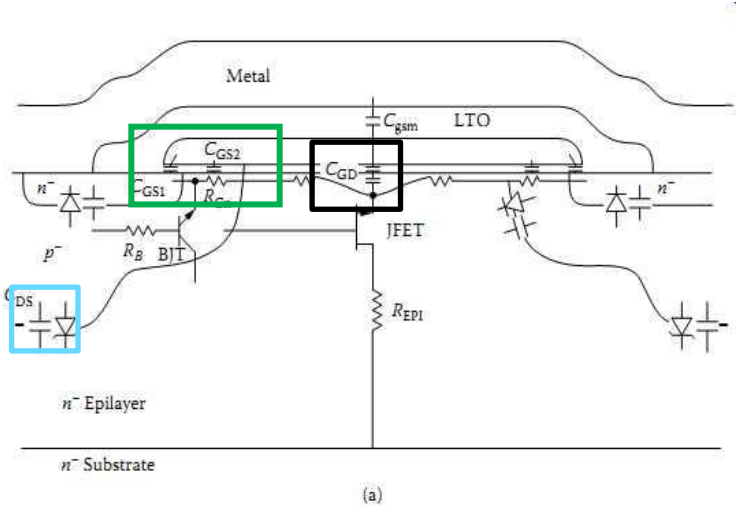
Parasitic capacitance modeling in BSIM3 and the structure in power MOSFET



Capacitances structure defined in BSIM3 [4]

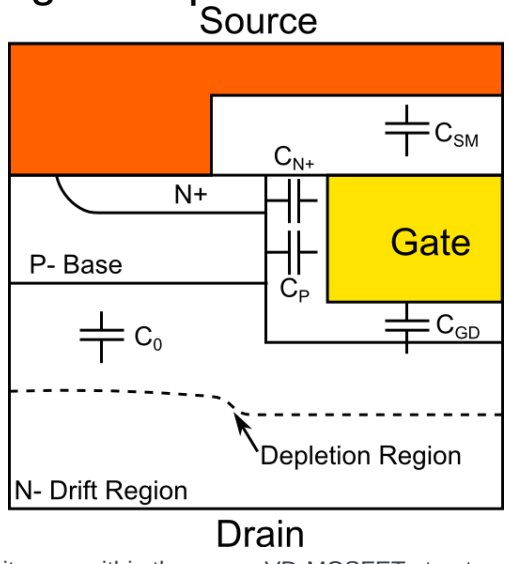


Capacitances structure defined in EKV2.6 [7]



Power MOSFET parasitic capacitance structure [6]

Drain-gate capaciatnce definition in power MOSFET

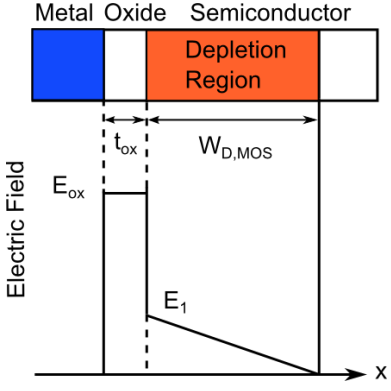


Capacitances within the power VD-MOSFET structure [2]

$$C_{GD,sp} = \frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}}$$

$C_{S,M}$: Semiconductor capacitance under the gate oxide, defined in series with the capacitor of the gate oxide.

$$C_{S,M} = \frac{\epsilon_S}{W_{D,MOS}}$$



Electric field profile for the MOS structure [2]

According to the relationship between the electrical field in semiconductor and depletion layer width[2], we have:

$$W_{D,MOS} = \frac{\epsilon_S}{C_{OX}}\left(\sqrt{1 + \frac{2V_D {C_{OX}}^2}{q\epsilon_S N_D}} - 1\right)$$

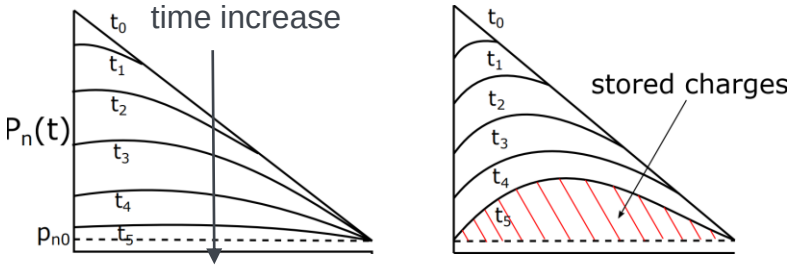
$$C_{GD} = C_{OX}\left(1 + \frac{2{C_{OX}}^2}{q\varepsilon_S N_D} \cdot V_D\right)^{-\frac{1}{2}}$$

$$C_{DG} = C_{OX}(1 + C_q \cdot (V_{DG} - V_{fb})^{Nc}$$

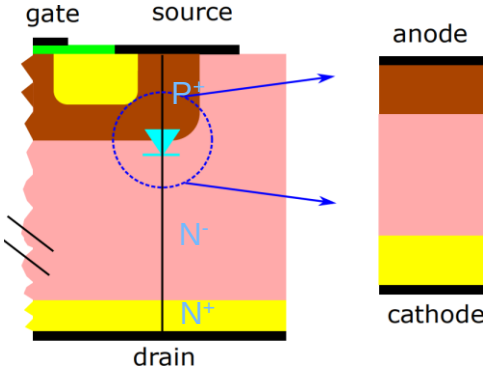
Transient model for Reverse Recovery of Body-diode

Diffusion capacitance defined by the stored charge model:

- Stored charge model is a simple lumped charge control model

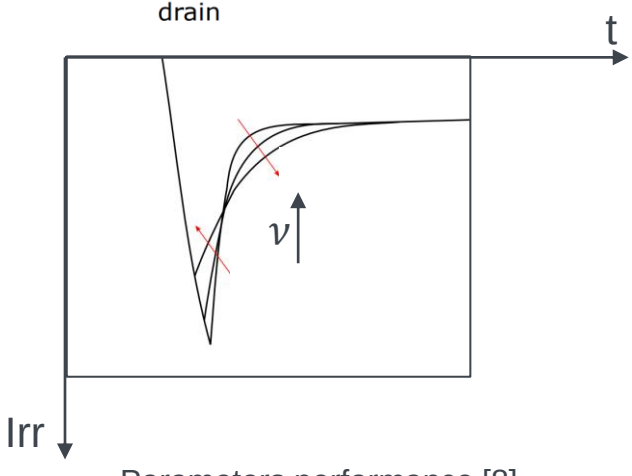


Carrier distribution profile changing with time [8]



$$Q = \tau \left[I_d - \nu \frac{dQ}{dt} \right]$$

$$I_d = \frac{Q}{\tau} + \nu \frac{dQ}{dt}$$



Parameters performance [8]

Thermal model

Temperature dependence defined in BSIM3 [4]

$$V_{th}(T) = V_{th}(T_{norm}) + \left(K_{T1} + \frac{K_{T1l}}{L_{eff}} + K_{T2} \cdot V_{bseff}\right)\left(\frac{T}{T_{norm}} - 1\right)$$

$$\mu_0(T) = \mu_0(T_{norm})\left(\frac{T}{T_{norm}}\right)^{\mu te}$$

$$U_a(T) = U_a(T_{norm}) + U_{a1}\left(\frac{T}{T_{norm}} - 1\right)$$

$$vsat(T) = vsat(T_{norm}) - A_T\left(\frac{T}{T_{norm}} - 1\right)$$

Temperature dependence defined in EKV 2.6 [9]

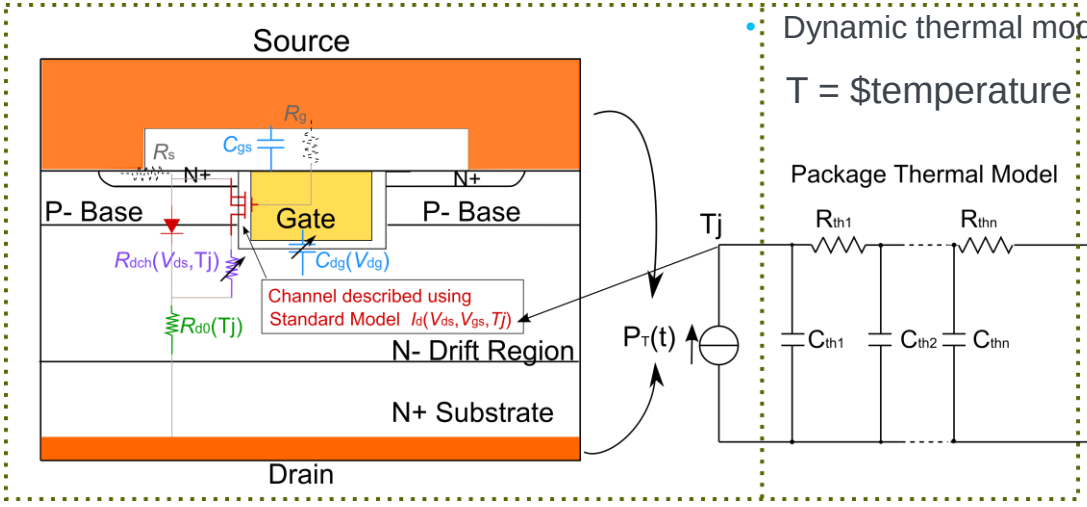
$$VTO(T) = VTO - TCV \cdot (T - T_{ref})$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{ref}}\right)^{BEX}$$

$$UCRIT(T) = UCRIT \cdot \left(\frac{T}{T_{ref}}\right)^{UCEX}$$

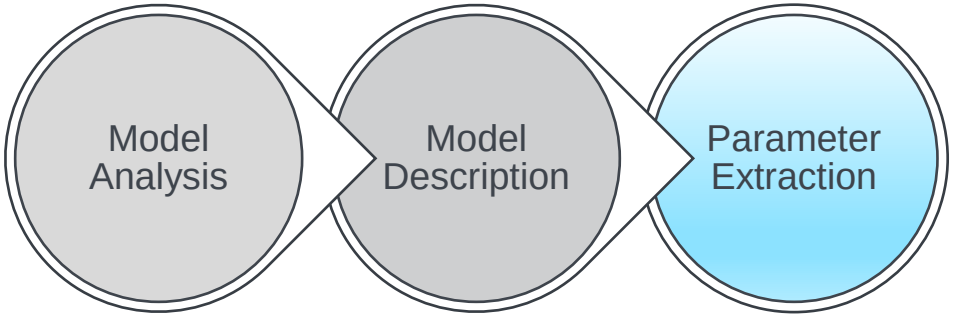
Temperature dependence for drift resistance [10]:

$$R_{drift}(T) = R_{drift}(T_0)[1 + \alpha(T - T_0) + \beta\,(T - T_0)^2]$$



Outline

- Background and Motivation

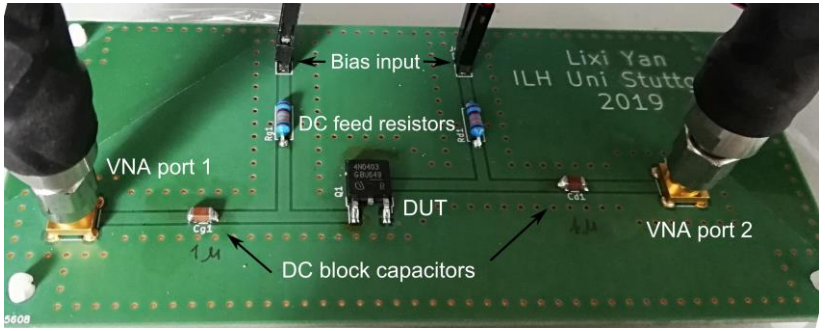


- Conclusion and Outlook

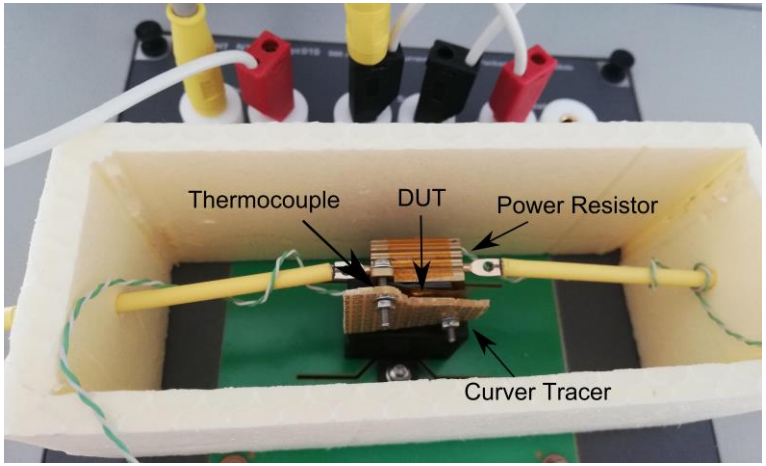
Device Characterization

Static IV and parasitic capacitance

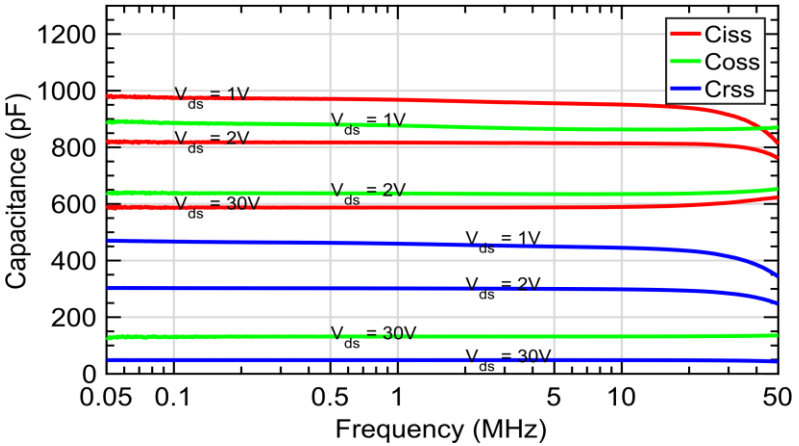
- The static IV characteristics are measured at different case temperature.
- Considering the frequency dependency, the 2-port S-Parameter measurement [11] is carried out for the capacitance measurement.



Measurement fixture with integrated bias tees



Static characterization at different case temperature setup

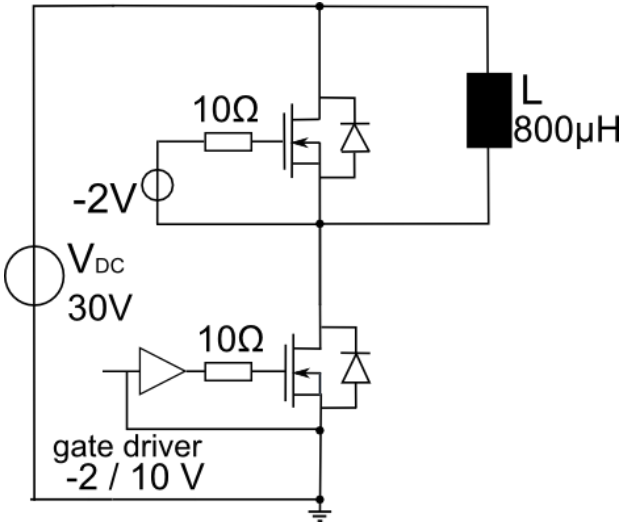


Measured capacitance vs frequency

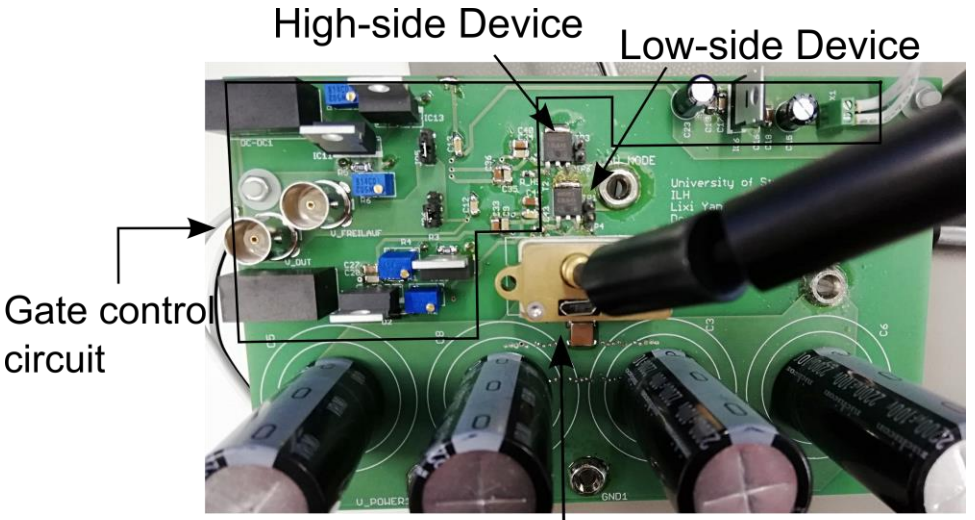
Device Characterization

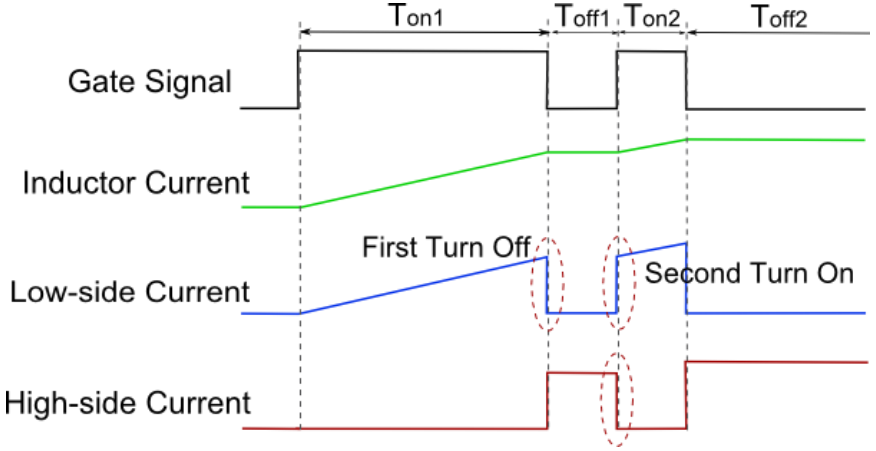
Transient Reverse Behavior

- Double pulse test to analyze the reverse recovery behavior of the device body diode



Sketch of the DPT measurement setup[12]

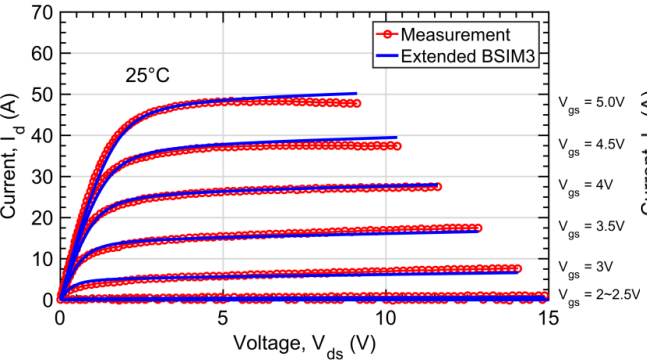


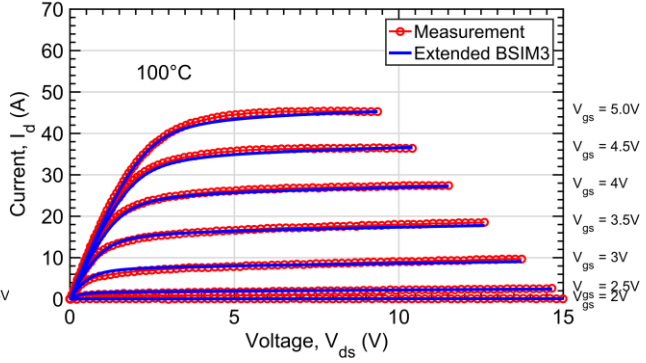


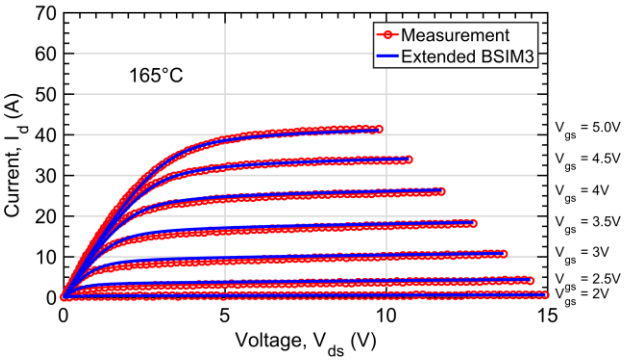
DPT waveform

IV Parameter extraction result

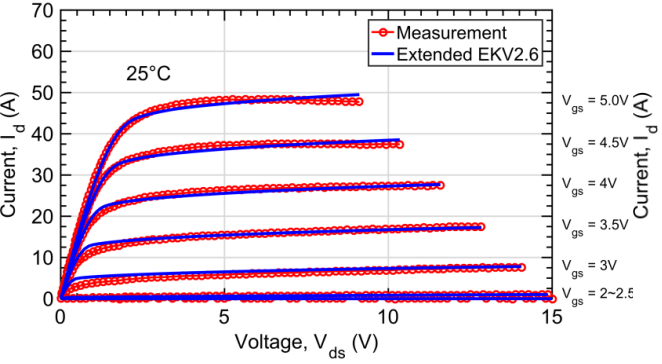
Adopting BSIM 3 for channel

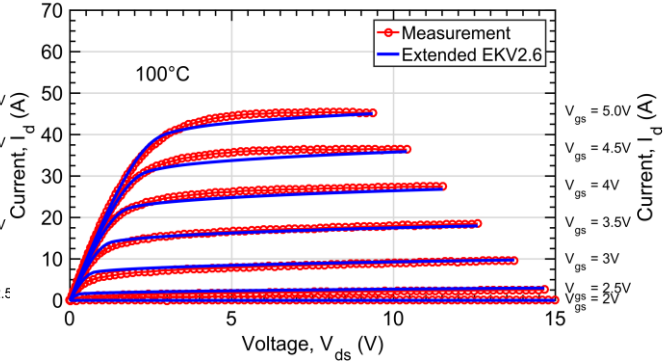


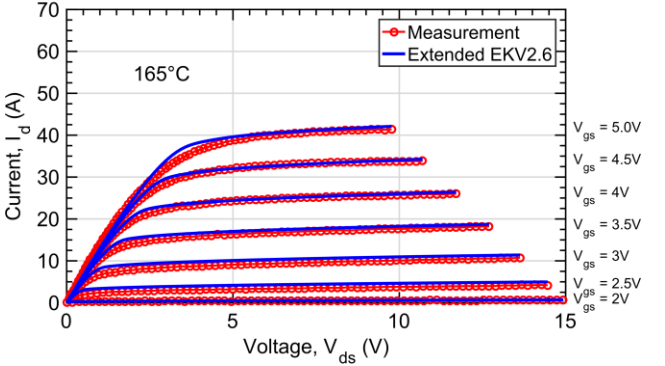




Adopting EKV 2.6 for channel

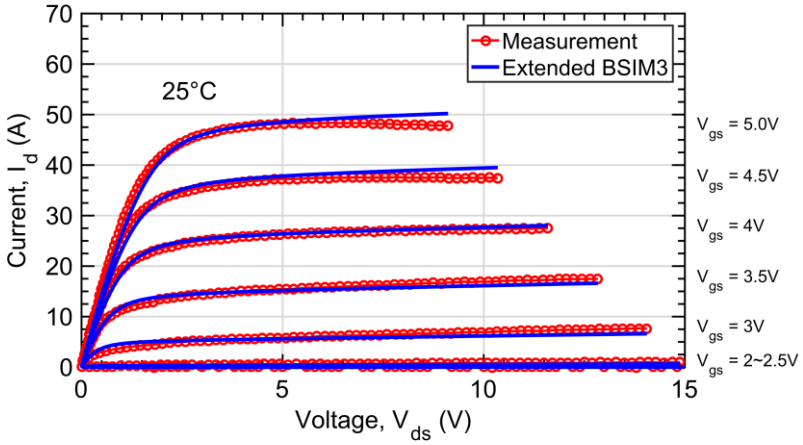


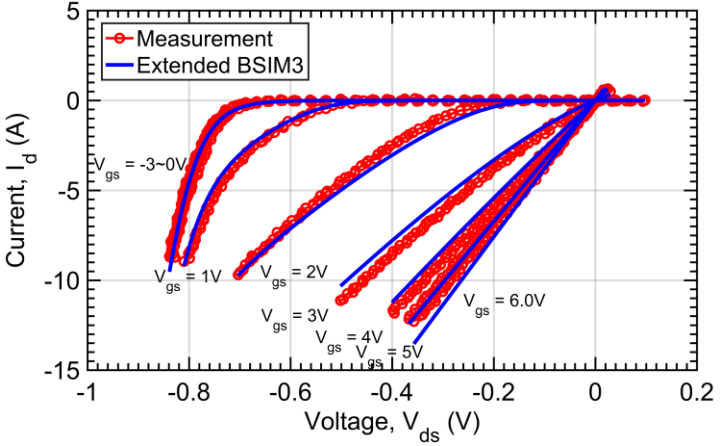


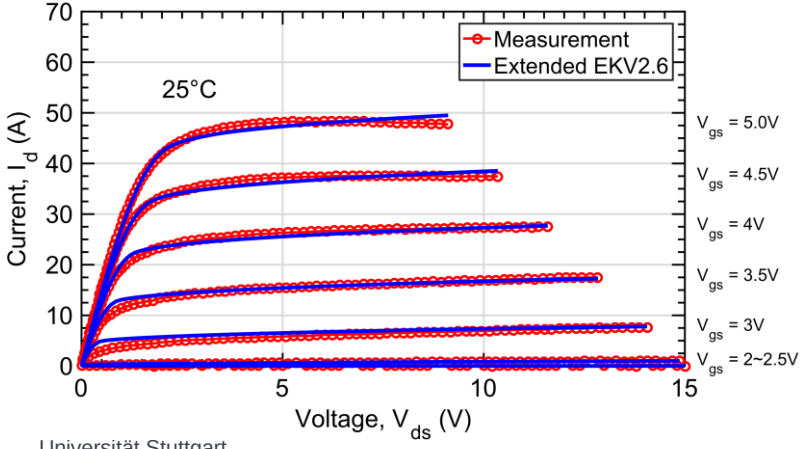


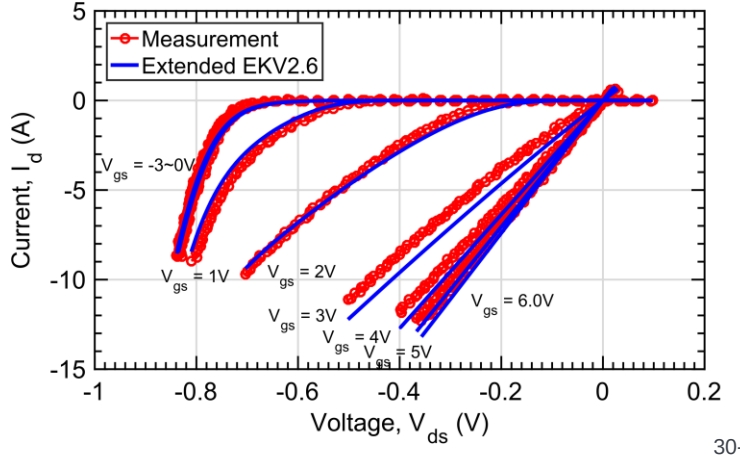
IV Parameter extraction result

The reverse IV parameters are also extracted, which involving the static diode model and the channel model considering body effect.



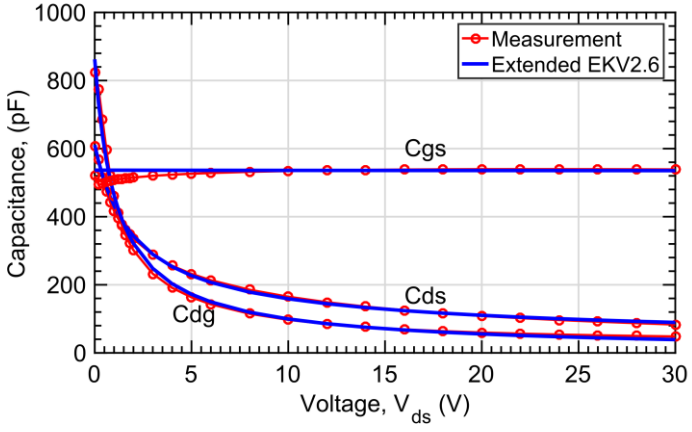




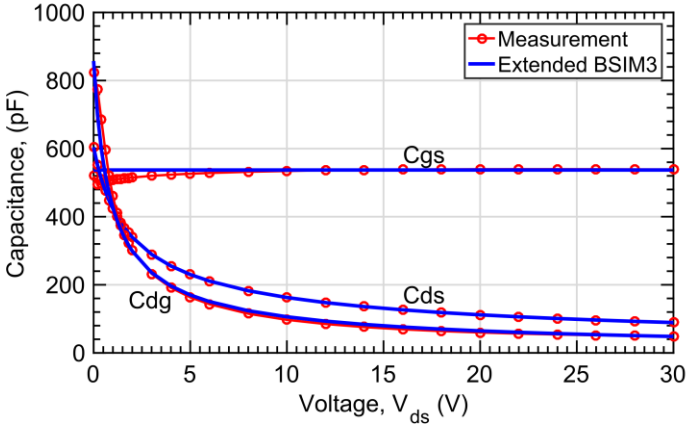


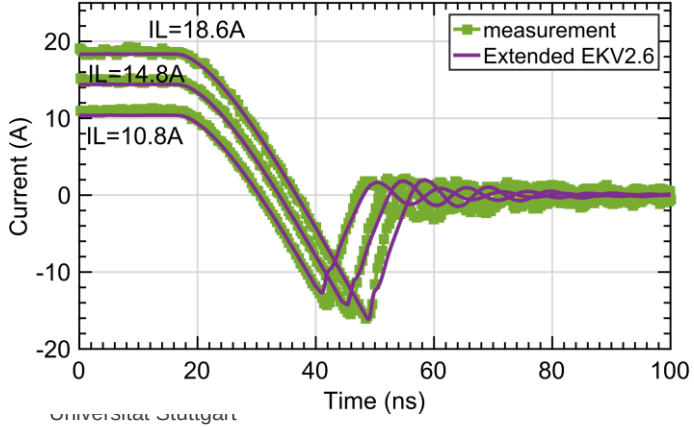
CV and reverse transient parameter extraction result

Extended EKV 2.6



Extended BSIM3





- The simulated capacitances at 1MHz are compared with the measurement with constant Vgs and sweeping Vds.
- The parameters of the diffusion capacitance model are extracted based on the DPT transient measurement at 10.8 A, 14.8 A, and 18.6 A forward current.

Standard model extension for power MOSFETs

Adopting BSIM 3 and EKV 2.6

Extension requirement	BSIM 3	EKV 2.6
Drift resistance	A constant resistor	A voltage dependent resistor
Overlap capacitance	Cgd	Cgs, Cgd, Cds
Body-diode	Diffusion capacitance for RR	Static definition Diffusion capacitance for RR
Thermal	Dynamic setup	Dynamic setup

Number of extracted parameters	**41**	**24**

Conclusion and Outlook

- The industry-standard models BSIM 3 and EKV 2.6 are able to be adopted with dedicated extensions to describe vertical structure Si power MOSFETs.
- In terms of the drift resistance, parasitic capacitance and reverse transient behavior of power MOSFETs , the proposed extended models are able to describe the device performance precisely.
- According to different definitions of the core model, different extension strategies need to be used. They can be appropriately applied considering the particular application conditions and requirements.
- The model can be improved to describe the Vgs dependent capacitance for a more precise description of the dynamic behavior.
- The model can be further modified to apply to a wider range of power MOSFETs e.g Super-junction devices, SiC power MOSFETs etc.

Reference

- [1] https://economictimes.indiatimes.com/news/international/business/the-18-billion-electric-car-bubble-is-in-danger-of-bursting-in-china/articleshow/68898218.cms
- [2] B. Jayant Baliga, “Power Semiconductor Devices” PWS Publishing Company, 1996.
- [3] L. Yan and I. Kallfass, "Adopting the BSIM3 Model to Describe the DC-IV Characteristics of a Vertical Power MOSFET," 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, 2018, pp. 1-6
- [4] Y. Cheng, C. Hu, MOSFET Modeling & BSIM3 User's Guide, Kluwer Academic Publisher, 1999.
- [5] Y. S. Chauhan, F. Krummenacher, and A. M. Ionescu, Modeling of High Voltage MOSFETs Based on EKV (HV-EKV). Dordrecht: Springer Netherlands, 2010, pp. 95–127.
- [6] http://www.industrial-electronics.com/DC_pwr_3b.html
- [7] W. Grabinski *et al*., "FOSS EKV2.6 Verilog-A Compact MOSFET Model," *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Cracow, Poland, 2019, pp. 190-193..
- [8] K. J. Tseng and S. Pan, "Modified charge-control equation for simulation of diode reverse recovery," in Electronics Letters, vol. 32, no. 4, pp. 404-, 15 Feb. 1996.
- [9] M. Bucher, C. Lallement, C. Enz, F. Théodoloz and F. Krummenacher, "The EPFL-EKV MOSFET model equations for simulation Version 2.6", *Technical Report Electronics Laboratory*, June 1997, [online] Available: https://ekv.epfl.ch/wp-content/uploads/2019/02/ekv_v262.pdf.
- [10] F. Kerrour, A. Boukabache and P. Pons, "Modelling of Thermal Behavior N-Doped Silicon Resistor," *Journal of Sensor Technology*, Vol. 2 No. 3, 2012, pp. 132-137
- [11] C. Salcines, Y. Pathak and I. Kallfass, ”Characterization of power transistors intrinsic parasitics based on 2-Port S-parameter measurements,” 2017 19th European Conference on Power Electronics and Applications, Warsaw, 2017, pp. P.1-P.6
- [12] L. Yan, T. Li, and I. Kallfass, “Characterization and modeling of the reverse behavior of a vertical power MOSFET,” Microwave and Optical Technology Letters. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/mop.32119

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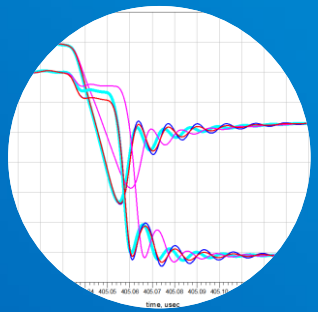
Thank you!



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