# Design-oriented compact model for FinFET


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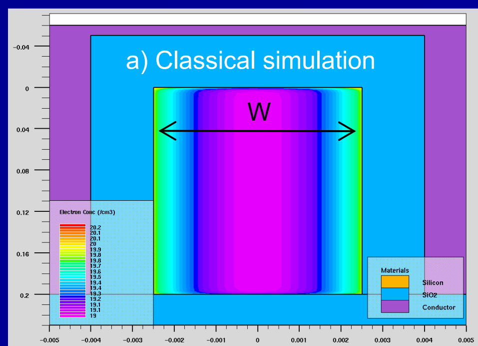
## Model characteristics (v1.1)

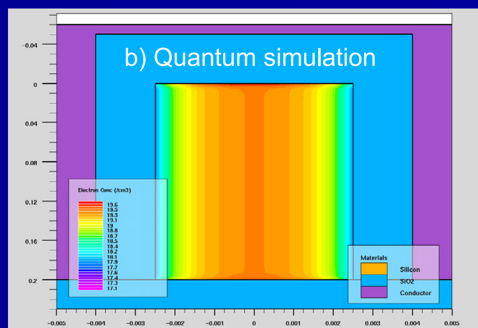
- Explicit compact model for both undoped FinFET and symmetric DG MOSFET.
- Charge-based model relying on a robust algorithm dedicated to circuit design and simulation [1-3].
- Modeling of both static and dynamic modes of operation.
- Short-channel effects such as roll-off, DIBL, subthreshold slope degradation and mobility degradation are taken into account down to 60 nm of channel length [4].
- Model validated with respect to 2D and 3D simulations (Atlas) for DG MOSFET and FinFET, respectively.

## 3D FinFET simulations

### Technological parameters

- Gate length (L) : 1 µm → 25 nm
- Fin width (W) : 50 nm → 3 nm (i.e. $t_{si}$ for DG MOSFET)
- Fin height (H) : 1 µm → 20 nm
- Gate oxide thickness ($T_{ox}$) : 1.5 nm
- Channel doping ($N_{ch}$) : $5{\times}10^{14}$ cm$^{-3}$
- Source-drain doping ($N_{sd}$) : $5{\times}10^{21}$ cm$^{-3}$

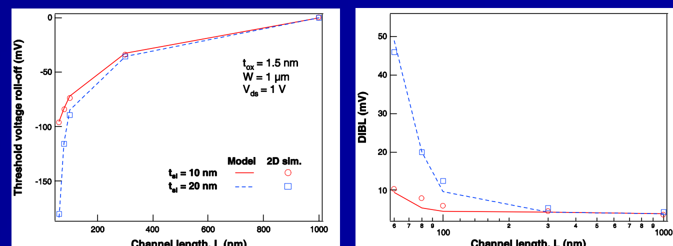


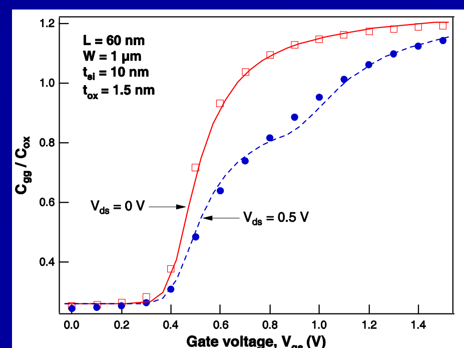

*Transverse cross section of a device with a Fin width of 5 nm showing the electron concentration in the channel. Quantum effects (Fig. b) significantly alter the electrical characteristics for W < 10 nm and thus must be accounted for in FinFET compact models.*

## Model results

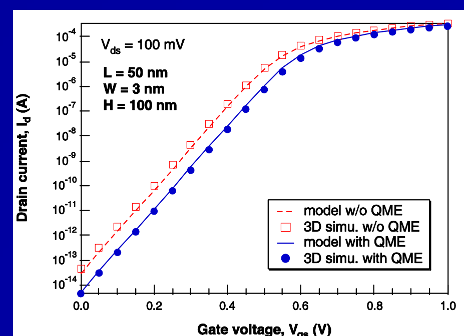
➔ Roll-off and DIBL for the DG MOSFET as a function of channel length. For all graphs: Model = lines; 2D/3D simulations = markers.




➔ Normalized gate transcapacitance for a 60 nm DG MOSFET.




➔ Drain current of FinFET showing the influence of quantum mechanical effects (QME).




## Forthcoming model (v1.2)

Additional physical effects to be included in the v1.2 model :

- Quantum-mechanical effects (under validation)
- Channel length modulation and saturation voltage
- Overlap capacitance and series resistance

Study in progress with 3D TCAD simulator :

- 3D effects such as corner effect


[1] F. Prégaldiny *et al.*, *Int. J. Numer. Modelling*, vol. 19, pp. 239-256, 2006.
[2] J.-M. Sallese *et al.*, *Solid-State Electronics*, vol. 49, pp. 485-489, 2005.
[3] F. Prégaldiny *et al.*, *in Proc. Nanotech 2006, WCM*, pp. 686-691, invited paper.
[4] B. Diagne, F. Prégaldiny *et al.*, *Solid-State Electronics*, vol. 52, pp. 99-106, 2008.



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