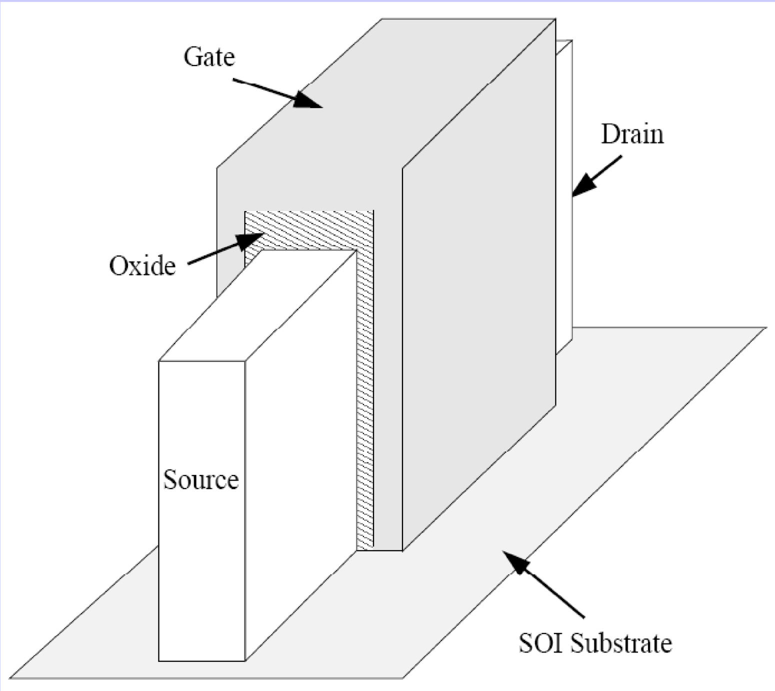
Compact Modeling of Nanoscale Multiple-Gate FETs

[a]Alexander Kloes, [a,b]Michaela Weidemann

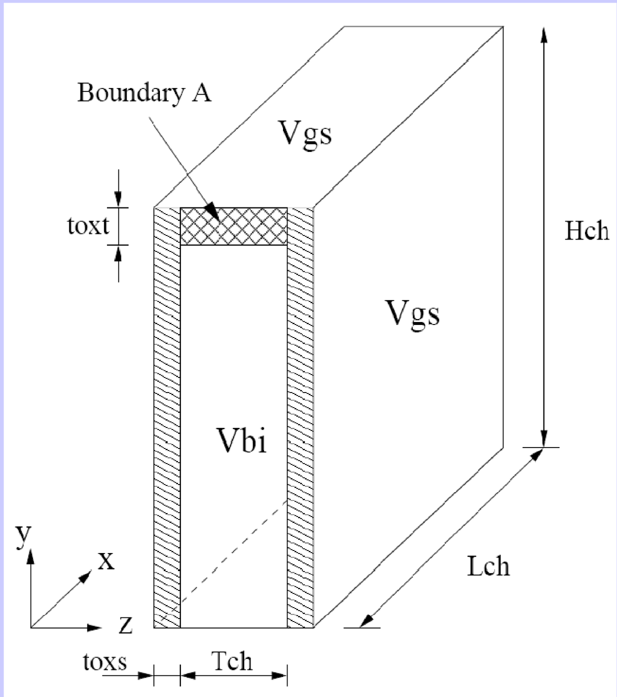
[a] University of Applied Sciences Giessen-Friedberg, Germany

[b] Universitat Rovira i Virgili, Spanien

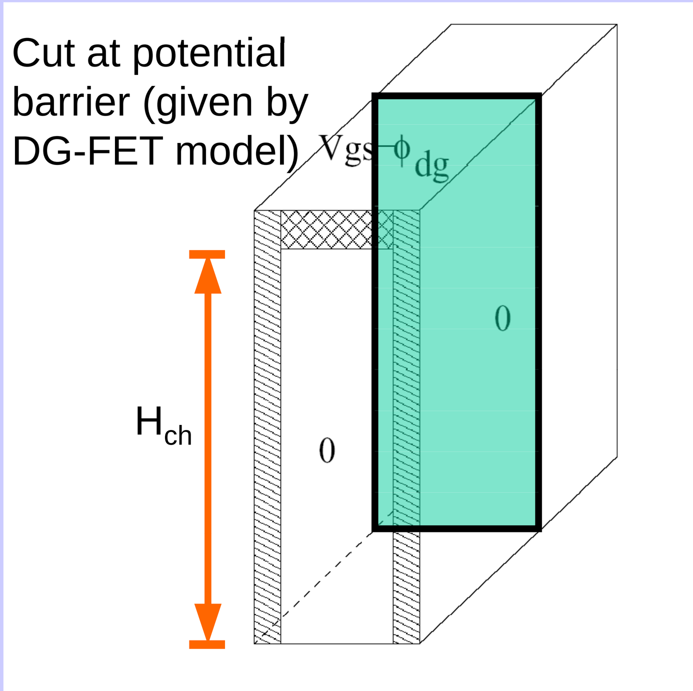
Approach: Reducing 3D potential problem to 2D $\Delta\varphi(x,y,z)=0 \rightarrow \Delta\varphi(y',z)=0$



FinFET on SOI Substrate



Boundary for 3D Laplace

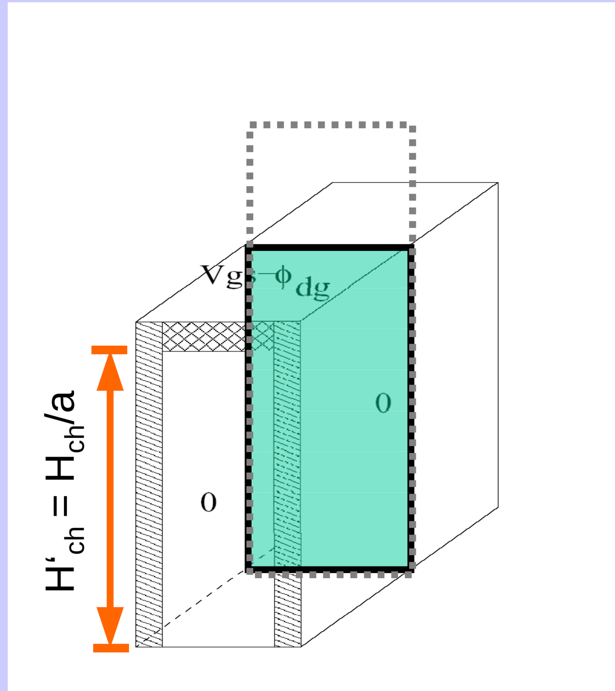


Transformed boundaries

Scaling vertically:

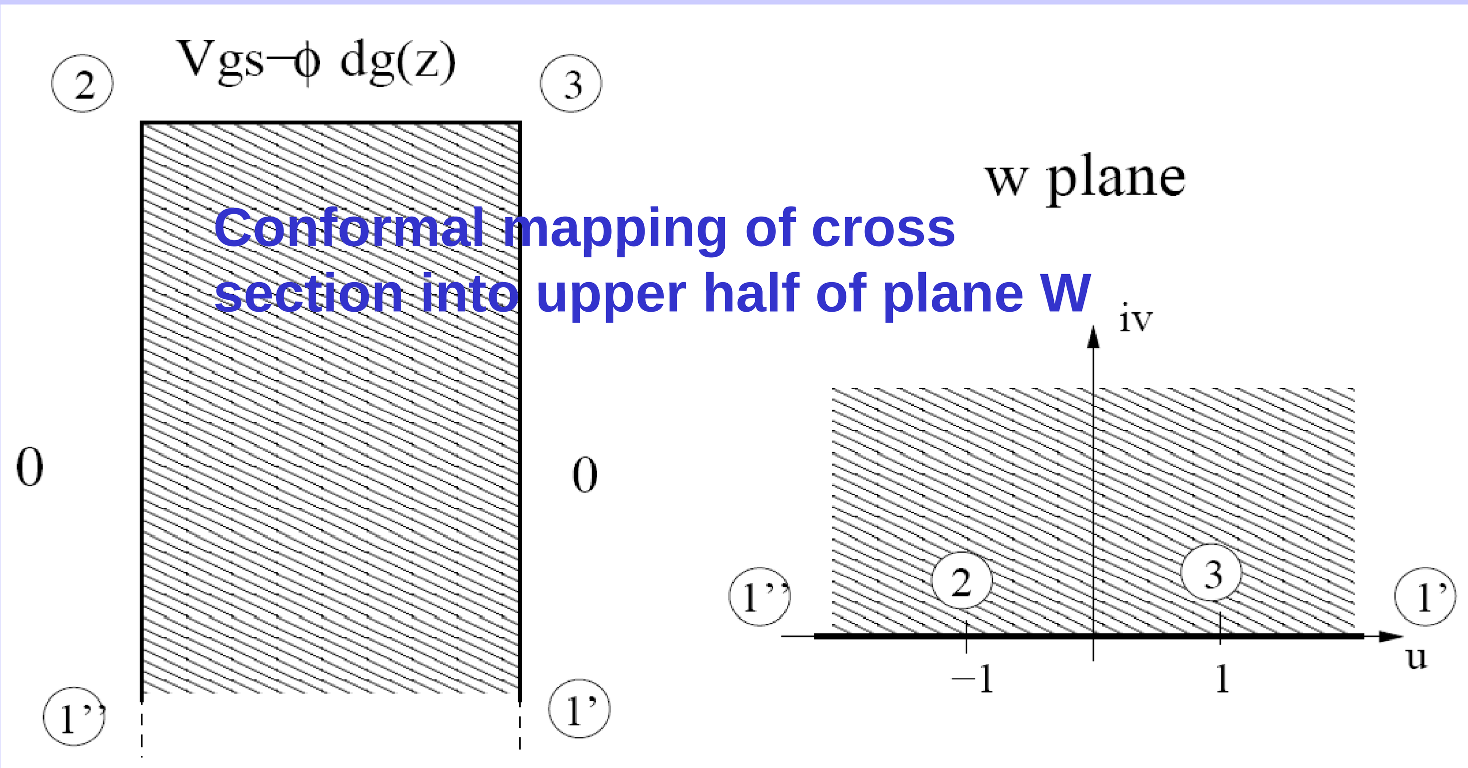
$y' = y / a$

Parameter a is derived from boundary conditions

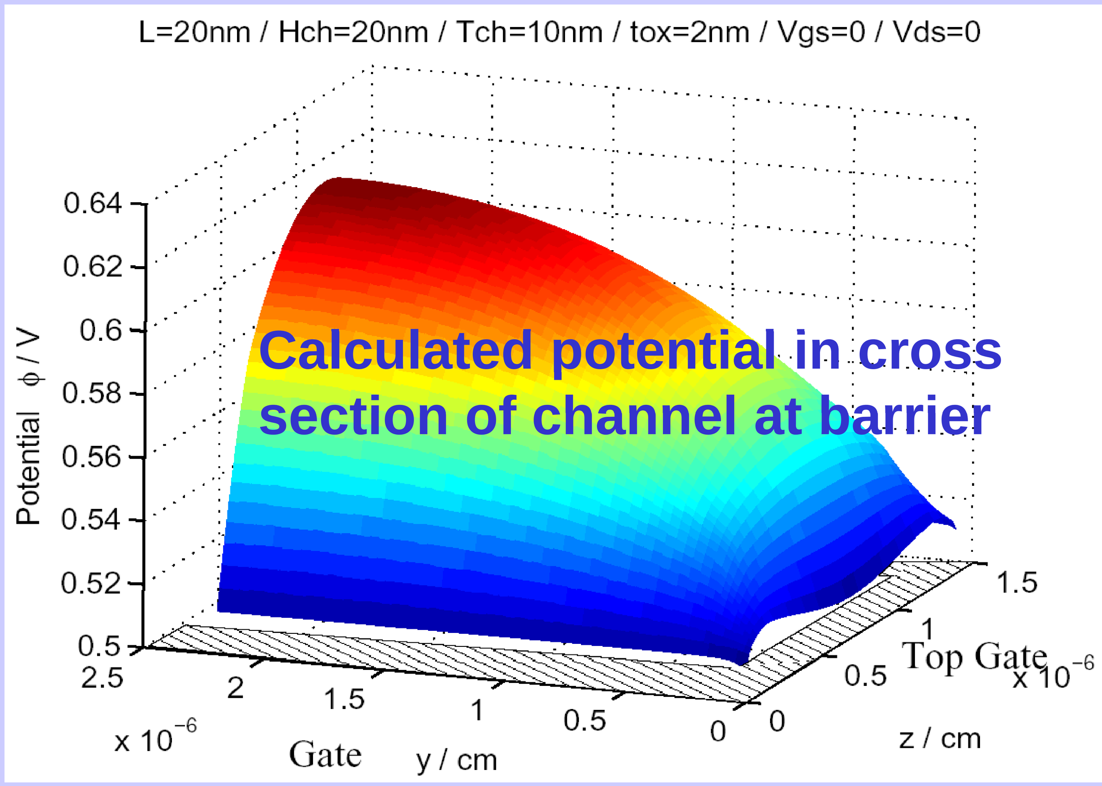


2D Laplacian

Analytically solving for potential at barrier by conformal mapping:

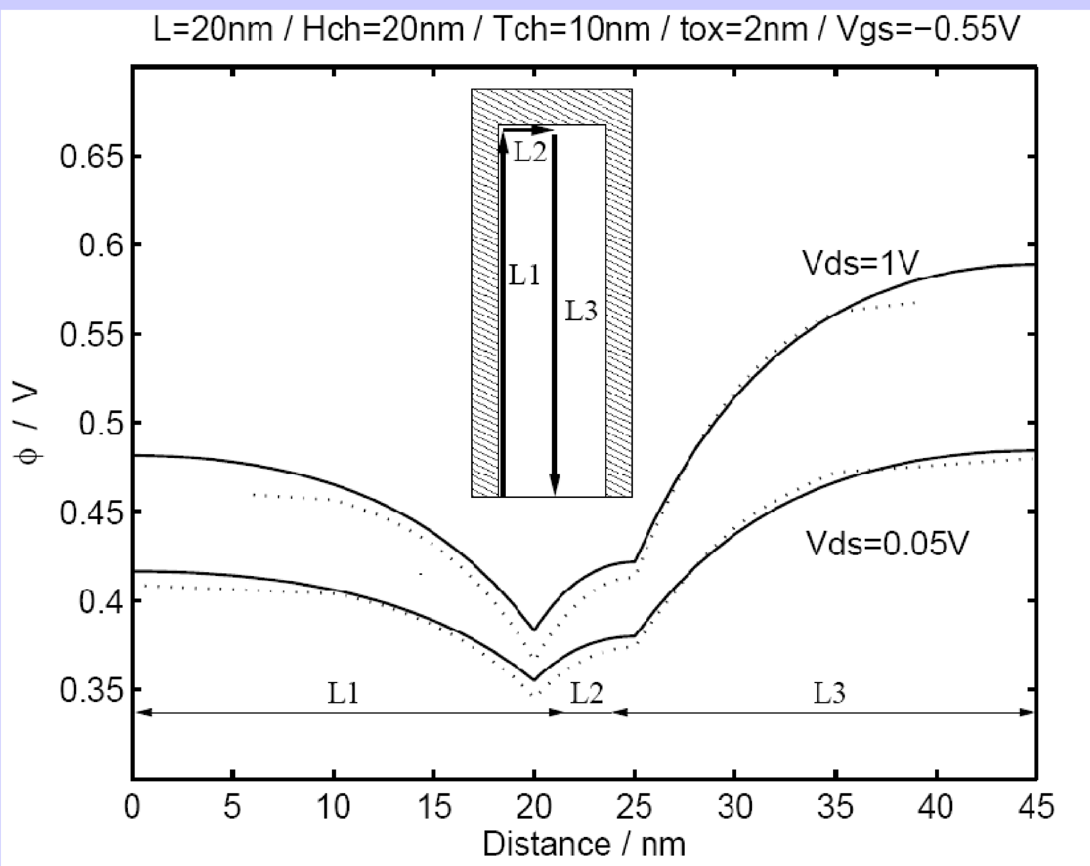


- Analytical solution of 3D Poisson's equation at potential barrier
- Conformal mapping technique results in closed-form equations

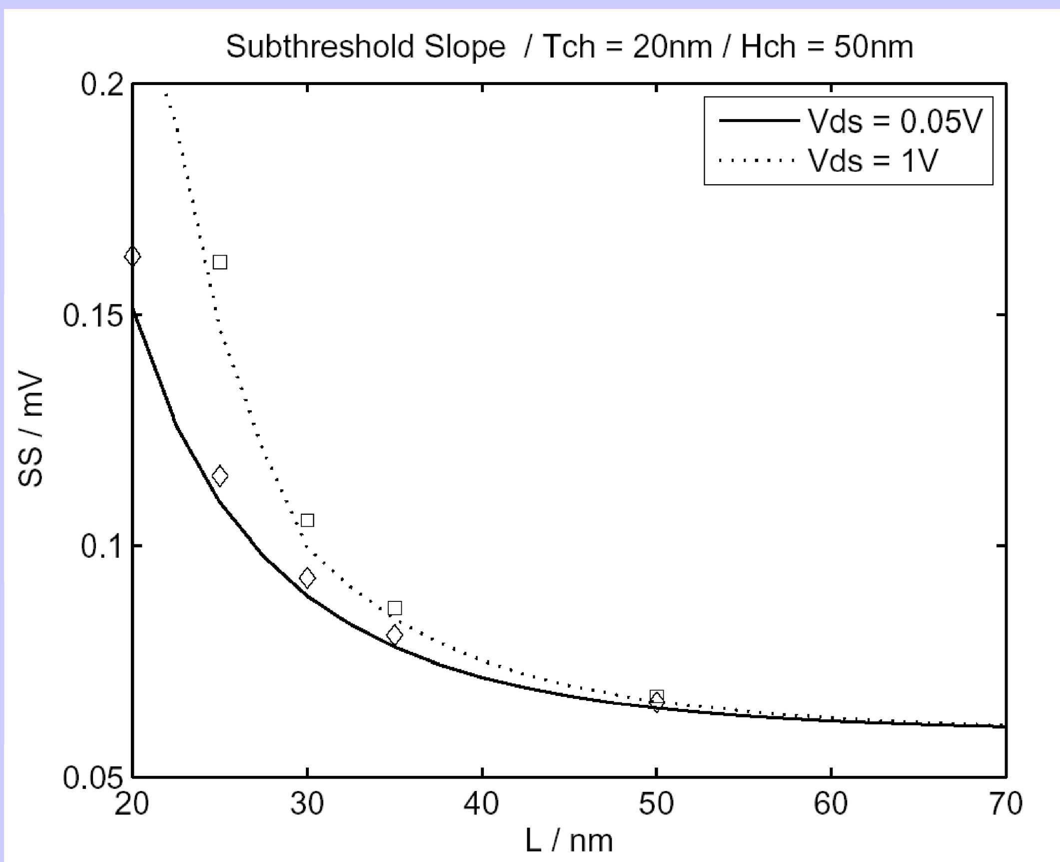


Results compared to numerical device simulations

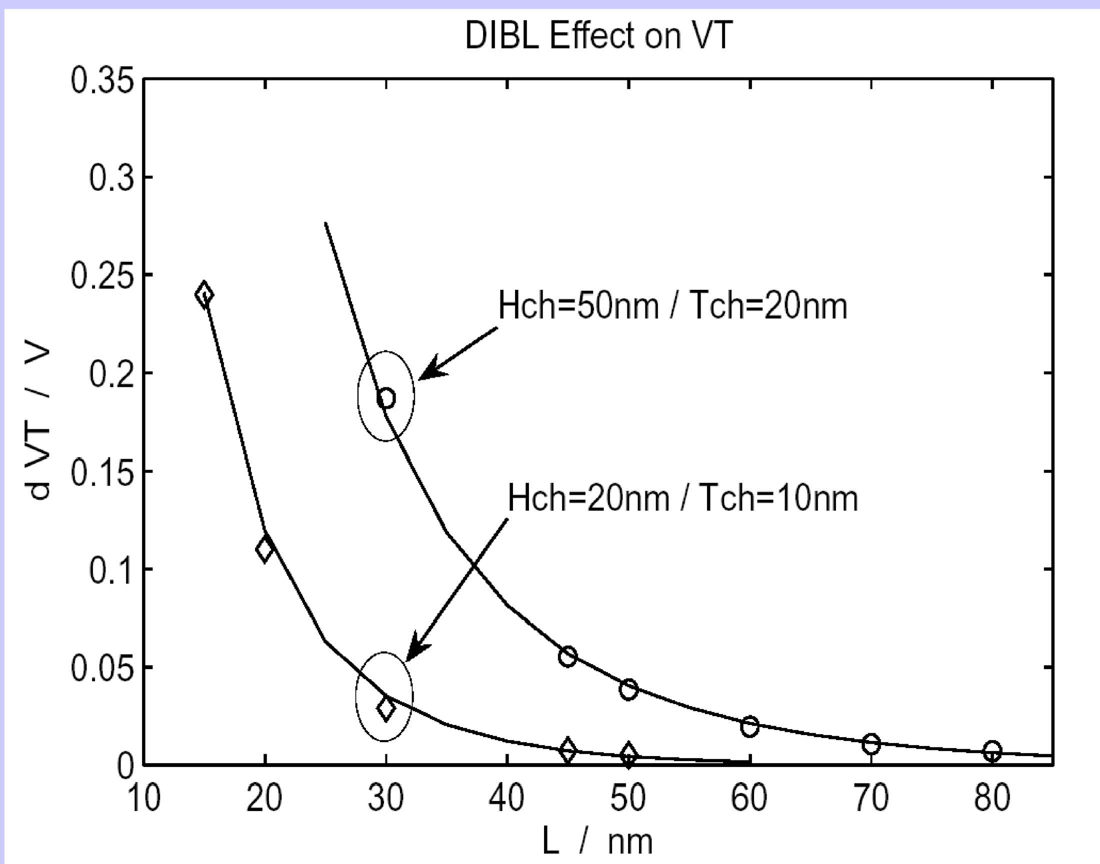
- Closed-form model equations for subthreshold slope and threshold voltage have been derived
- Since no unphysical fitting parameters are introduced the model offers a highly predictive ability
- Comparison with 3D numerical device simulations (Sentaurus) confirms accuracy of modeling approach



Potential along defined trace in cross section
(Lines: model, dashed lines: Sentaurus)



Sth slope vs. effective channel length
(Lines: model, symbols: Sentaurus)



Threshold voltage vs. effective channel length
(Lines: model, symbols: Sentaurus)

Partners:

- COMON (Compact Modelling Network) EU FP7 IAPP
- Universitat Rovira i Virgili (Spanien)
- University Graduate Center Kjeller (Norwegen)

Funding:

- 2006 – 2009: German Federal Ministry of Education and Research (contract no. 1764X06, AiF FH³)