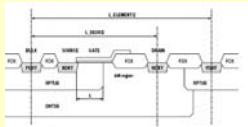


LD-MOS modeling in HV- CMOS Process - Ehrenfried Seebacher, Werner Posch, Biswanath Senapati, Kund Molnar and Alexander Steinmair

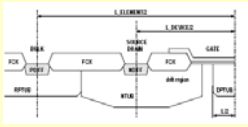
LD- MOS Transistor Modeling

Abstract: In this poster we present highly accurate High Voltage LDMOS-transistor models for analog applications. Special sub-circuits are demonstrated in order to model symmetrical and unsymmetrical N- and P- LDMOS transistors with emphasis on modeling of on resistor (RON), quasi saturation effects, body currents and parasitic diode/bipolar effects in addition to the standard MOS effects. The high flexibility of the sub-circuits allows individual configurations for all kind of LDMOS transistors. The paper shows different implementations of the parasitic behavior with diodes or BJTs for length and width scalable isolated and non isolated n- and p- channel HV transistors.

Isolated HV- NMOS Transistor



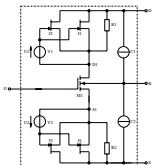
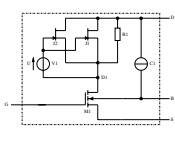
Symmetrical HV- NMOS Transistor



Introduction: High voltage CMOS technologies with lateral LDMOS transistors are used in markets like portable devices, automotive applications and display drivers. A accurate device model is key for the high efficiency of the circuit design. Increased breakdown voltages of HV transistors are achieved by an additional 'drift' region between the gate and drain terminal. This HV MOS device type is called Lateral Diffused MOS (LDMOS) transistor. Moreover parasitics resulting from complicated well structures are not sufficiently accounted for. The lack of existing analytical compact models is commonly available simulators for scalable LDMOS transistors can be overcome by introduction of sub-circuits. Standard low voltage MOS transistor models such as BSIM4 or EKV4 are not accurate enough for these purposes. They even miss the exact device behavior, e.g. in the saturation regime but also times even in the quasi saturation and Region regime. Deviations are due to the fact that the behavior of a HV MOS transistor is generally different compared to standard analog low voltage MOS transistors. These LDMOS transistor sub-circuits need to be compatible with all major SPICE simulators and need to include additional physical effects such as quasi-saturation, substrate currents as well as parasitic capacitances, diodes and bipolar. With this approach, highly accurate LDMOS SPICE models can be generated from standard BSIM4 or EKV4 low voltage transistor models. The characteristic curves presented below show a comparison between measurement data and simulation data and give an impression about the great agreement between measurement and model.

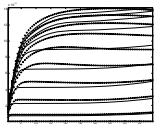
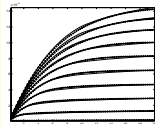
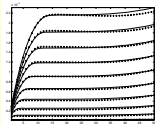
The control of parasitics is essential for HVCMOS technologies and the LDMOS devices because there is no buried layer available in HV CMOS technology. The switching of inductive loads can result in the turn on of parasitic bipolar transistors. An example of such a parasitic bipolar effect in an LDMOS can be seen in the right upper part of the poster. Highly accurate compact modeling is essential for controlling these parasitics effectively in visual design and avoiding detrimental substrate currents and latch-up.

Flexible Sub-circuit LD-MOS Transistor Modeling



DIG/SB Drain/Gate/Source/Bulk
 V1 Voltage controlled voltage source
 J1/J2 JFET
 M1 MOS transistor
 R1 Resistor
 C1 Controlled current source in order to model the substrate current

LDMOS Transistor Output Characteristic Sub-circuit Modeling



NMOS300 output characteristic of a typical device. $W_L = 200\mu$, $V_{GS} = 2.1, 4.4, 6.7, 8.9, 11.2, 13.5, 15.8, 18.1, 20.4, 22.7, 25.0, 27.3, 29.6, 31.9, 34.2, 36.5, 38.8, 41.1, 43.4, 45.7, 48.0, 50.3, 52.6, 54.9, 57.2, 59.5, 61.8, 64.1, 66.4, 68.7, 71.0, 73.3, 75.6, 77.9, 80.2, 82.5, 84.8, 87.1, 89.4, 91.7, 94.0, 96.3, 98.6, 100.9, 103.2, 105.5, 107.8, 110.1, 112.4, 114.7, 117.0, 119.3, 121.6, 123.9, 126.2, 128.5, 130.8, 133.1, 135.4, 137.7, 140.0, 142.3, 144.6, 146.9, 149.2, 151.5, 153.8, 156.1, 158.4, 160.7, 163.0, 165.3, 167.6, 169.9, 172.2, 174.5, 176.8, 179.1, 181.4, 183.7, 186.0, 188.3, 190.6, 192.9, 195.2, 197.5, 199.8, 202.1, 204.4, 206.7, 209.0, 211.3, 213.6, 215.9, 218.2, 220.5, 222.8, 225.1, 227.4, 229.7, 232.0, 234.3, 236.6, 238.9, 241.2, 243.5, 245.8, 248.1, 250.4, 252.7, 255.0, 257.3, 259.6, 261.9, 264.2, 266.5, 268.8, 271.1, 273.4, 275.7, 278.0, 280.3, 282.6, 284.9, 287.2, 289.5, 291.8, 294.1, 296.4, 298.7, 301.0, 303.3, 305.6, 307.9, 310.2, 312.5, 314.8, 317.1, 319.4, 321.7, 324.0, 326.3, 328.6, 330.9, 333.2, 335.5, 337.8, 340.1, 342.4, 344.7, 347.0, 349.3, 351.6, 353.9, 356.2, 358.5, 360.8, 363.1, 365.4, 367.7, 370.0, 372.3, 374.6, 376.9, 379.2, 381.5, 383.8, 386.1, 388.4, 390.7, 393.0, 395.3, 397.6, 399.9, 402.2, 404.5, 406.8, 409.1, 411.4, 413.7, 416.0, 418.3, 420.6, 422.9, 425.2, 427.5, 429.8, 432.1, 434.4, 436.7, 439.0, 441.3, 443.6, 445.9, 448.2, 450.5, 452.8, 455.1, 457.4, 459.7, 462.0, 464.3, 466.6, 468.9, 471.2, 473.5, 475.8, 478.1, 480.4, 482.7, 485.0, 487.3, 489.6, 491.9, 494.2, 496.5, 498.8, 501.1, 503.4, 505.7, 508.0, 510.3, 512.6, 514.9, 517.2, 519.5, 521.8, 524.1, 526.4, 528.7, 531.0, 533.3, 535.6, 537.9, 540.2, 542.5, 544.8, 547.1, 549.4, 551.7, 554.0, 556.3, 558.6, 560.9, 563.2, 565.5, 567.8, 570.1, 572.4, 574.7, 577.0, 579.3, 581.6, 583.9, 586.2, 588.5, 590.8, 593.1, 595.4, 597.7, 600.0, 602.3, 604.6, 606.9, 609.2, 611.5, 613.8, 616.1, 618.4, 620.7, 623.0, 625.3, 627.6, 629.9, 632.2, 634.5, 636.8, 639.1, 641.4, 643.7, 646.0, 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