MOS-AK Meeting
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Statistical Modeling of Leakage in Nano-CMOS Circuits

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… controlling leakage in nanometer CMOS SOC's

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Outline

- **Motivation**
- **Variability and leakage**
- **Statistical simulation: the standard approach**
- **Problems of statistical simulation**
- **Statistical simulation: virtual manufacturing**
- **Examples**
- **Conclusions**

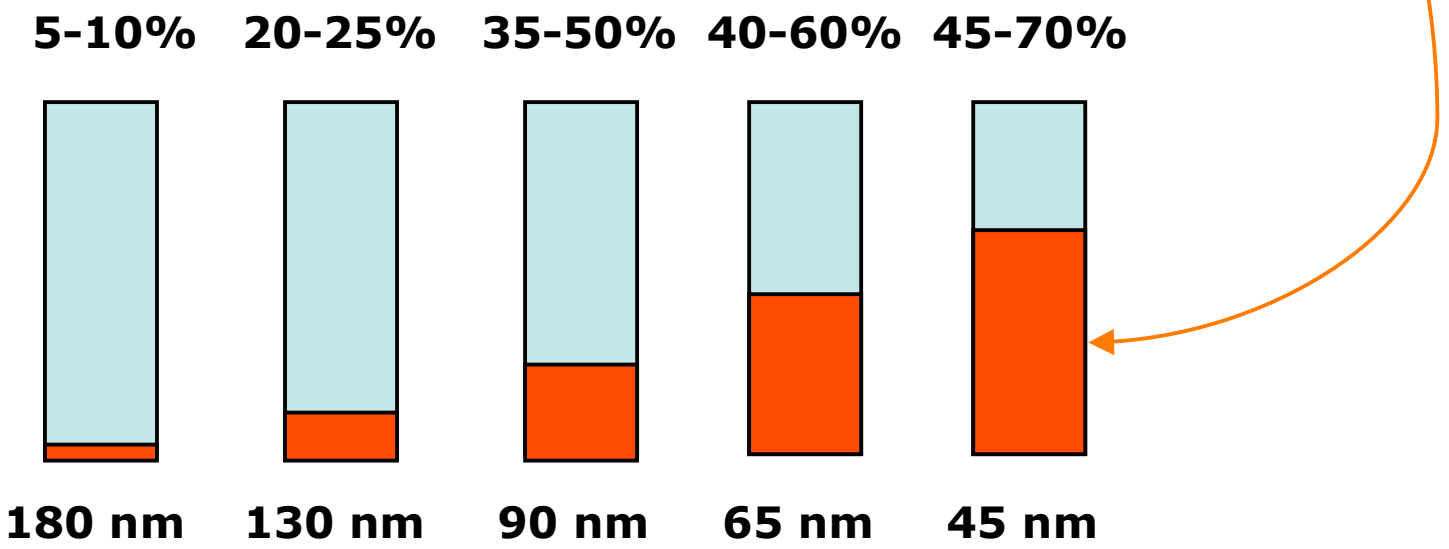
The power crisis

- **Power density in high performance VLSI chips is already at the same level as in a nuclear reactor**
- **Cooling is a big problem and is becoming expensive**
- **Increasing amount of energy is consumed by electronic devices (Amsterdam: 20% for telecom; USA: 9% for internet,...*)**
- **Battery maximum power and capacity increase by 10-15% per year, but chip power requirements increase much faster: 35-40% per year.**

***Source: 2000 CO^2 conference, Amsterdam, NL**

Leakage: a major contributor…

Leakage in nanometer scale CMOS: % of total power budget



The main advantage of static CMOS logic - negligible static power consumption - is lost!

How variability affects leakage

The problem: highly nonlinear dependences of some leakage currents on parameters that are subject to process variability.

Examples:

- **subthreshold current as a function of the threshold voltage**
- **gate tunneling current as a function of gate oxide thickness**

Subthreshold "off" current:

$$I_{subth} = \mu_n C \frac{W_N}{L_N} V_t^2 \exp\left(\frac{-V_{TH}}{nV_t}\right)$$

If V_{TH} is a random variable distributed normally with mean value V_{TH0} and standard deviation ΔV_{TH}, the distribution of the "off" current I_{subth} is log-normal with mean value

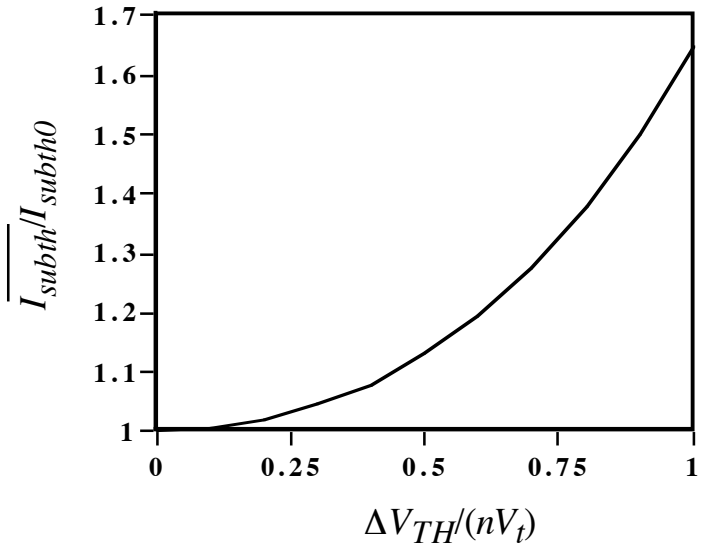
$$\overline{I_{subth}} = I_{subth0} \exp\left[\frac{1}{2}\left(\frac{\Delta V_{TH}}{nV_t}\right)^2\right]$$

($I_{subth0} = I_{subth}$ for $V_{TH} = V_{TH0}$)

How variability affects leakage

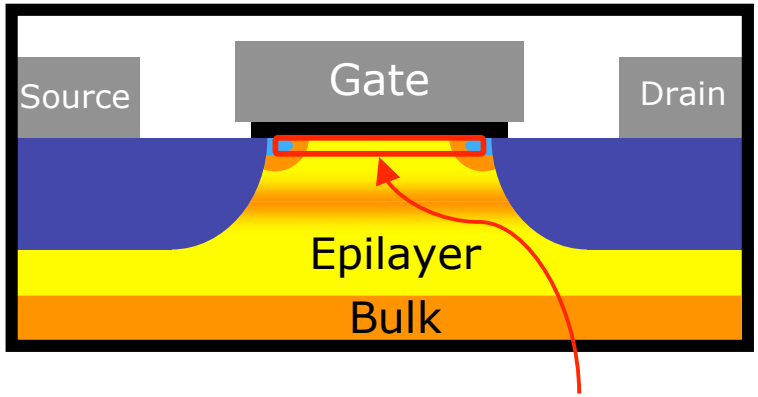
For V_{TH} variability of the order of nkT/q (n*26 mV; n between 1 and 2) the mean value of the "off" current increases by about 65%.

If this is local (intra-die) variability, the sum of "off" currents of all devices increases accordingly.



The mean value and the total subthreshold "off" current increases with increasing variability

Variability is large and unavoidable



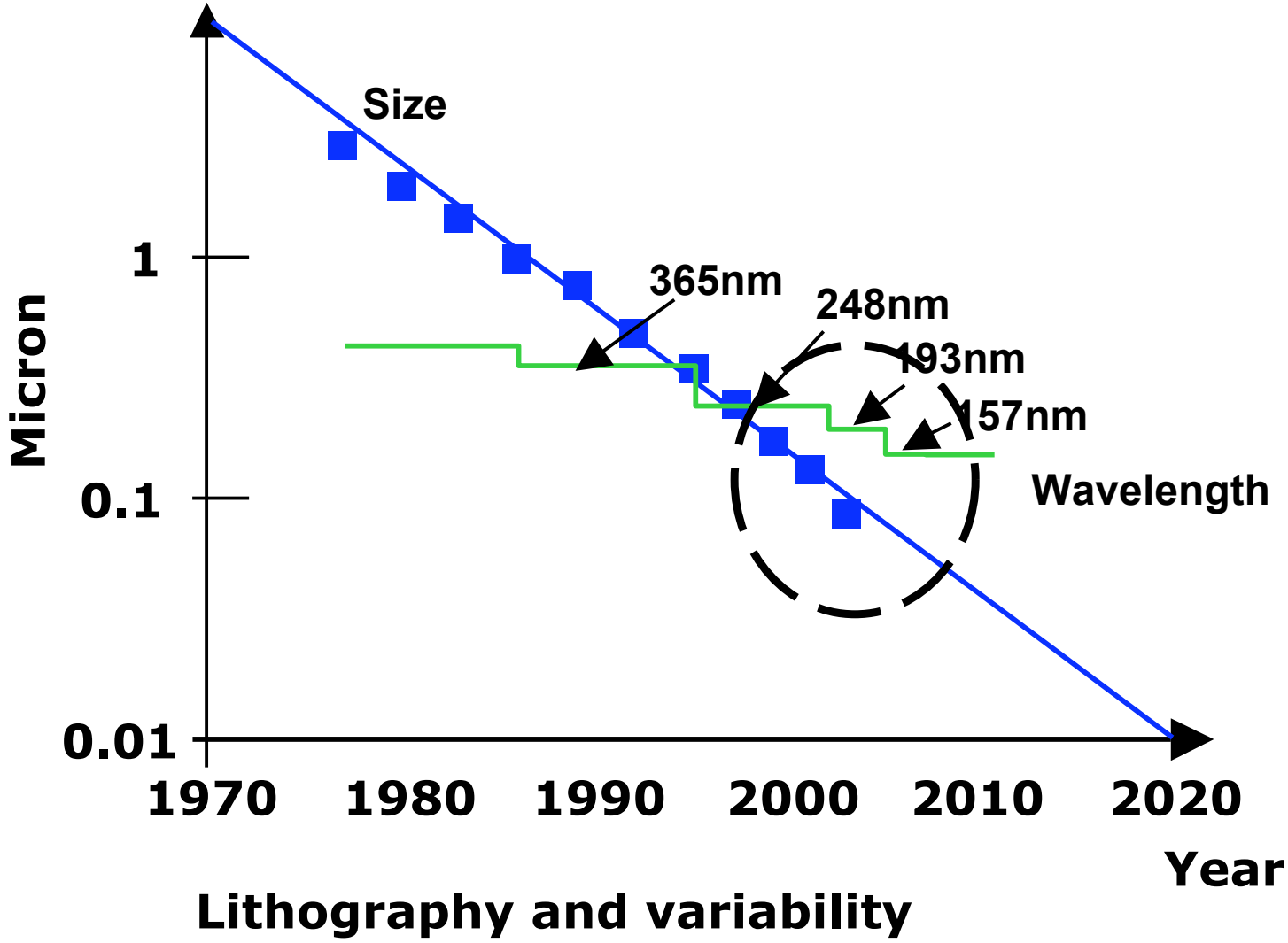
Threshold voltage V_{TH} is a function of doping in the channel, and subthreshold leakage depends on V_{TH} exponentially

However, doping in the channel means single atoms in nanometer CMOS: the average number of boron atoms in the channel of a 32 nm device is 3.5.

-> 3 atoms in one device and 4 atoms in another means 25% difference of the doping dose.

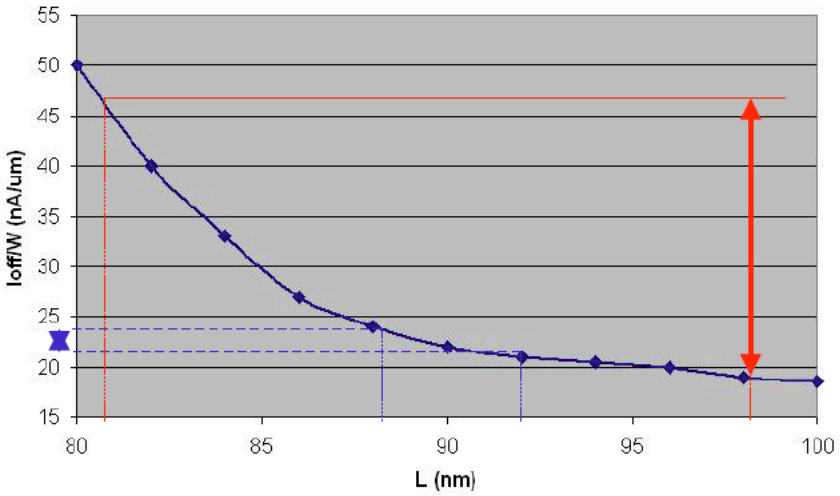
Source: T. Skotnicki, "Nano-CMOS & Emerging Technologies–Myths and Hopes", Plenary presentation PL-1, 2006 Int. Conf. on Solid State Devices and Materials, Yokohama, Sept. 2006.

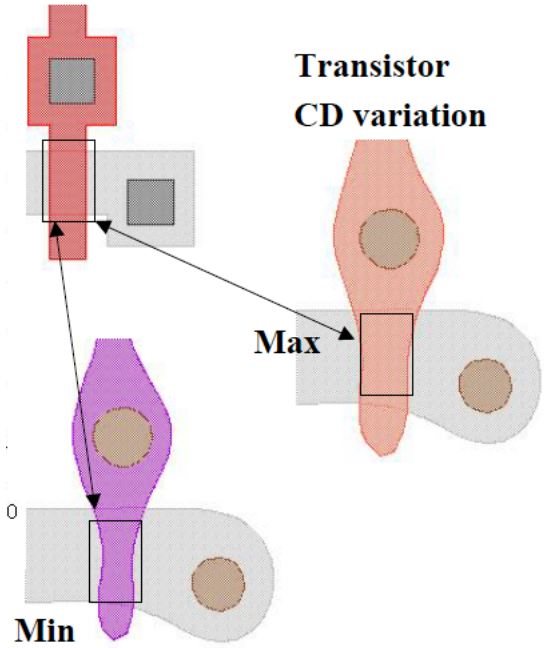
Variability is large and unavoidable



Variability is large and unavoidable

Litography related variations of subthreshold leakage:



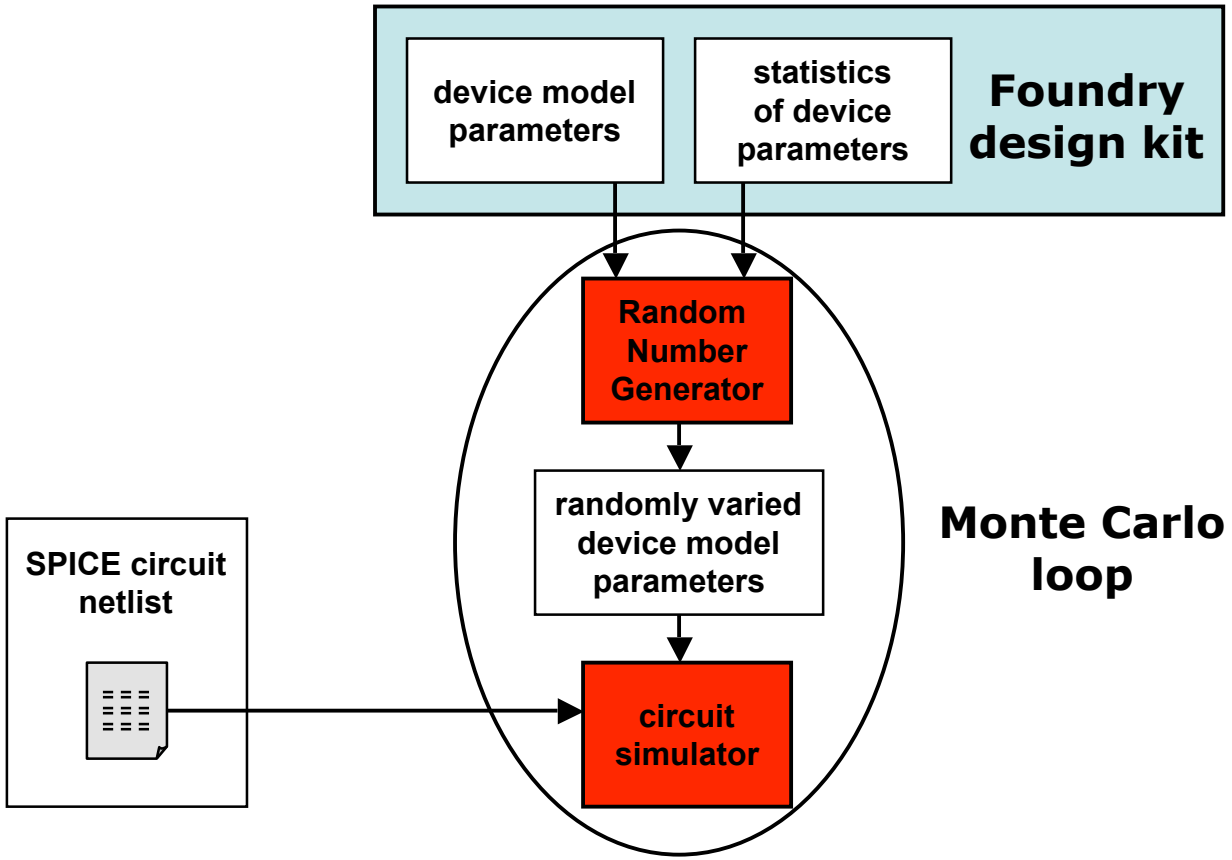


90 nm: 20% variations of channel dimensions -> 2x I_{off} variations

Source: J-M. Brunet [9] "Addressing Variability in the Design to Manufacturing Flow", in Design and Process Engineering: Bridging the EDA Gap, IEEE Web Seminar, November 9, 2006, reproduced with permission

Variability: modeling methods

Compact model based methodology (the standard approach): statistical Monte Carlo simulation in a circuit simulator



Variability: modeling methods

Compact model based methodology: statistical Monte Carlo simulation in a circuit simulator

- **Advantages:**
  - **Well established**
  - **Only standard EDA tools needed**
  - **Limited computational complexity**
- **Disadvantages**
  - **It is difficult to include correlations (between model parameters in a single device and between parameters of various devices in the circuit)**
  - **No direct link to physical design and to manufacturing**
  - **Expensive and time consuming experimental characterization of test devices needed**

Variability affects leakage in a complex way

Litography: variability of channel dimensions

- **directly affects I_{on}, I_{off}**
- **indirectly affects I_{on}, I_{off} via V_{TH} variations (short channel effect)**

Variability of gate oxide thickness

- **directly affects I_{on}, I_{off} via C_{ox}**
- **indirectly affects I_{on}, I_{off} via V_{TH} variations (V_{TH} depends on C_{ox})**

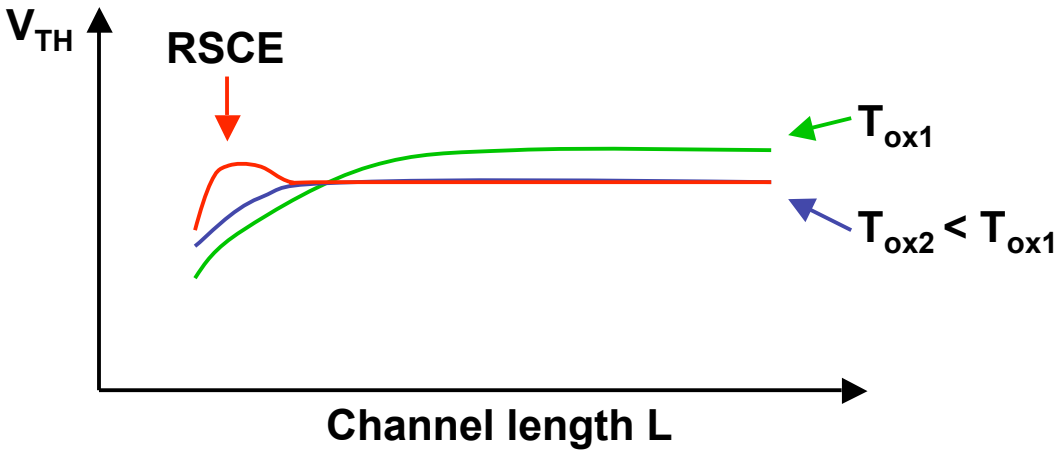
Variability of doping concentrations and profiles

- **indirectly affects I_{on}, I_{off} via:**
  - **V_{TH} variations**
  - **variations of actual channel length**
  - **variations of body effect factor**

Variability affects leakage in a complex way

Intra-device correlations

Intra-device correlations: e.g. threshold voltage is correlated with gate oxide thickness and channel length

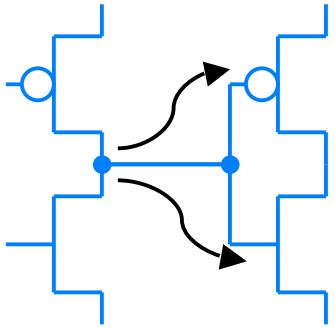


These correlations are not accounted for in compact model based Monte Carlo simulation.

The mathematical technique is known (K. S. Eshbaugh, IEEE Trans. on CAD, vol. 11, no. 10, 1992, pp. 1198-1206) but computationally infeasible in most cases.

Variability affects leakage in a complex way

The loading effect

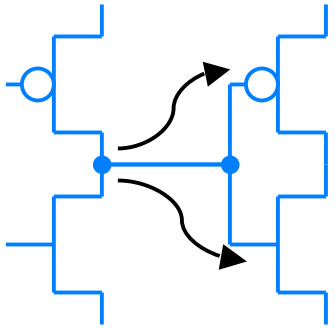


Unlike other leakage components, gate leakage changes the way CMOS static gates work: DC current flows from gate output nodes to input nodes of other gates (the "loading effect").

Consequences:

- **logic levels and noise margins may be affected,**
- **gate fanout is limited by the DC load,**
- **total leakage in a digital circuit can no longer be calculated as a sum of leakages of all gates treated independently.**

Variability affects leakage in a complex way



The loading effect may either increase or reduce the total leakage of the gate.

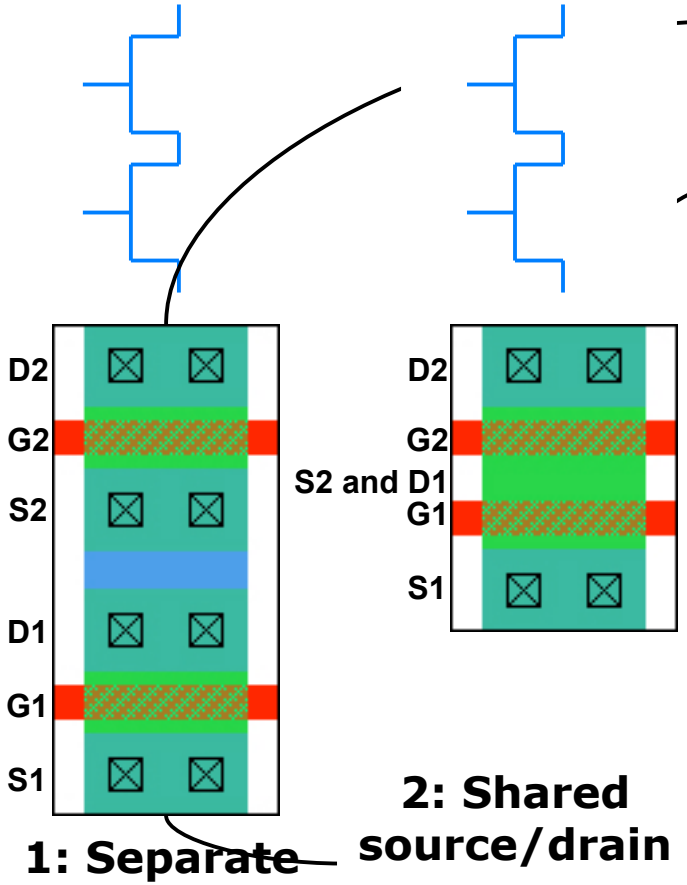
R. Mendoza, R. Ferre, L. Balado and J. Figueras, in Proc. IEEE Int. Conf. on Design and Test of Integrated Systems in Nanoscale Technology, Tunis, Sept. 2006.:
1% error in estimated total leakage of a logic block (t_{ox}=1.85 nm)

S. Mukhopadhyay, S. Bhunia and K. Roy, IEEE Trans. on CAD, vol. 25, no. 8, 2006, pp. 1486-1495:
5% to 8% error for a single gate (t_{ox}=1.0 nm) but lower for bigger logic blocks

A. Rastogi, W. Chen and S. Kundu, in Proc. DAC 2007, San Diego, June 2007, pp. 712 - 715:
from 1.9% up to 17.2% error for various ISCAS benchmark blocks

Variability affects leakage in a complex way

Two MOS transistors connected in series



Pre-layout simulation:

```
MN1 1 2 3 0 Nchan W=325E-9 L=65E-9
+PD=1040E-9 AD=6.34E-14

MN2 3 4 5 0 Nchan W=325E-9 L=65E-9
+PD=1040E-9 AD=6.34E-14
```

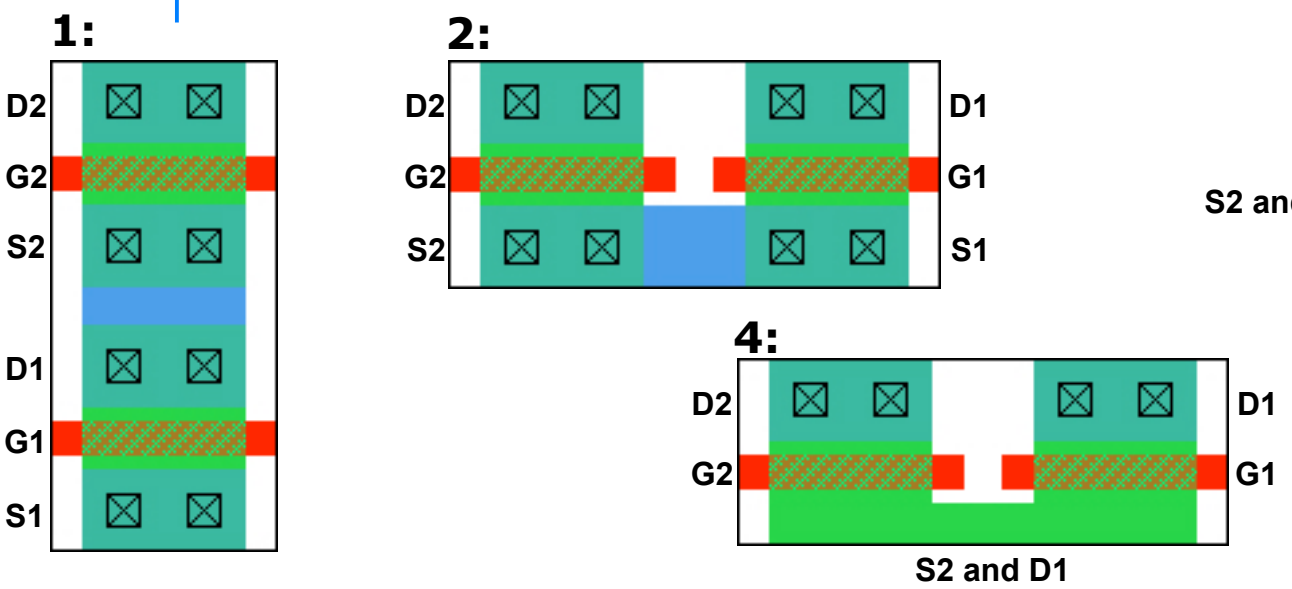
OK for layout 1

WRONG for layout 2: actual area and perimeter of D1 and S2 much lower than the sum for individual drain/source junctions

The same schematic, the same W and L, but different S1 and D2 areas and perimeters -> different leakage

Variability affects leakage in a complex way

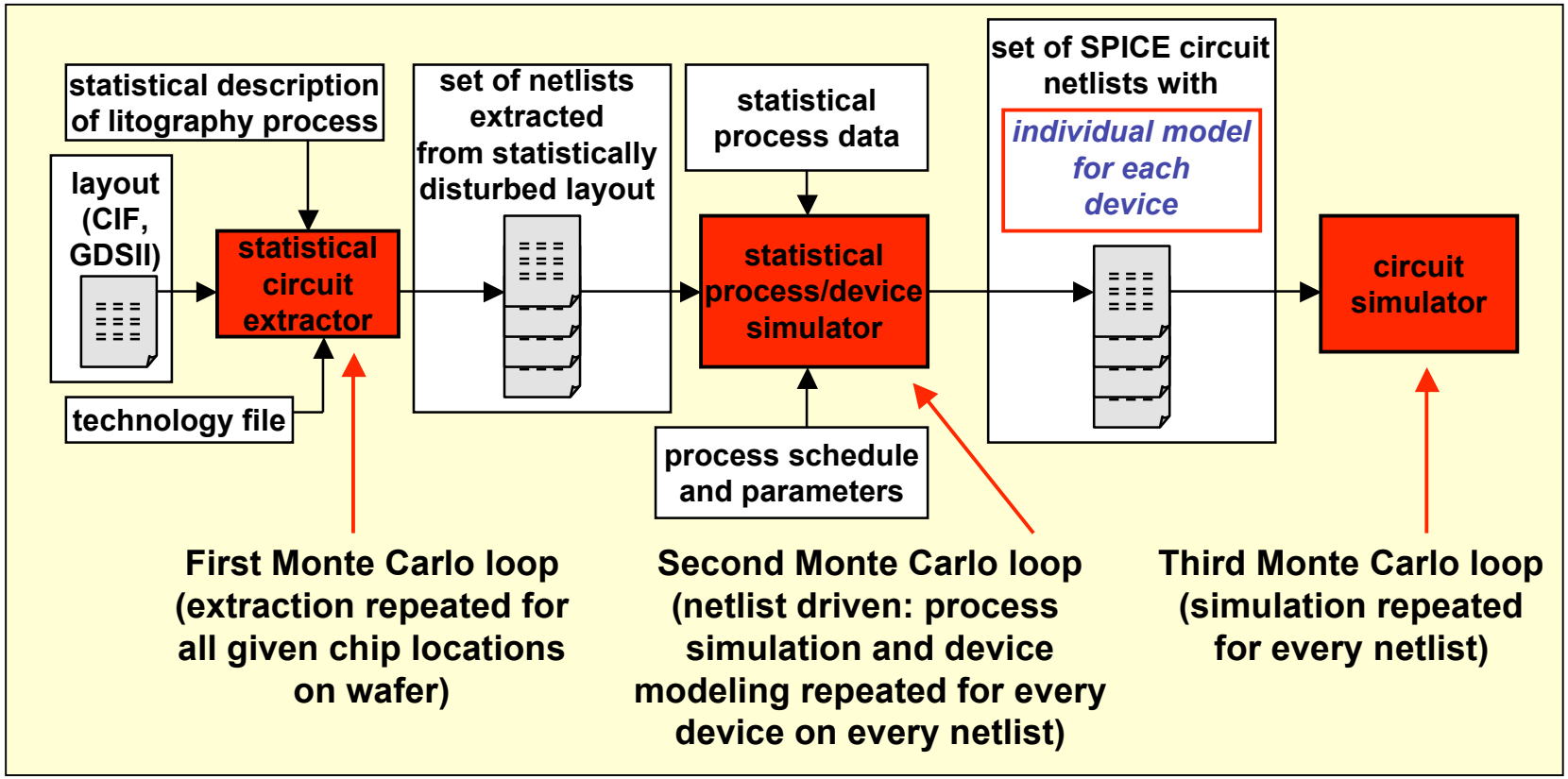
Two MOS transistors connected in series:
1,2: separate devices; 3,4: shared source/drain



Post-layout simulation (after extraction): to avoid ambiguities and either missing or duplicated S/D areas, transistors and S/D diodes should be extracted separately -> PSP and JUNCAP2 models

Process variability: modeling methods

"Virtual manufacturing" methodology: statistical (Monte Carlo) process, device and circuit simulation



Process variability: modeling methods

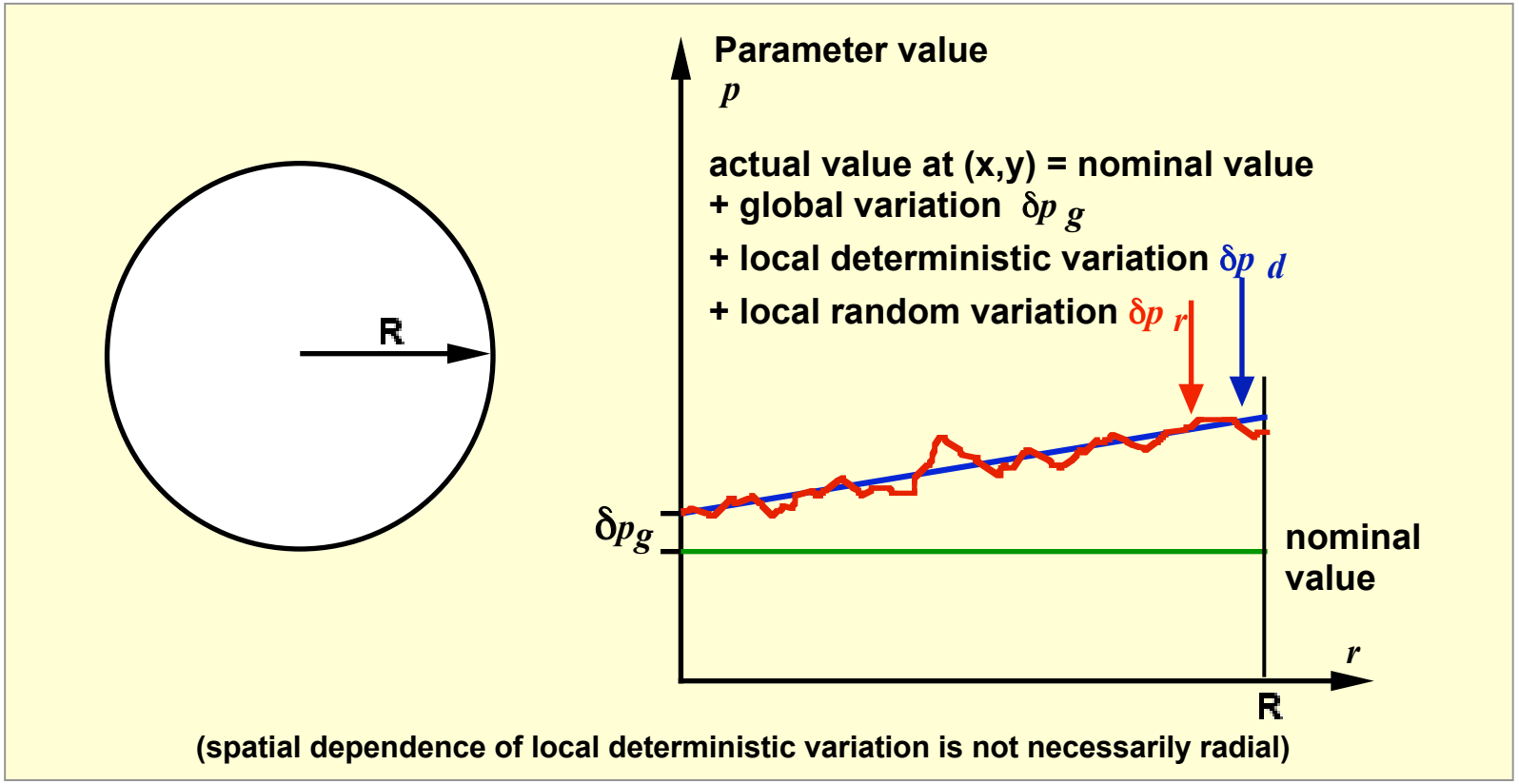
Virtual manufacturing methodology: statistical (Monte Carlo) process, device and circuit simulation

- **Advantages:**
  - **Based on statistical process and device simulations, with process variabilities accounted for**
  - **All correlations taken into account**
  - **Actual device layout taken into account**
  - **Allows "what if" experiments with processing parameters, may show directions to process and device design optimization**
- **Disadvantages**
  - **Special software needed**
  - **Process must be known or at least reasonable assumptions must be made; fitting to nominal characteristics of real devices needed**
  - **Significant computational resources needed for large statistical samples**

Process variability: variation types

Process variations

Local value of a parameter p: $p = p_{nom} + \partial p_g + \partial p_d(x,y) + \partial p_r$



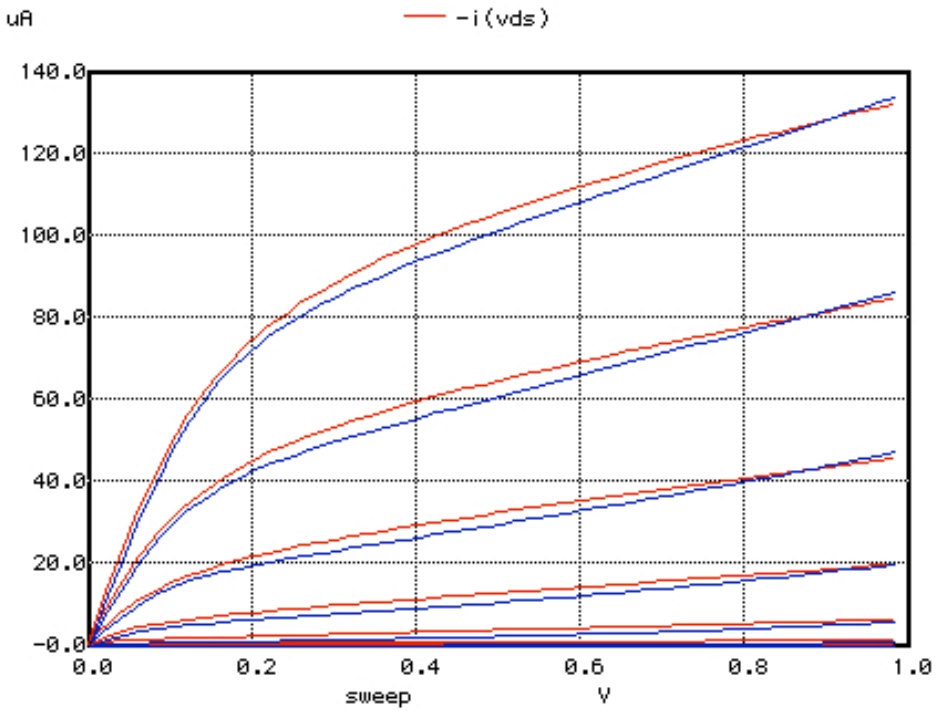
(spatial dependence of local deterministic variation is not necessarily radial)

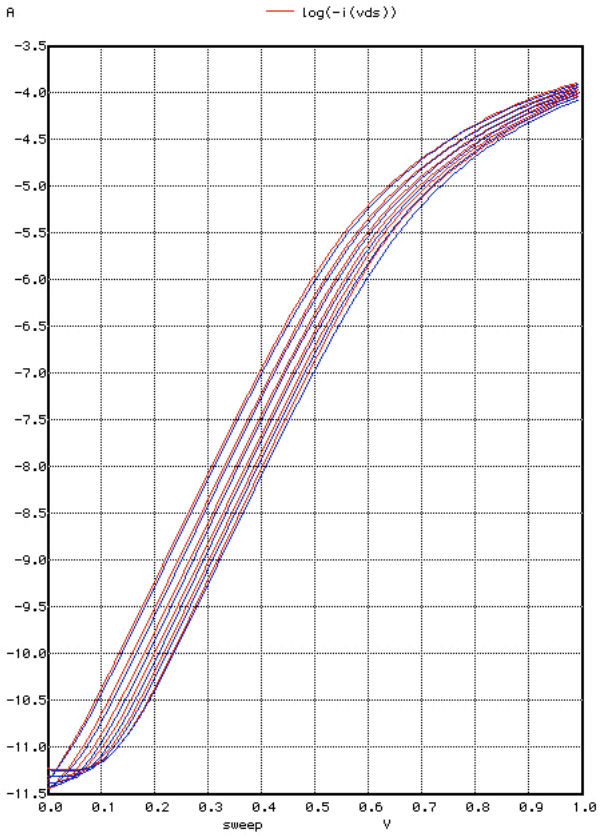
Virtual manufacturing

Virtual technology fitted to an industrial 65 nm technology: 65 nm NMOS device

target (real) device

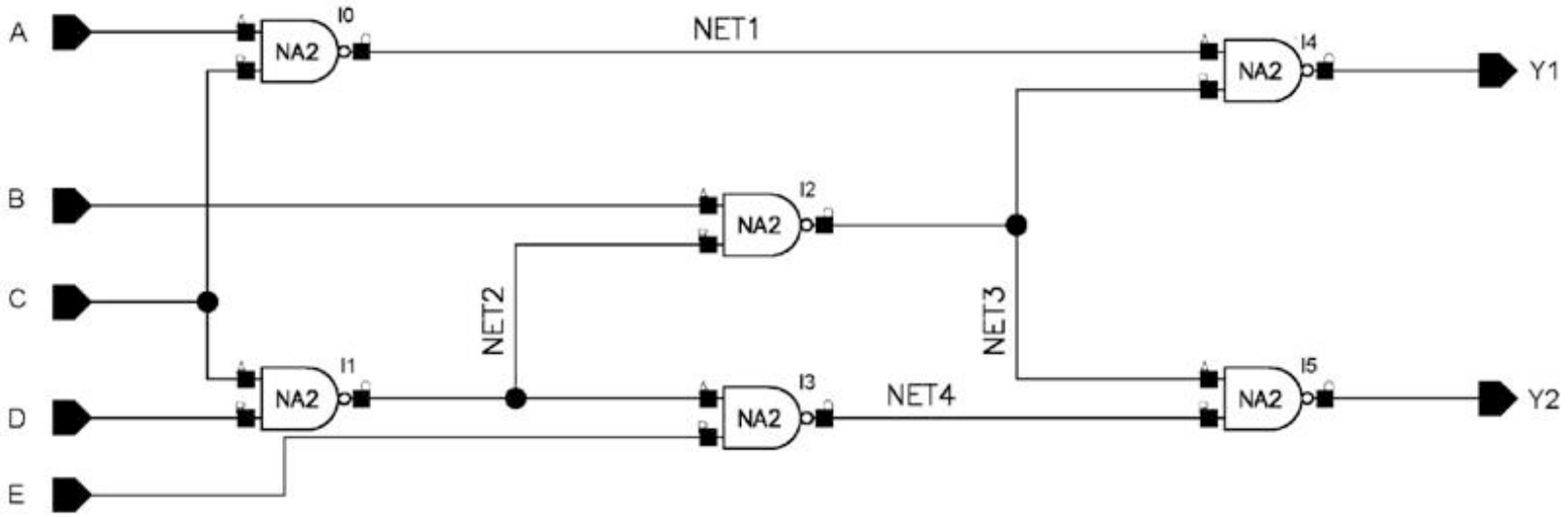
virtually manufactured device





Example

Example: a small digital block (c17 ISCAS benchmark)

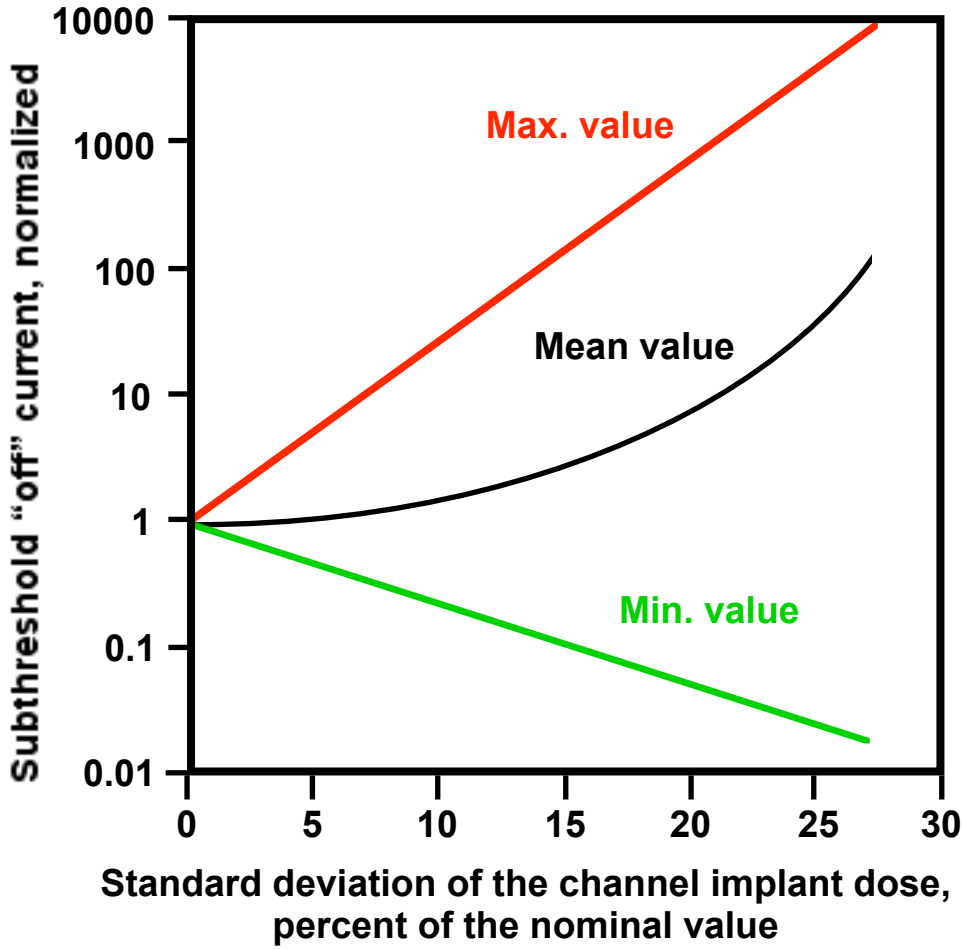


Virtual manufacturing

Variability of "off" drain current vs. doping variability

A single nMOSFET, L=65 nm

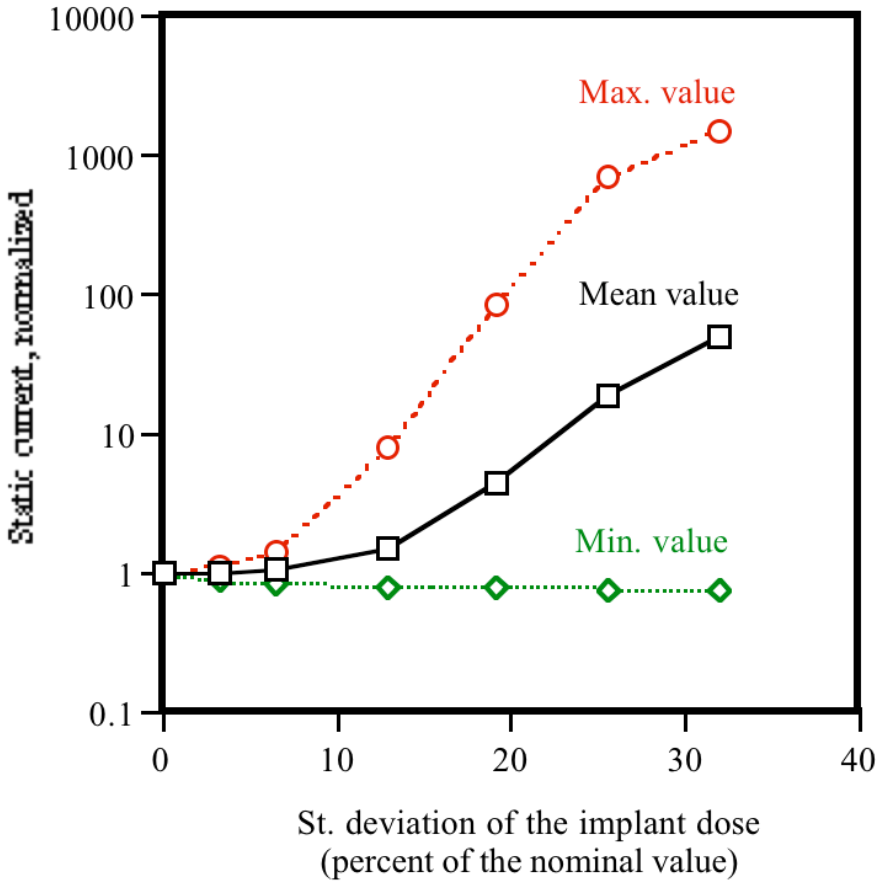
"Off" drain current vs. variability of channel implant dose



Virtual manufacturing

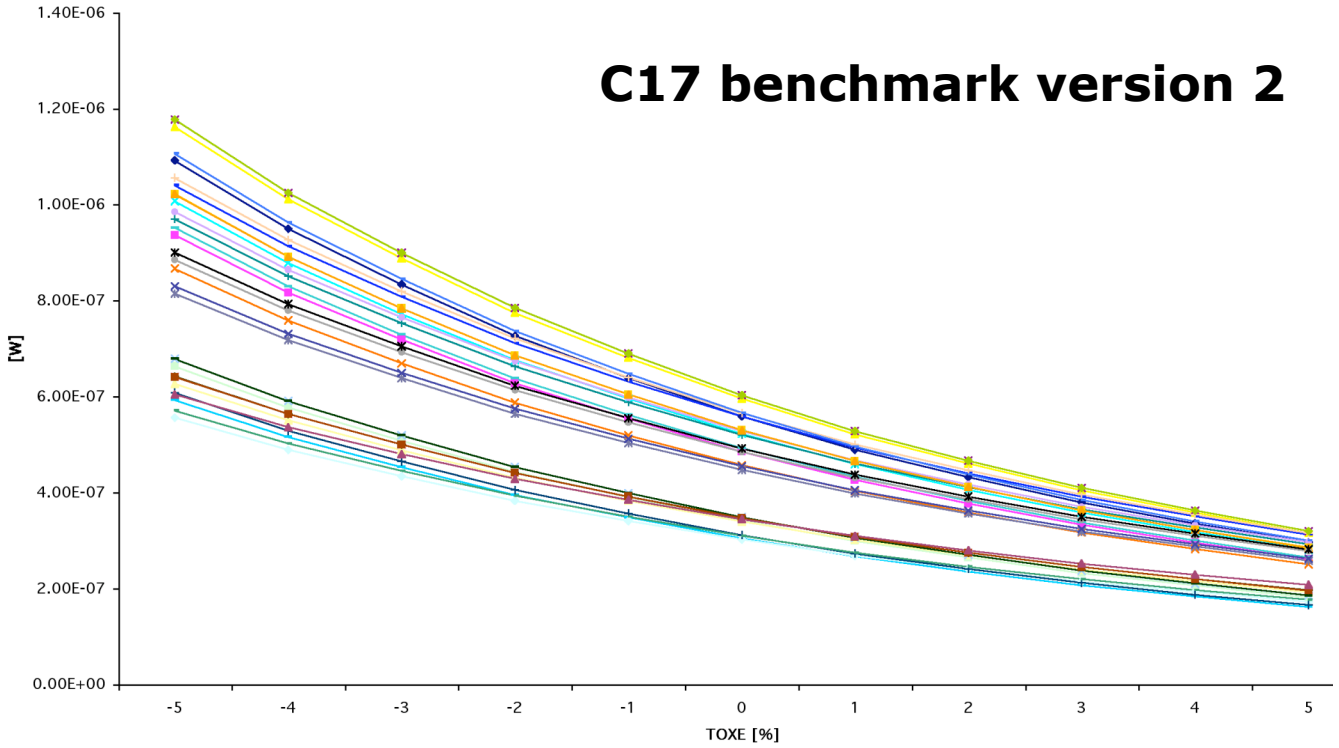
Total leakage power vs. local variability of the channel doping

C17 benchmark version 1



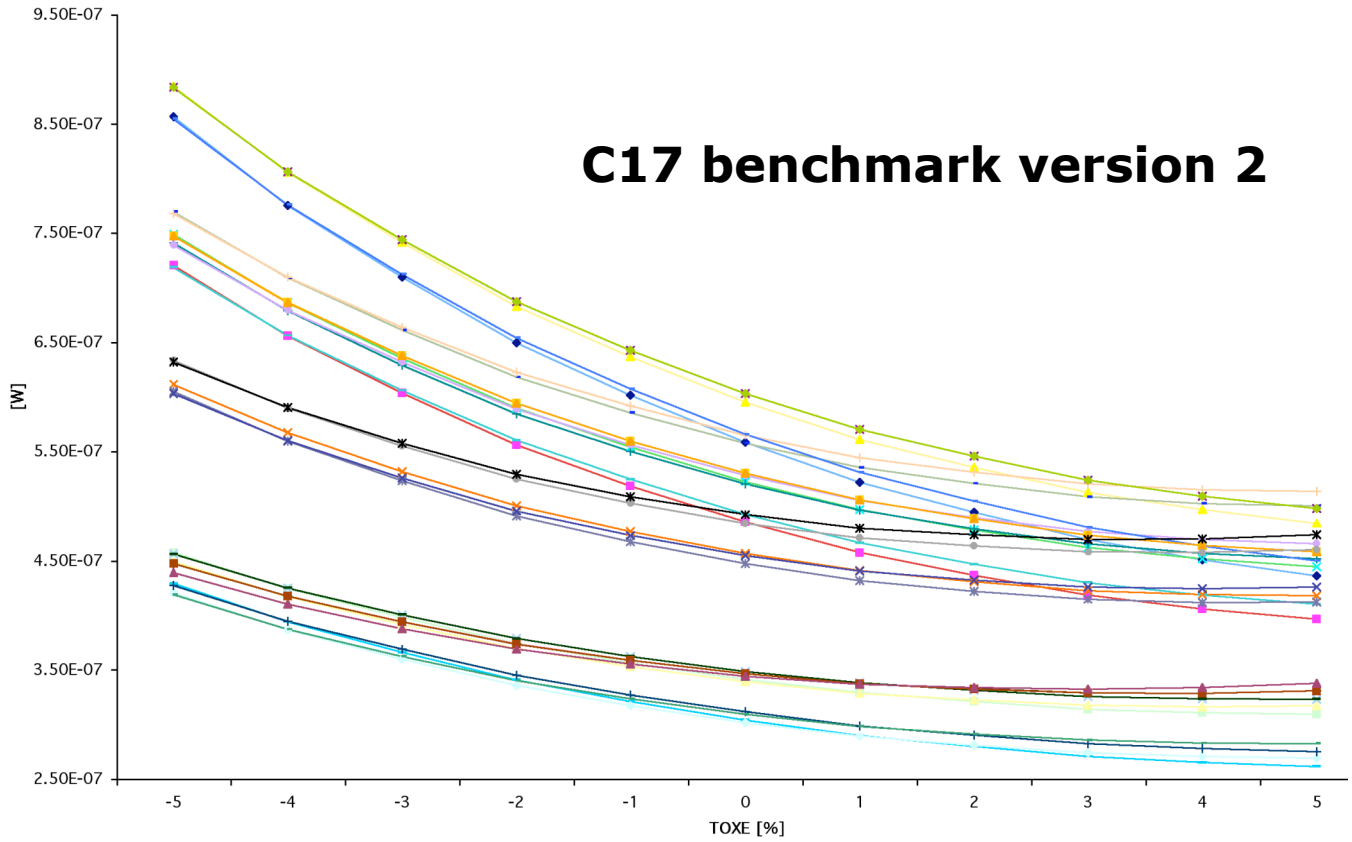
The standard approach

Total leakage power vs. variability of the gate oxide thickness



Virtual manufacturing

Total leakage power vs. variability of the gate oxide thickness



Conclusions

- **Large process variability leads to increased total static power consumption**
- **Standard approach (compact model based Monte Carlo simulation inside a circuit simulator) may lead to inaccurate or even misleading results due to:**
  - **Complex intra-device correlations**
  - **No direct link to layout**
  - **No direct link to manufacturing process**