Xsim: Unification of MOSFET Compact Models with the Unified Regional Modeling Approach

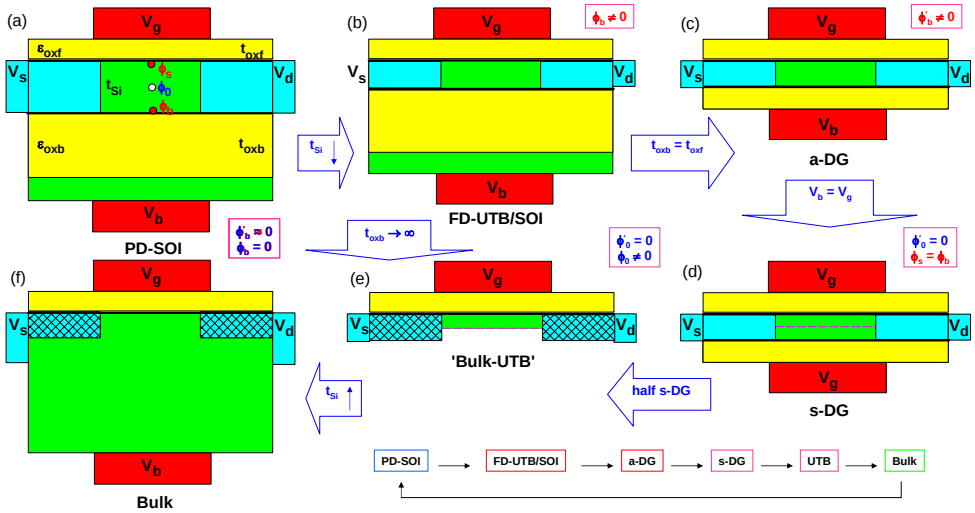
Guojun Zhu, Guan Huei See, Shihuan Lin, Chengqing Wei, Junbin Zhang, Zuhui Chen, Ramachandran Selvakumar, and Xing Zhou*
School of Electrical and Electronic Engineering & Institute for Sustainable Nanoelectronics
Nanyang Technological University, Singapore (*Email: exzhou@ntu.edu.sg)

Abstract

This poster presents the motivation and philosophy behind the development of a compact model (Xsim) for unification of MOSFET models with the unified regional modeling (URM) approach. It is based on unified regional surface potential solutions for generic double-gate (including SOI and nanowire) MOSFETs with common/independent-gate biasing and with/without body contact. The DC/AC model is physically scalable in geometry/bias as well as in body thickness and doping, encompassing partial/full-depletion and volume inversion. New paradigm shift in ground-referencing and source/drain-by-label provides complete Gummel symmetry while allowing physical modeling of asymmetric devices, which also provides easy extension to include contact effects for modeling doped as well as Schottky-barrier source/drain. The core model is directed towards modeling emerging devices and technologies in one unified framework without duplicating efforts, which also provides seamless transitions among various device structures and operations, with selectable accuracy for simulation and verification of future-generation ULSI circuits.

Philosophy

Seamless Transformation and Unification of MOSFETs



Key Model Equations

Unified regional channel surface-potential equations

$$\phi_s = \begin{cases} \phi_{cc} = V_{gf} + 2v_{th}\mathcal{L}\left\{\dfrac{\Upsilon}{2\sqrt{v_{th}}}e^{-(V_{gf}-V_r)/v_{th}}\right\} & (V_{gr} << V_{FB}) \\ \phi_{dd} = V_r + \left(-\dfrac{\Upsilon}{2} + \sqrt{\dfrac{\Upsilon^2}{4} + V_{gf} - V_r}\right)^2 & (V_{FB} < V_{gr} < V_{FD}) \\ \phi_{vi} = V_{gf} - \Upsilon\sqrt{\psi_{fd}} & (V_{FD} < V_{gr} < V_t) \\ \phi_{ss} = V_{gf} - 2v_{th}\mathcal{L}\left\{\dfrac{\Upsilon}{2\sqrt{v_{th}}}e^{(V_{gf}-2\phi_F-V_c)/v_{th}}\right\} & (V_{gr} >> V_t) \end{cases}$$

Drift-Diffusion based Carrier transport

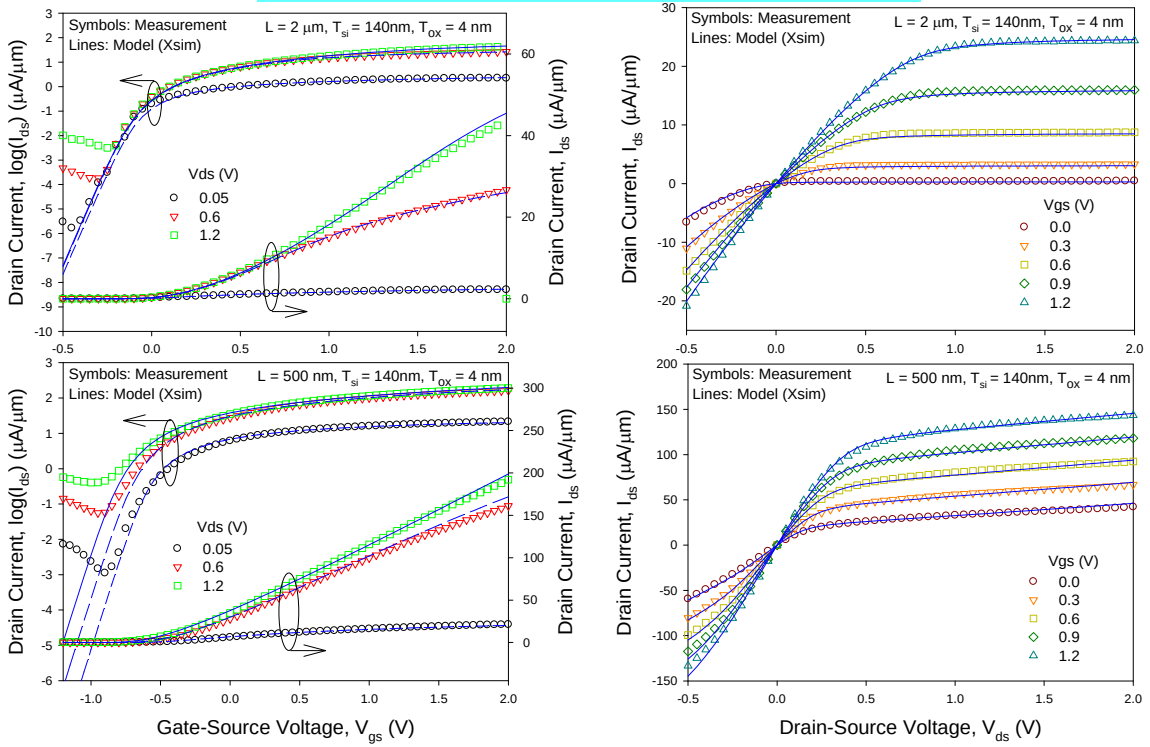
$$I_{ds} = \mu_{eff\,0} C_{ox} \frac{W}{L}\left(\overline{q_i} + \overline{A_b} v_{th}\right) V_{ds,eff}$$

$$V_{ds,eff} = V_{d,eff} - V_{s,eff}$$

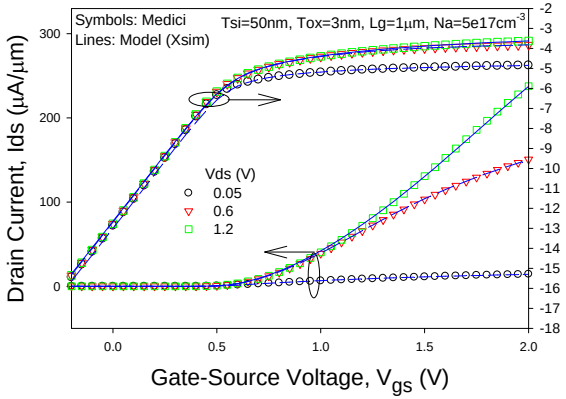
Thermionic-Tunneling based Carrier transport

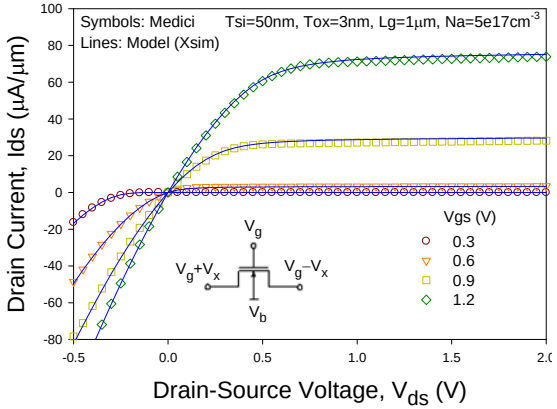
$$I_{ds,n} = -\frac{AA_n^* T}{k_B} \int_{q(\Phi_{B,n} - \Delta\Phi_{B,n} + \Phi_{Cn})}^{E_\infty} T_t(E) \cdot \left[f_C\left\{E; -q(V_d - V_n)\right\} - f_C\left\{E; -q(V_s - V_n)\right\}\right] dE$$

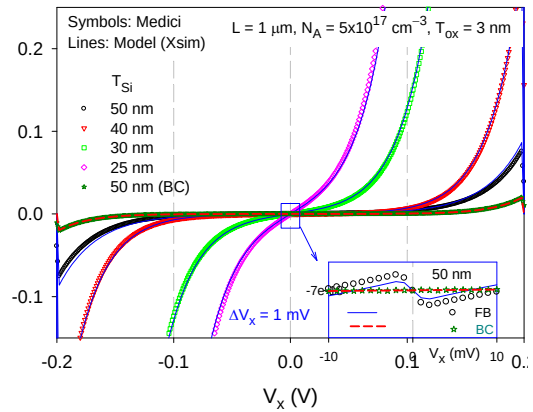
Double Gate / Silicon Nanowire MOSFETs

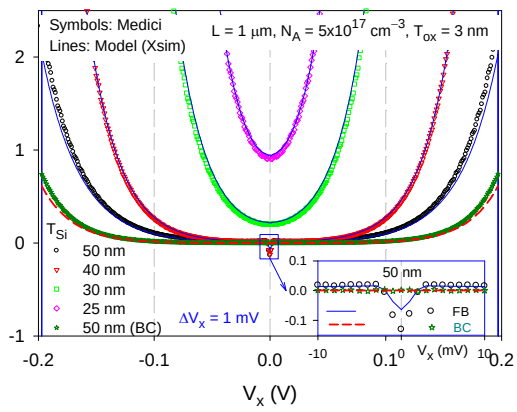


SOI MOSFETs

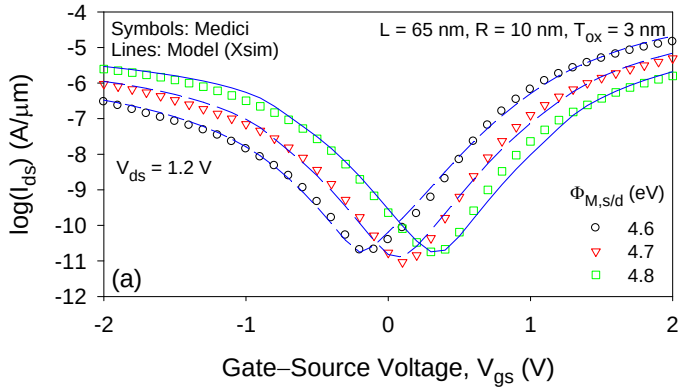


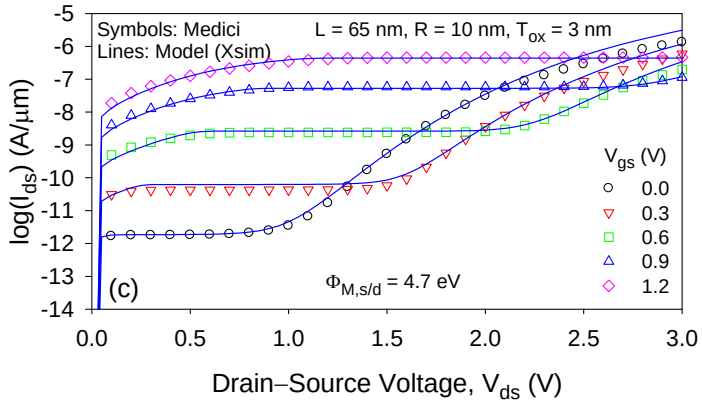


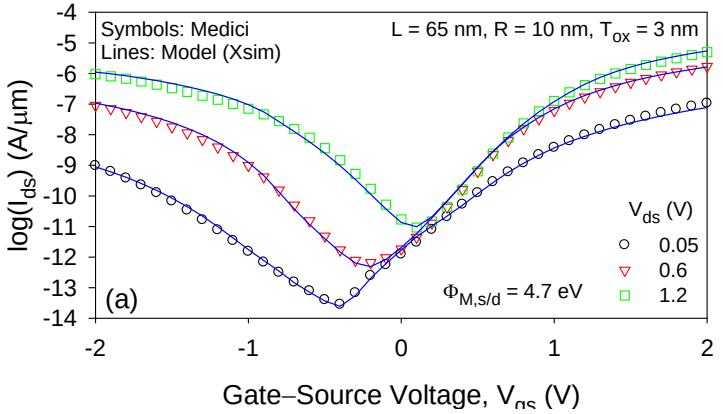


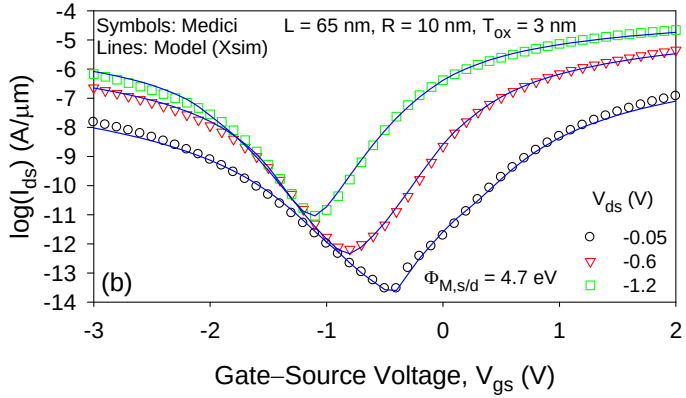


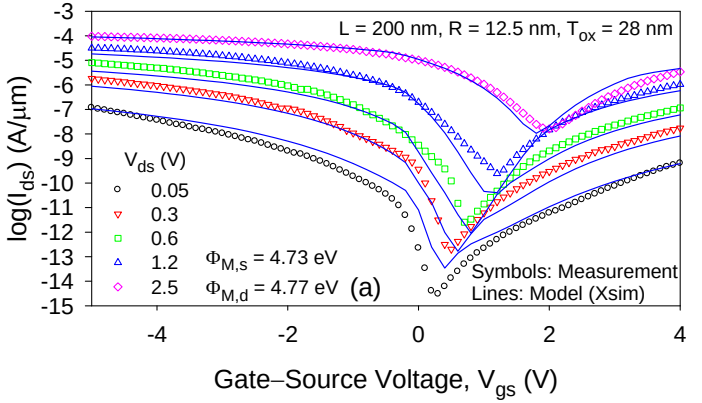
Schottky Barrier DG/SiNW MOSFETs

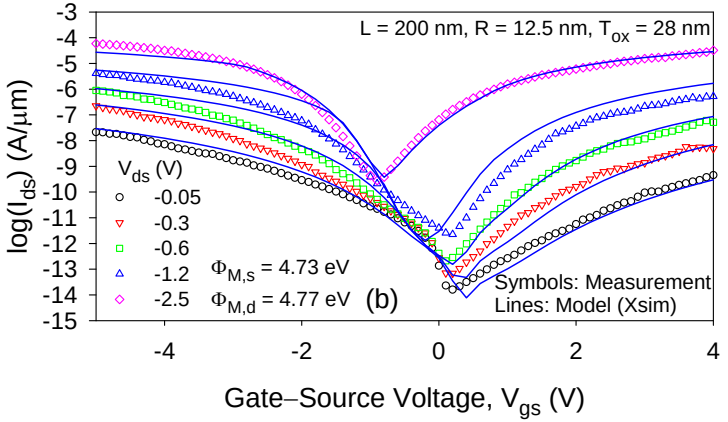












G. J. Zhu, *et al.*, "'Ground-Referenced' Compact for Three-Terminal Symmetric Double-Gate MOSFETs with Source-Drain Symmetry," *IEEE TED*, Vol. 55, No.9, pp. 2526–2530, Sep. 2008.

G. J. Zhu, *et al.*, "A Compact Model for Symmetric Double-Gate MOSFETs with Schottky-Barrier Source/Drain," *ESSDERC*, Edinburgh, 2008.

This work was supported in part by Semiconductor Research Corp. under Contract No. 2004-VJ-1166G and Nanyang Technological University under Grant RGM30/03.