Compact Modeling for Process and Device Characterization

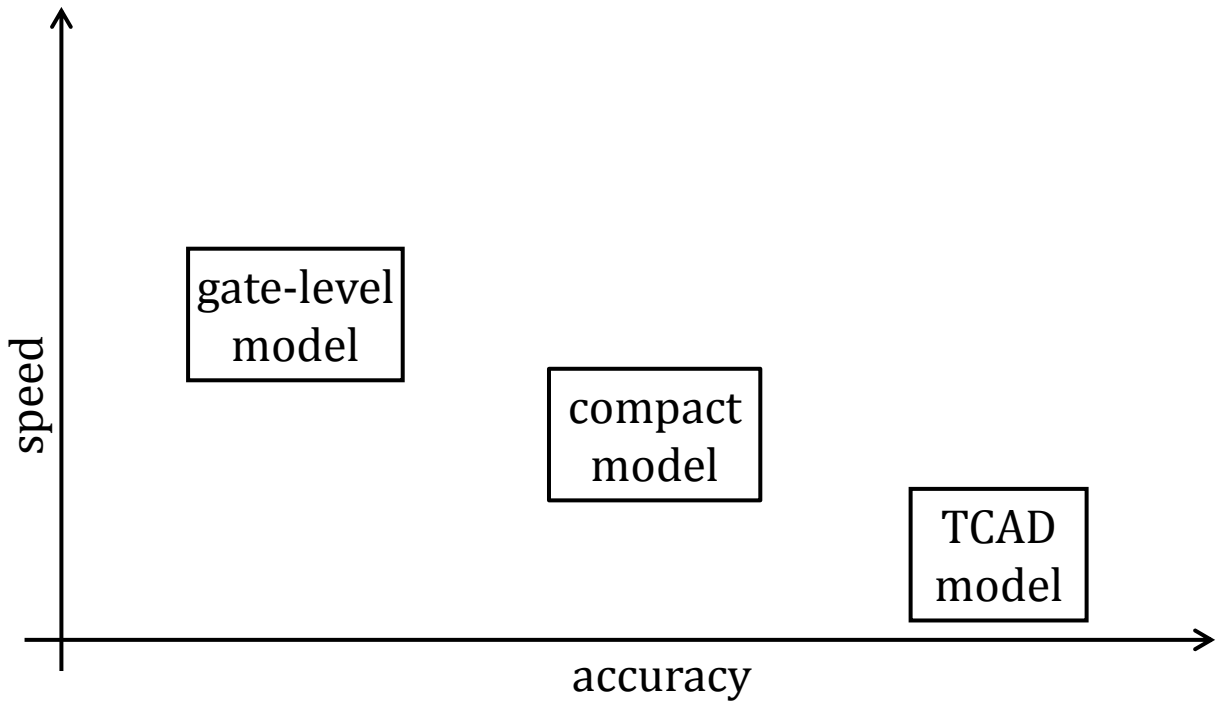
Daniel Tomaszewski, Wladek Grabinski
ITE (PL), MOS-AK (EU)

Outline

- Compact modeling of devices, subcircuits
- Compact modeling for process/device characterization
- Subjective survey of parameter extraction methods
  - Local methods with based on different ranges of experimental data
  - Local methods using optimization
  - Global methods using evolutionary algorithms
  - Statistical modeling
- Integrated tools for modeling and parameter extraction
- Compact modeling for IC design
- Summary, acknowledgments

Semiconductor device compact modeling

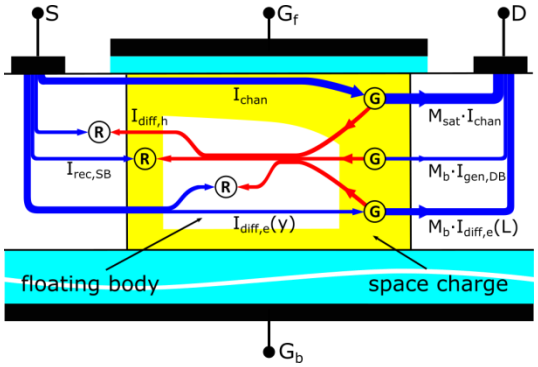
G.J. Coram, Tutorial: "How to (and How NOT to) Write a Compact Model in Verilog-A", BMAS2004



What is a Compact Model ?

- A model of transistor currents & voltages
- Built from physically-motivated equations
- Intended for use in an analog circuit simulator

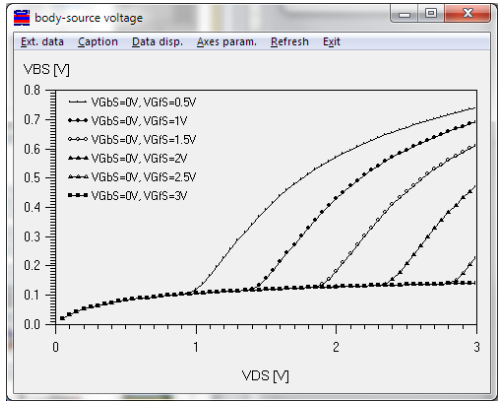
Compact modeling of PDSOI MOSFETs



D. Tomaszewski, A.Jakubowski, J. Gibki, "A Small-Signal Non-Quasistatic Model of PD SOI MOSFETs", Electron Technology, "A Model of I-V Characteristics of Partially-Depleted SOI MOSFET", Electron Technology, 1999, no. 1/2

H.-K. Yu, et al., "A Physical Model of Floating Body Thin Film Silicon-On-Insulator nMOSFET with Parasitic Bipolar Transistor", IEEE TED 1994, No.5

$$i_S(t) + i_{Gf}(t) + i_D(t) + i_{Gb}(t) = 0$$

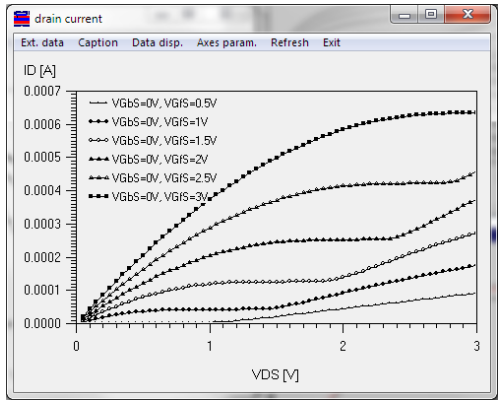


S. E. Laux, "Techniques for Small-Signal Analysis of Semiconductor Devices", IEEE TCAD 1985. No.4

$$u(t) = U + u^* \cdot e^{j\omega t} \qquad (S^3A)$$

$$\text{DC:} \quad I_S + I_{Gf} + I_D + I_{Gb} = I_S + I_D = 0 \quad \Rightarrow \mathbf{V_{BS}}$$

$$\text{AC:} \quad i_s^* + i_{gf}^* + i_d^* + i_{gb}^* = 0 \quad \Rightarrow \mathbf{v_{bs}^*}$$



J. R. Hauser, "Small Signal Properties of Field Effect Devices", IEEE TED 1965, No.12

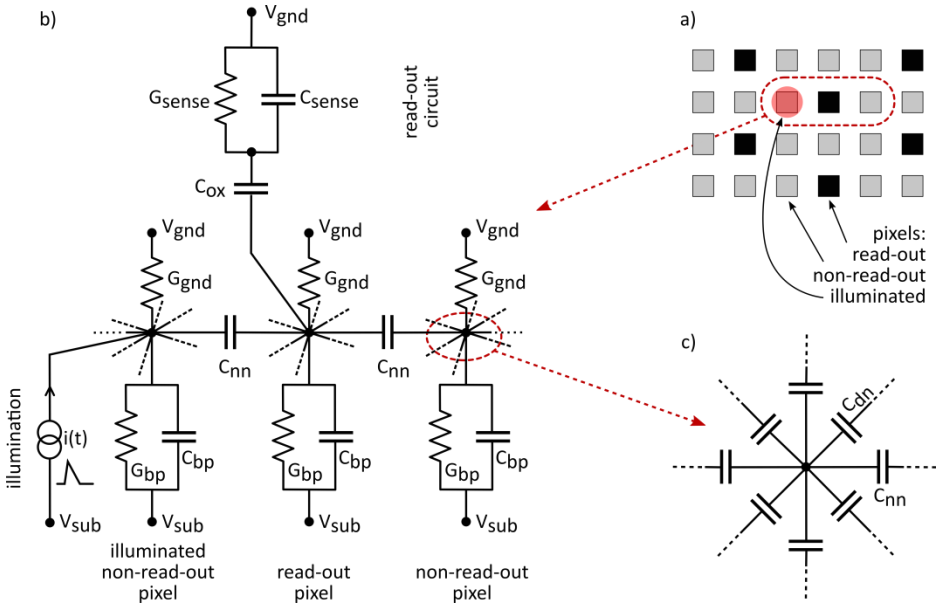
$$i_{cf}^*(0) = \{\lambda_{f0}[v_s^* - (v_{gf}^* - v_{thf}^*)] + \mu_{f0}[v_d^* - (v_{gf}^* - v_{thf}^*)]\}/\Theta_f$$

$$i_{cf}^*(L) = \{\lambda_{fL}[v_s^* - (v_{gf}^* - v_{thf}^*)] + \mu_{fL}[v_d^* - (v_{gf}^* - v_{thf}^*)]\}/\Theta_f$$

$$Y_{xy} = \delta_{xy} \cdot i_x^*/v_y^*; \quad C_{xy} = \mathrm{Im}(Y_{xy})/\omega; \quad x, y \in \{s, gf, d, gb\}$$

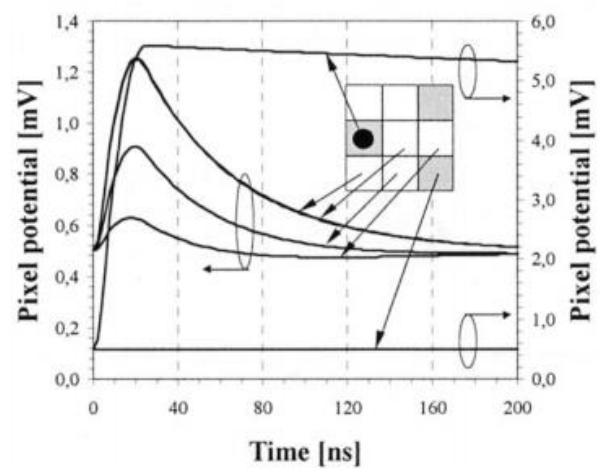
D. Tomaszewski, K. Domański, L. Łukasiak, A. Zaręba, J. Gibki, A. Jakubowski, "DC and AC models of partially-depleted SOI MOSFETs in weak inversion", in "Progress in SOI Structures and Devices Operating at Extreme Conditions", Ed.: F. Balestra, A. Nazarov. V. S. Lysenko, NATO Science Series (Series II: Mathematics, Physics and Chemistry), vol 58, Springer, Dordrecht, 2002

Compact modeling of an ionizing radiation pixel detector with interleaved pixels



M. Caccia, et al., "Characterization of hybrid pixel detectors with capacitive charge division" in AIP Conf. Proc., 2001, vol. 57

J. Marczewski, D. Tomaszewski, K. Domański, P. Grabiec, M. Caccia, S. Borghi, R. Campagnolo, W. Kucewicz, "Charge sharing modeling in pixel detectors with capacitive charge division", IEEE TED, 2003, No. 1



k-th non-readout pixel:

$$-G_{gnd}\cdot v_k(t)+G_{bp}\cdot[V_{sub}-v_k(t)]+C_{bp}\cdot d[V_{sub}-v_k(t)]/dt+\sum_i C_{n(d)n}\cdot d[v_i(t)-v_k(t)]/dt=0$$

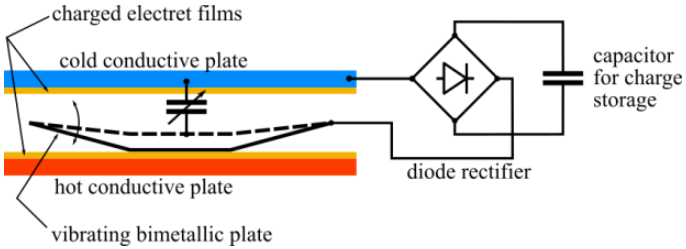
l-th readout pixel:

$$-G_{gnd}\cdot v_l(t)+G_{bp}\cdot[V_{sub}-v_l(t)]+C_{bp}\cdot d[V_{sub}-v_l(t)]/dt+\sum_j C_{n(d)n}\cdot d\big[v_j(t)-v_l(t)\big]/dt+$$

$$+C_{ox}\cdot d\big[v_{l,sense}(t)-v_l(t)\big]/dt=0$$

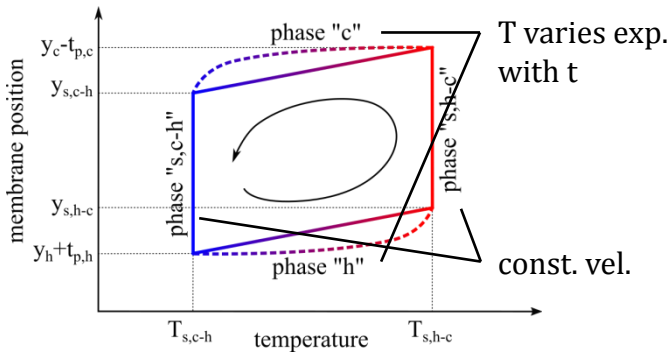
$$-G_{sense}\cdot v_{l,sense}(t)-C_{sense}\cdot dv_{l,sense}(t)/dt-C_{ox}\cdot d\big(v_{l,sense}(t)-v_l(t)\big)/dt=0$$

Compact modeling of a device for the thermal energy harvesting

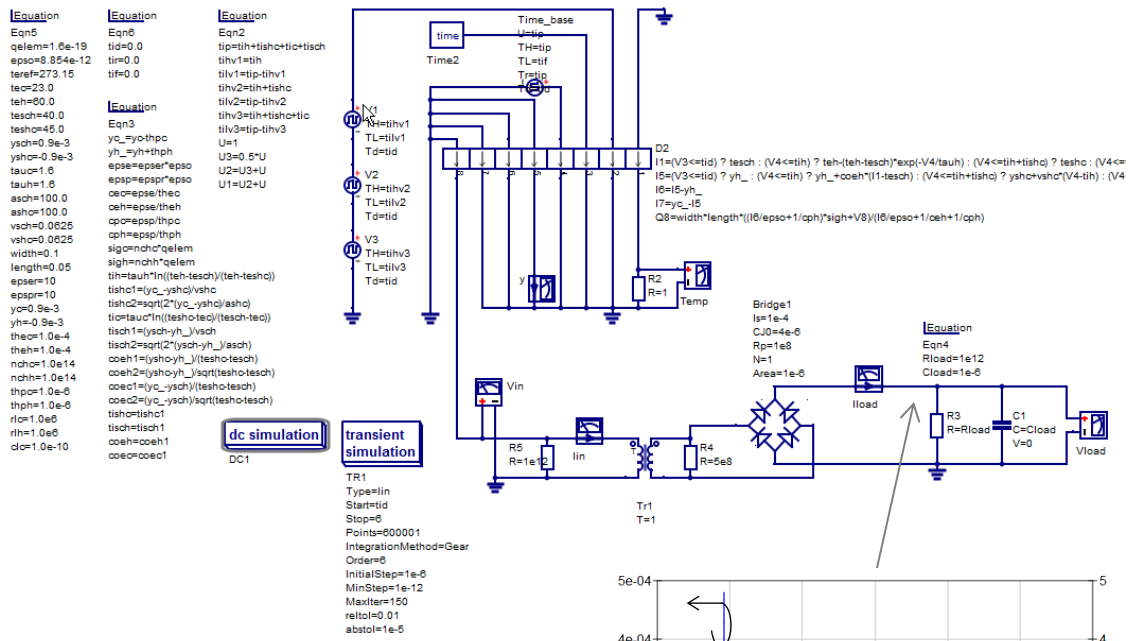


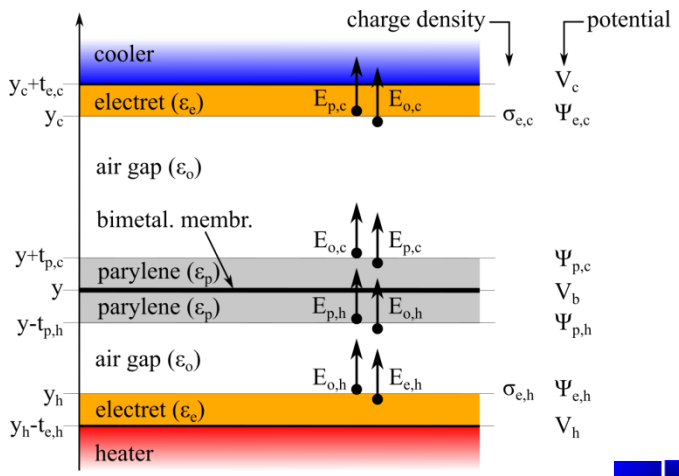
O. Puscasu, et al., "An innovative heat harvesting technology (HEATec) for above-Seebeck performance", Proc. IEDM, 2012

C. Ucke, H.-J. Schlichting, "Revival of the jumping disc", Phys. Educ. 44 (6) 612-617, 2009

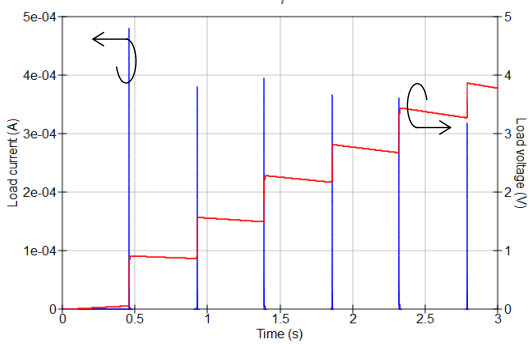


M. E. Brinson, V. Kuznetsov, "A new approach to compact semiconductor device modelling with Qucs Verilog-A analogue module synthesis", IJNM, 2016; Vol. 28, 2016





D. Tomaszewski, K. Domański, P. Prokaryn, "Qucs-Based Development of an Energy Harvester Compact Model", Proc. MIXDES'2015



C_{Load} = 0.1 μF, R_{Load} = 1 GΩ

Compact modeling for process/device characterization

Typical elements in the characterization tasks

Purpose of characterization / Object of characterization	Characterization of material	Characterization of layers	Characterization of devices	Characterization of interaction between the devices
Si wafer	resistivity, carrier mobility	×	×	×
Diffusion/Polysilicon resistor		sheet resistance	parameters of resistors and groups of resistors	×
Thin film induction coil	×	×	self inductance	mutual inductance
Capacitor	carrier lifetime; doping concentration in the substrate	thickness of dielectric layers	workfunction difference; charges in the MOS/MIS structures	×
Diode	carrier lifetime in the area next to the p-n junction; doping concentration in the base region	×	parameters of p-n junctions and groups of p-n junctions	×
Gate-controlled diode	carrier lifetime in the area next to the p-n junction; carrier lifetime below the gate dielectric; concentration of the doping in the substrate under the junction and under the gate	thickness of dielectric layers; surface generation velocity	×	×
MOS transistor	concentration of the doping in the substrate under the junction and under the gate	thickness of dielectric layers	parameters of MOS transistors and groups of MOS transistors	parameters characterizing short channel effects, latch-up effects, and others determining the design rules
Groups of MOS transistors; **Groups of IC cells.**	×	×	characteristics of the statistical distributions of MOS transistor parameters	×

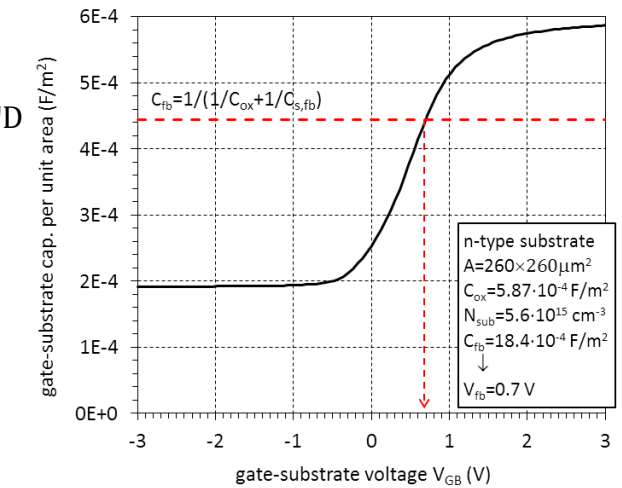
Compact modeling for characterization – parameter extraction methods

- **Methods based on information in a single point of the electrical characteristics**

- Extraction of the MOSFET threshold voltage V_{th}: $V_{th} = V_{GS}$ @ $I_D/(W_{eff}/L_{eff})=10^{-7}$ A

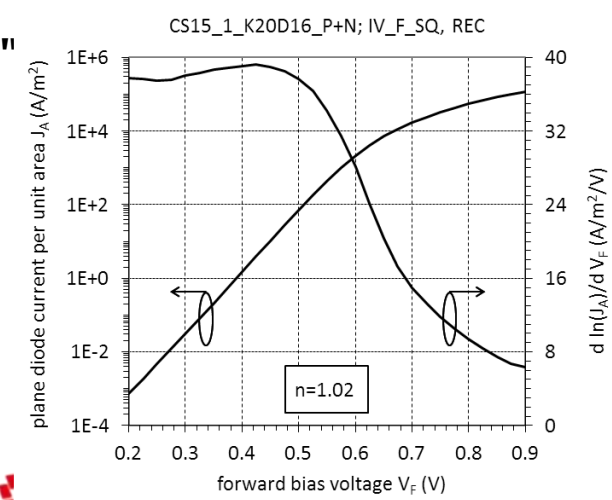
- Extraction of the MIS structure flat-band voltage V_{fb}: $V_{fb} = V_{GB}$ @ $C_{gb}=C_{fb}$ where $C_{fb}=1/(1/C_{ox}+1/C_{s,fb})$; $C_{s,fb} = \varepsilon_s/L_D$

✓ Simple measurement
× Additional information required
× Uncertainty of the characteristics in the neighbourhood



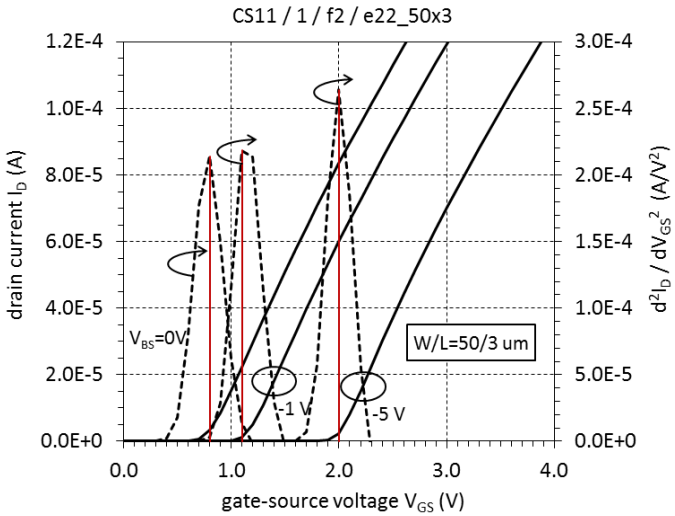
- **Methods using extremum of a "primary" or "secondary" characteristics**

- Extraction of the ideality factor n of the $I(V_F)$ characteristics of the p-n junction: $n = 1/[\max(d \ln(J_A)/d V_F)]$



Compact modeling for characterization – parameter extraction methods

Extraction of the MOSFET threshold voltage V_{th}:



- $V_{th}=V_{GS}$ @ max (d^2I_D/dV_{GS}^2)

  H. S. Wong, et al., "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET", Solid-State El., Vol. 30, No. 9

  ✓ serial resistance, mobility degradation effects eliminated

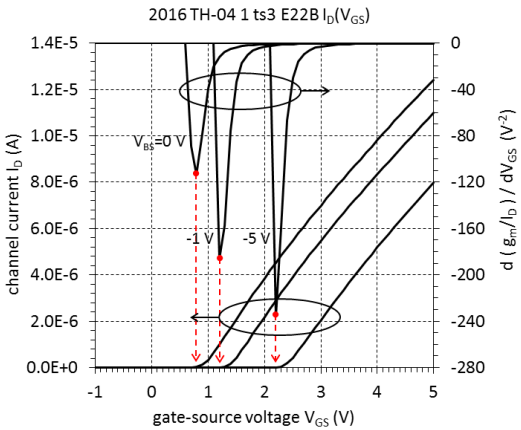
- $V_{th}=V_{GS}$ @ max (dC_{gc}/dV_{GS})

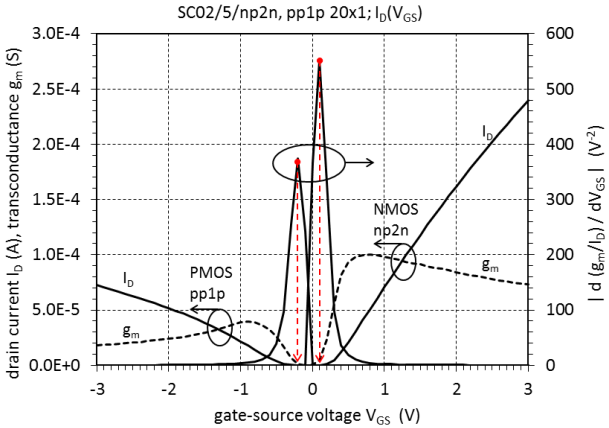
  C.-K. Park, et al., "A unified current–voltage model for long-channel MOSFETs", IEEE TED, vol. 38, no. 2

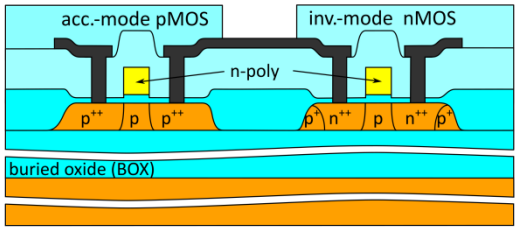
  ✓ serial resistance, mobility degradation effects eliminated

- $V_{th} = V_{GS}$ @ max $[\, d(g_m/I_D)/dV_{GS} \,] \equiv V_{GS}$ @ max (dC_{gc}/dV_{GS})

  D. Flandre, et al., "gm/Id Method for Threshold Voltage Extraction Applicable in Advanced MOSFETs With Nonlinear Behavior Above Threshold", IEEE EDL, Vol. 31, No. 9







Process: Dr. K.Kucharski + ITE team

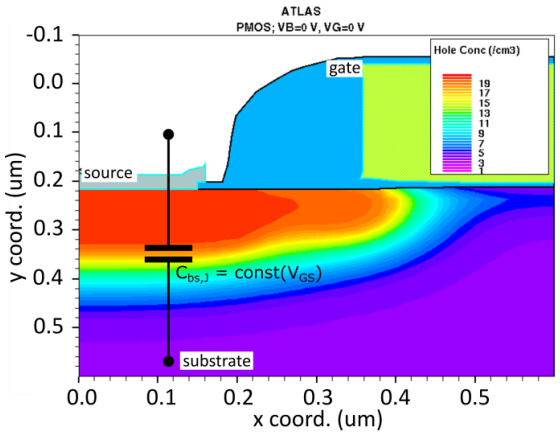
Compact modeling for characterization – parameter extraction methods

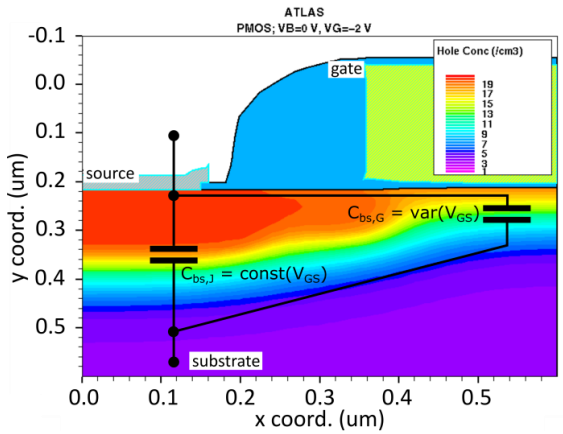
- Extraction of the MOSFET threshold voltage V_{th}: $V_{th}=V_{GS}$ @ max (dC_{bs}/dV_{GS})

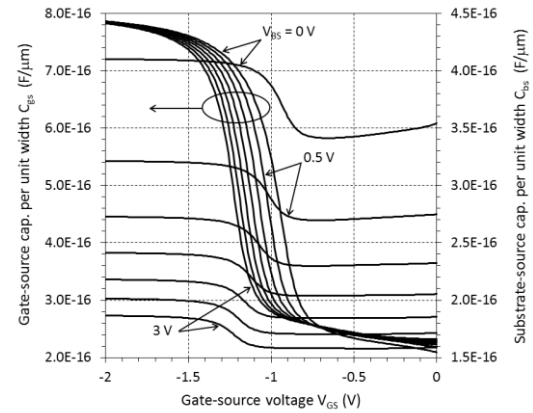
  D. Tomaszewski, et al., "A method for combined characterization of MOSFET threshold voltage and junction capacitance eliminating channel current effect", EUROSOI-ULIS, 2016

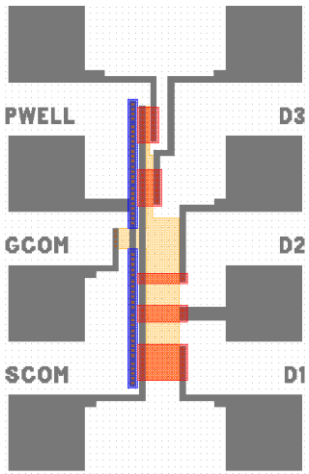
  D. Tomaszewski, et al., "Elimination of the channel current effect on the characterization of MOSFET threshold voltage using junction capacitance measurements", Solid-State El., Feb. 2017

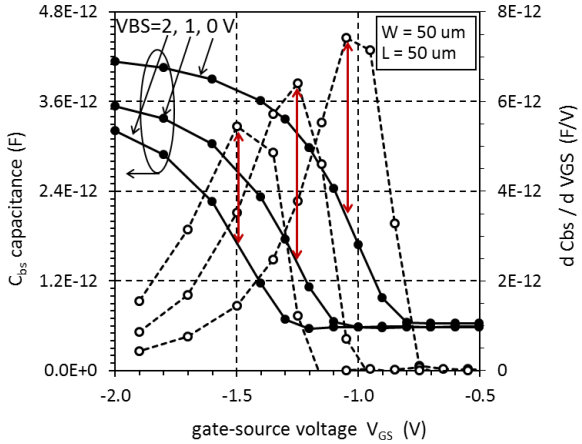
  ✓ serial resistance, mobility degradation effects eliminated

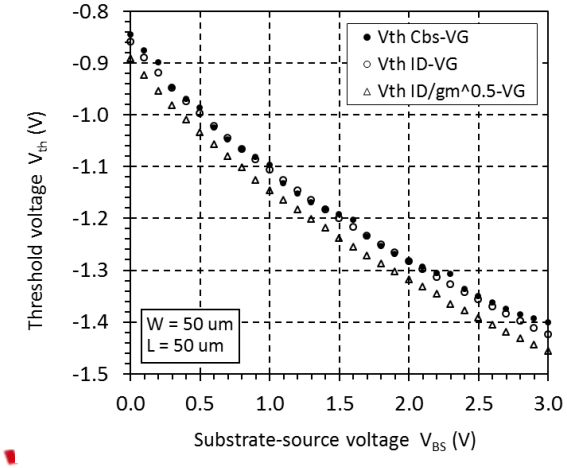










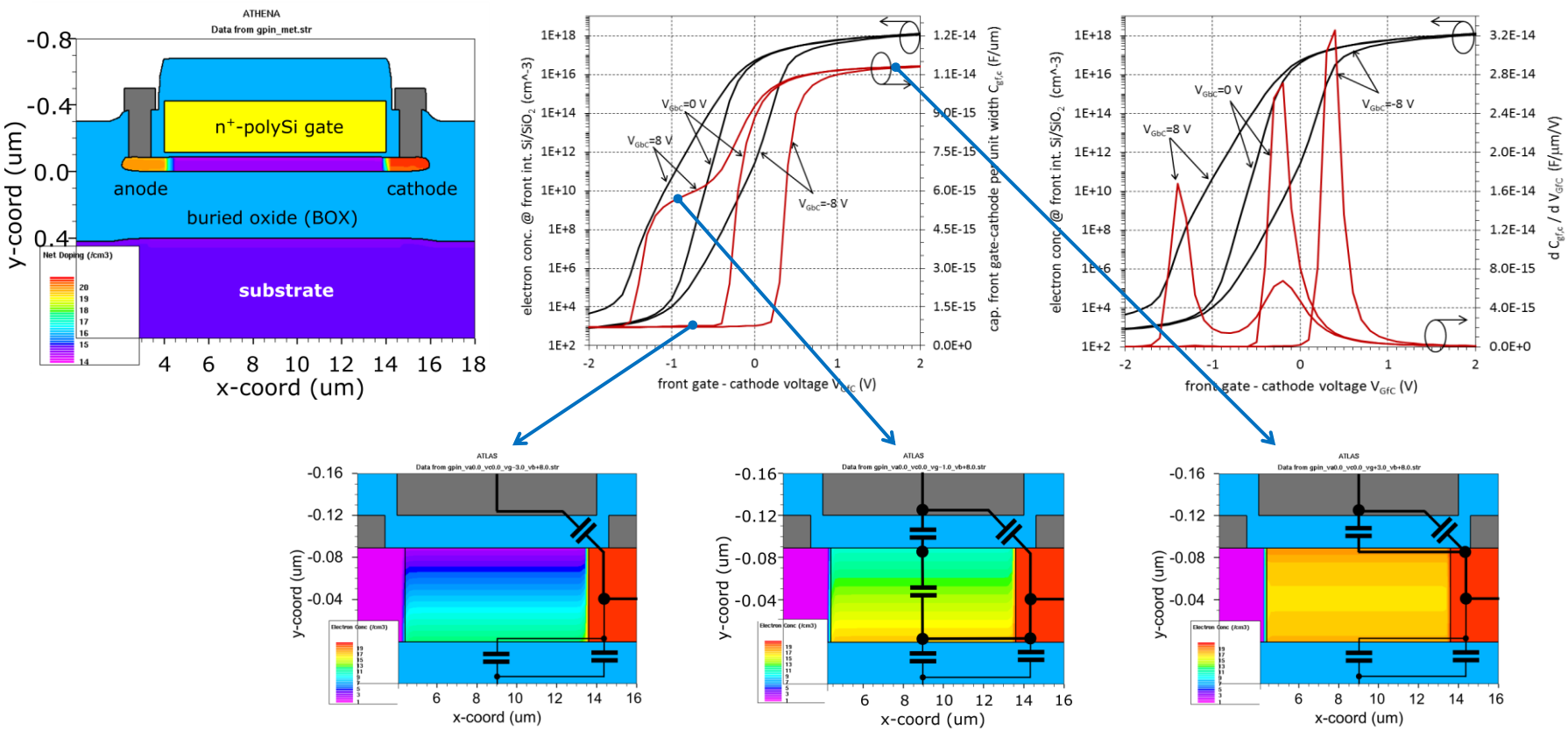


Compact modeling for characterization – parameter extraction methods

- Extraction of the FDSOI MOSFET threshold voltage V_{th}:

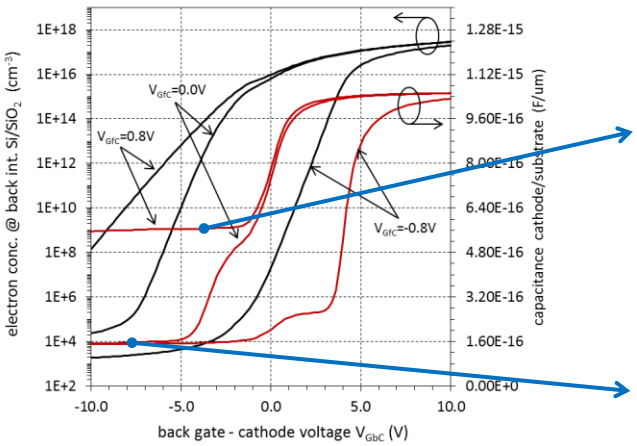
  $V_{th,f}=V_{GfS}$ @ max [$dC_{gf,s}(V_{GfS})/dV_{GfS}$] $V_{th,b}=V_{GbS}$ @ max [$dC_{gb,s}(V_{GbS})/dV_{GbS}$]

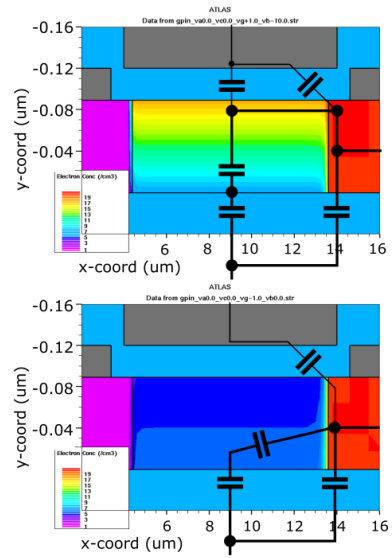
C. Navarro, et al., "Fully Depleted SOI Characterization by Capacitance Analysis of p-i-n Gated Diodes", IEEE EDL., Vol. 36, No. 1, 2015
S. Cristoloveanu, et al., "A review of electrical characterization techniques for ultrathin FDSOI materials and devices", Solid-State El., Vol. 117, No. 3, 2016
D. Tomaszewski, et al., "FDSOI MOSFET threshold voltage characterization based on AC simulation and measurements", Proc. 2017 EUROSOI-ULIS, Athens, April 3-5, 2017

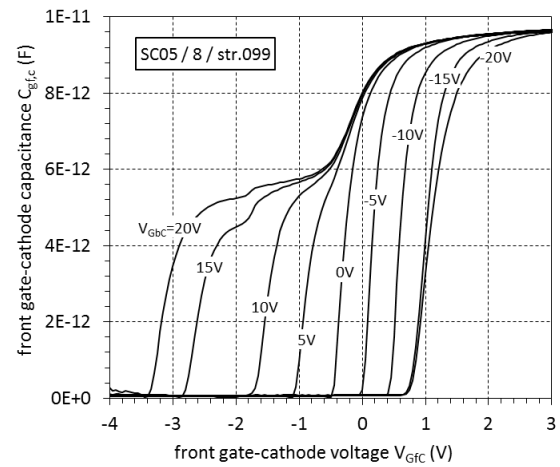


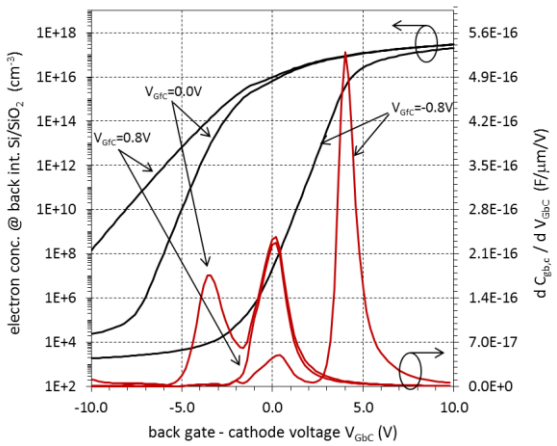
Compact modeling for characterization – parameter extraction methods

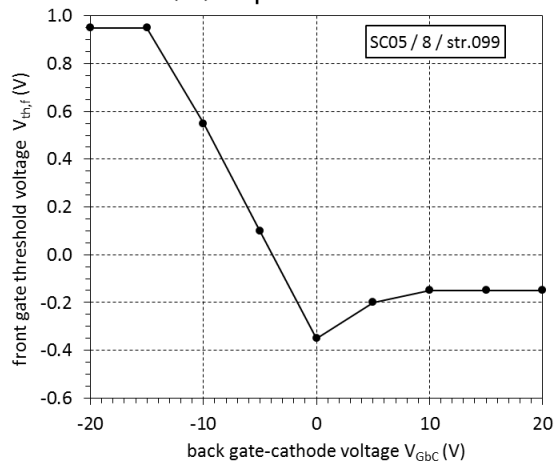
- Extraction of the FDSOI MOSFET threshold voltage V_{th} (cont'd):
  $V_{th,f}=V_{GfS}$ @ max [$dC_{gf,s}(V_{GfS})/dV_{GfS}$] $V_{th,b}=V_{GbS}$ @ max [$dC_{gb,s}(V_{GbS})/dV_{GbS}$]

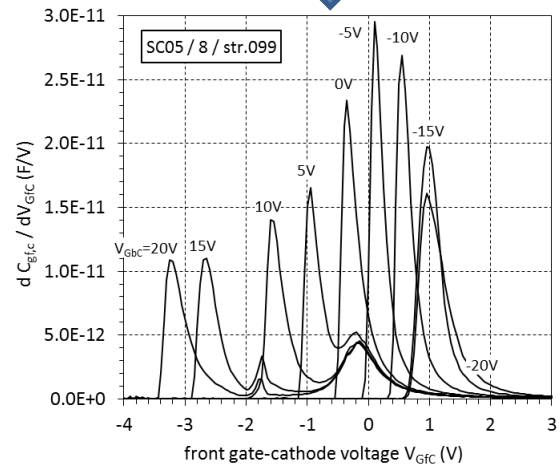












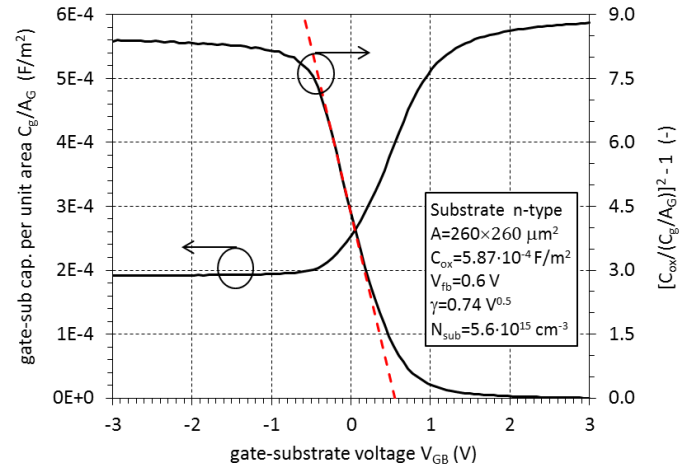
Compact modeling for characterization – parameter extraction methods

▪ Methods using a subset of points of the electrical characteristics

- Extraction of the flat-band voltage V_{fb} and effective doping concentration in MOS structure based on $C_g(V_{GB})$ characteristics:

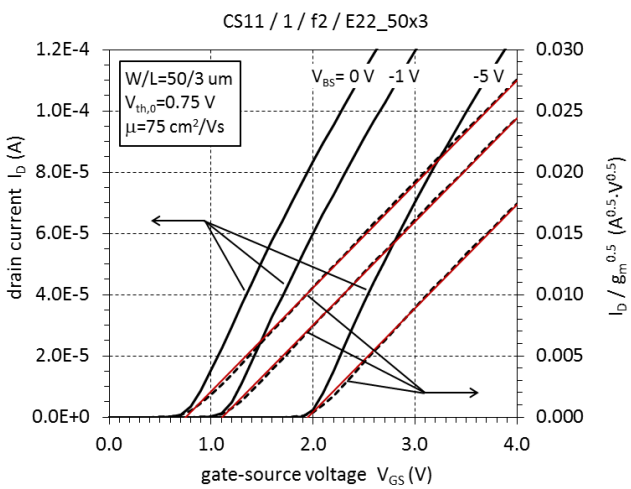
$$\left[C_{ox}/\left(C_{g/gb}/A_G\right)\right]^2 - 1 = t \cdot (V_{GB} - V_{fb})/(\gamma^2/4)$$

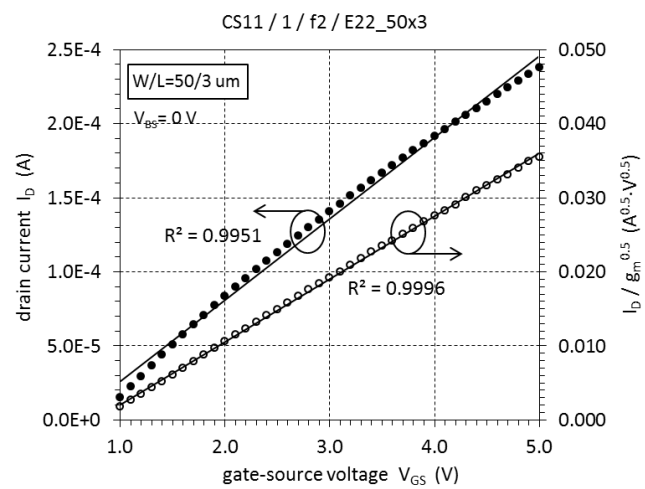
$$\gamma = (2 \cdot q \cdot \varepsilon_{Si} \cdot N_{sub})^{0.5}/C_{ox}$$



- Extraction of the MOSFET threshold voltage V_{th}:

$$I_D/\sqrt{g_m} = \sqrt{(W/L) \cdot \mu_0 \cdot C_{ox}} \cdot (V_{GS} - V_{th})$$





G. Ghibaudo, "New method for the extraction of MOSFET parameters", Electronics Letters, 28th April 1988, vol. 24, no. 9

✓ serial resistance, mobility degradation effects reduced

Compact modeling for characterization – parameter extraction methods

- A method for extracting a subset of the MOSFET EKV model parameters:

C. Enz, F. Krummenacher, E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", J. Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, July 1995

C. C. Enz, E. A. Vittoz, "Charge-based MOS Transistor Modeling:The EKV model for low-power and RF IC design", Wiley, 2006

Model: $V_G = V_{T0} + V_P + \Gamma_b \cdot \left(\sqrt{\Psi_0 + V_P} - \sqrt{\Psi_0}\right)$

Parameters: $I_S, V_{T0}, \Gamma_b, \Psi_0$

D. Tomaszewski, J. Malesińska, G. Głuszko, "Simple Methods of Threshold Voltage Parameter Extraction for MOSFET Models", Proc. MIXDES'2015

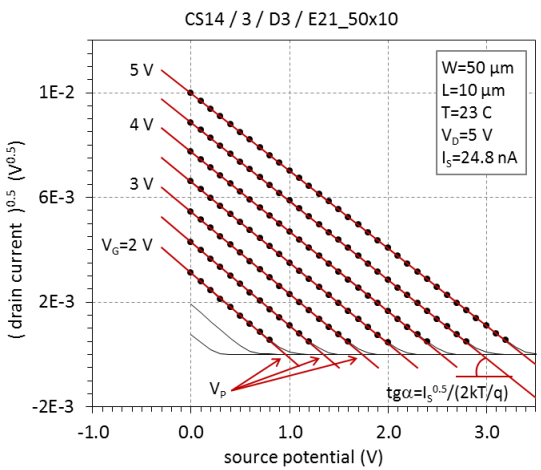
Transform: $V_P + V_{T0} - V_G = 0.5 \cdot \Gamma_b^2/(1 - dV_G/dV_P) + \Gamma_b \cdot \sqrt{\Psi_0}$

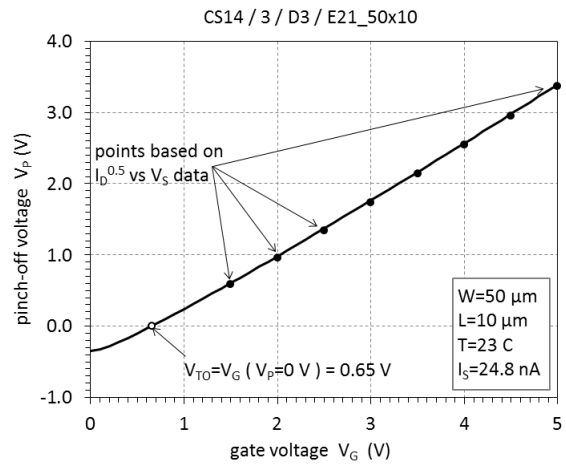
Extraction of I_S:

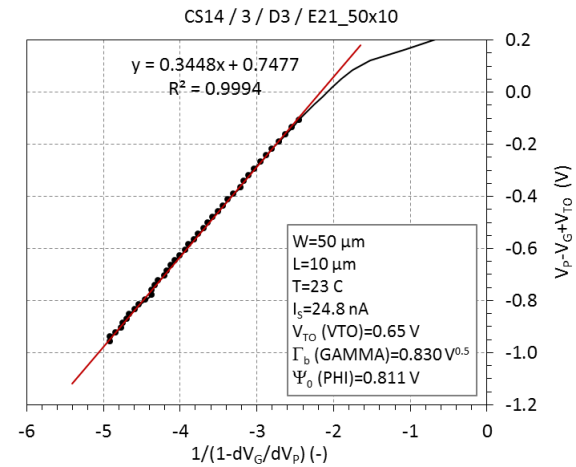
$\sqrt{I_D} = \sqrt{I_S}/(2U_T)\,(V_P - V_S)$

Extraction of $V_P(V_G)$, V_{T0}:

Extraction of Γ_b, Ψ_0







Compact modeling for characterization – parameter extraction methods

- Extraction of series resistances in MOSFETs:

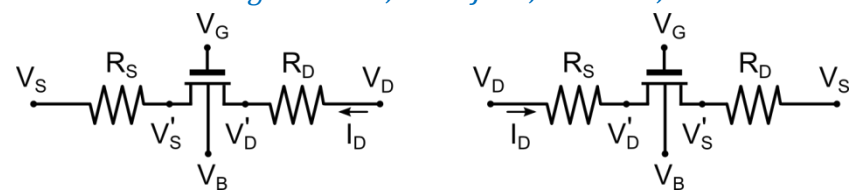
D. Tomaszewski, et al., "A Simple Method for Characterization of MOSFET Serial Resistance Asymmetry", Proc. 28th IEEE Int. Conf. on Microelectronic Test Structures, Phoenix, 23-26.03.2015

In saturation:

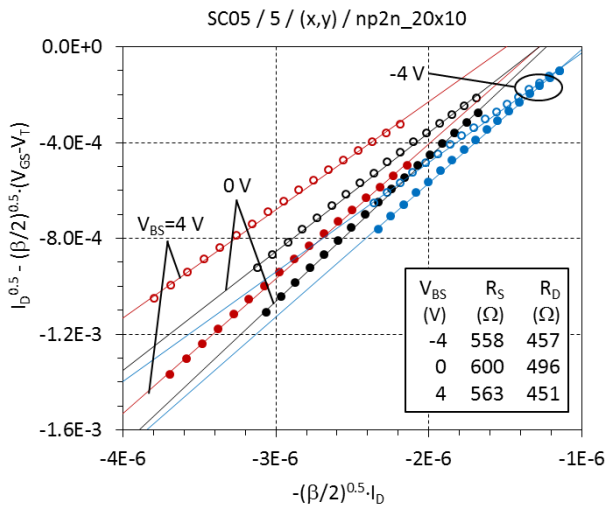
$$I_D = \beta/2 \cdot (V_{GS'} - V_T)^2 = \beta/2 \cdot (V_{GS} - V_T - I_D \cdot R_S)^2$$

$$\sqrt{I_D} - \sqrt{\beta/2} \cdot (V_{GS} - V_T) = -\sqrt{\beta/2} \cdot I_D \cdot R_S$$

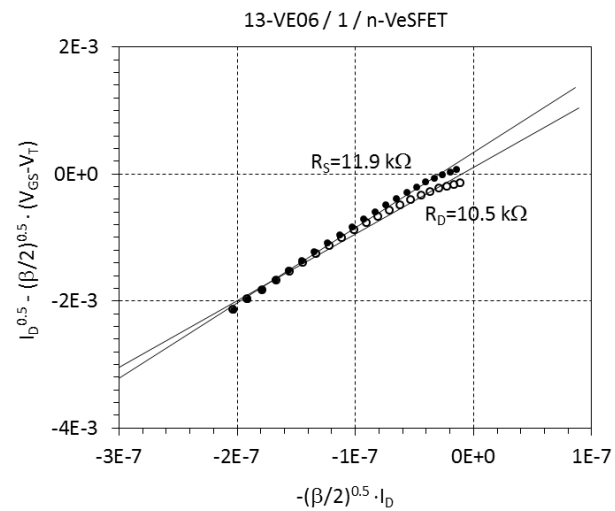
H. Shichman, D. A. Hodges, " Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits", IEEE JSSC, Vol. SC-3, No. 3



FDSOI nMOS



n-VeSFET



Concept: *W. Maly, et al., "Twin gate, vertical slit FET (VeSFET) for highly periodic layout and 3D integration", Proc. MIXDES'2011*

Design, proces: *D.Tomaszewski, K.Domański, G.Głuszko, et al., "MOSFETs in the VeSTIC process - fabrication and characterization", EUROSOI-ULIS'2017*

Compact modeling for characterization – parameter extraction methods

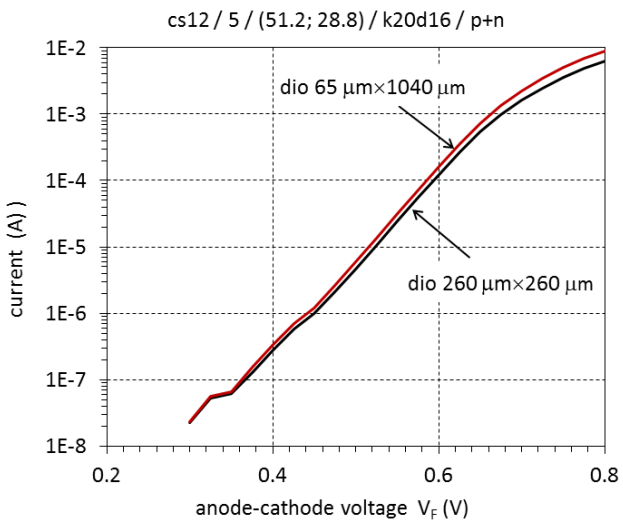
- **Methods using a series of semiconductor devices**

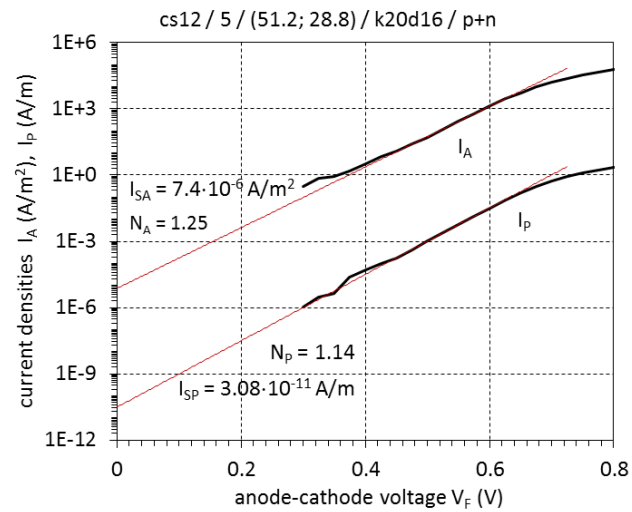
  D. Tomaszewski, A. Bąkowski, J. Gibki, T. Żebrowski, W. Jung, S. Kasjaniuk, "Methods for identification of lifetimes and surface recombination velocity based on electrical characteristics of semiconductor devices", ITE Reports, No. 7, 1993 (in Polish)
  D. Tomaszewski, T. Żebrowski, W. Jung, J. Gibki, A. Bąkowski, M. Hornowski, "Methodology of extraction of capacitance parameters in MOSFET models", ITE Reports, No. 5 7, 1992 (in Polish)
  A. Czerwiński, E. Simoen, C. Claeys, K. Klima, D. Tomaszewski, J. Gibki, J. Kątcki, "Optimized diode analysis of electrical silicon substrate properties", J. Electrochem. Soc., Vol. 145, No. 6

- A method for extraction of the ideality factors N_A, N_P and saturation current densities I_{SA}, I_{SP} of the flat and peripheral parts of the p-n junction

Diodes D_1, D_2

$$I_{1/2}(V_F) = A_{1/2} \cdot I_A(V_F) + P_{1/2} \cdot I_P(V_F) \qquad I_{A/P}(V_F) = I_{SA/P} \cdot \exp\left[V_F/\left(N_{A/P} \cdot U_T\right)\right]$$





Compact modeling for characterization – parameter extraction methods

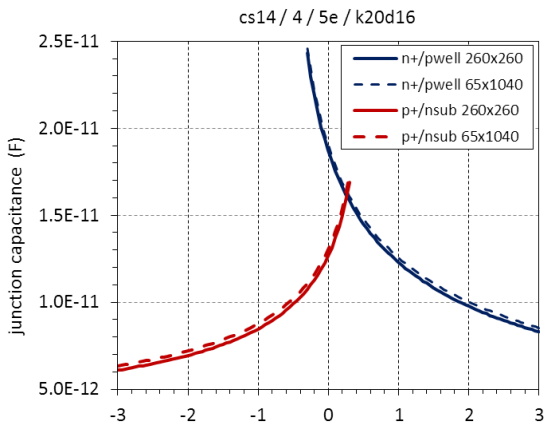
- Extraction of the reverse-biased p-n junction capacitance parameters with account for the plane and peripheral regions

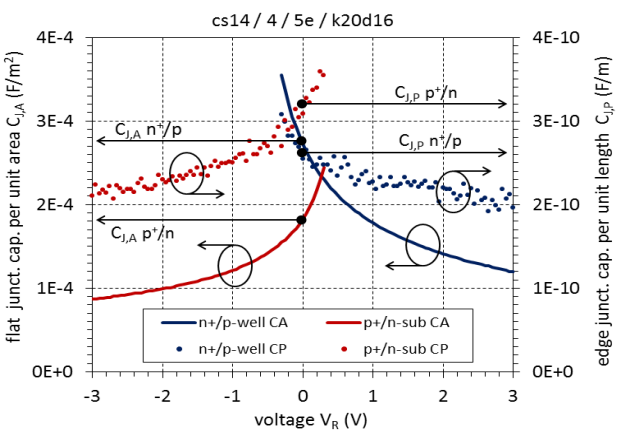
Diodes D_1, D_2

$$C_{1/2}(V_R) = A_{1/2} \cdot C_A(V_R) + P_{1/2} \cdot C_P(V_R)$$

$$C_{A/P}(V_R) = C_{J,A/P} / \left(1 + t \cdot V_R / \phi_{bi,A/P}\right)^{M_{J,A/P}}$$

D. Tomaszewski, et al., "A method for combined characterization of MOSFET threshold voltage and junction capacitance eliminating channel current effect", EUROSOI-ULIS, 2016

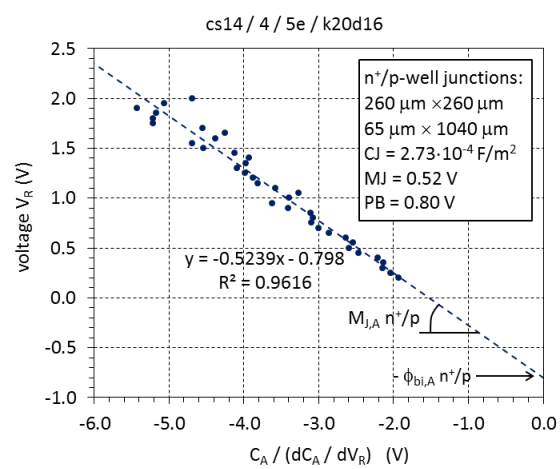


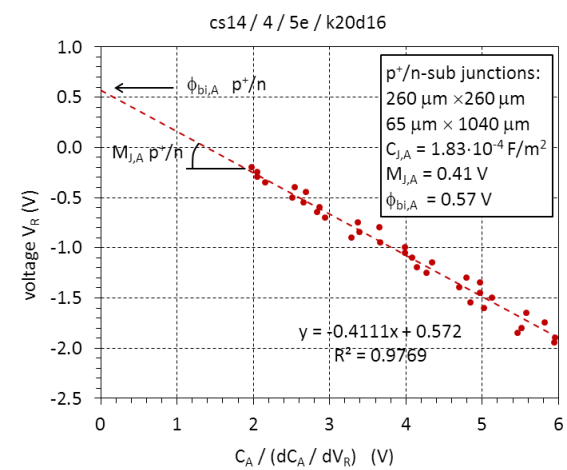


Extraction of $C_{J,A}$, $M_{J,A}$, $\phi_{bi,A}$

$$C_{J,A} = C_A(0)$$

$$V_R = -t \cdot \phi_{bi,A} - M_{J,A} \cdot C_A / (dC_A / dV_R)$$



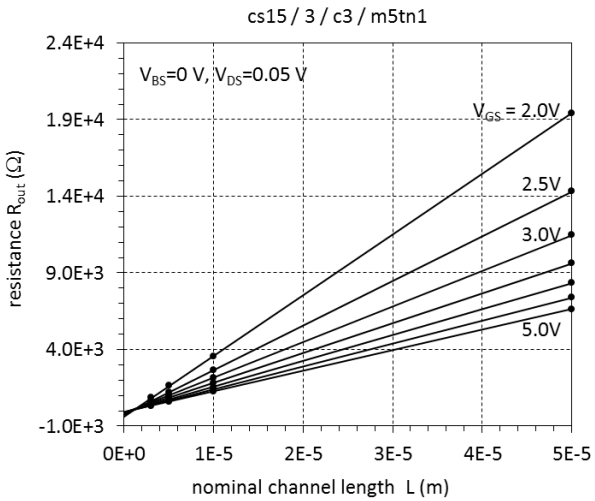


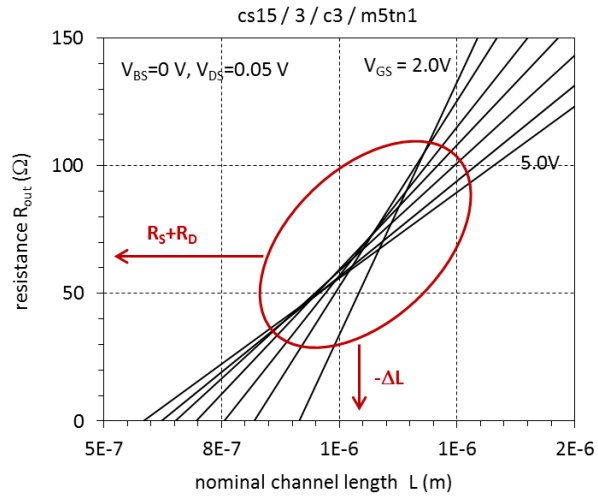
Compact modeling for characterization – parameter extraction methods

- Extraction of the MOSFET channel shortening ΔL and total serial source and drain resistance R_S+R_D

J. G. J. Chern, et al., "A New Method To Determine MOSFET Channel Length", IEEE Electron Device Letters, EDL-1, No.9, 1980

$$R_{out} = V_{DS}/I_D = [(L + \Delta L)/W]/[K_P \cdot (V'_{GS} - V_T - V'_{DS}/2)] + (R_S + R_D)$$



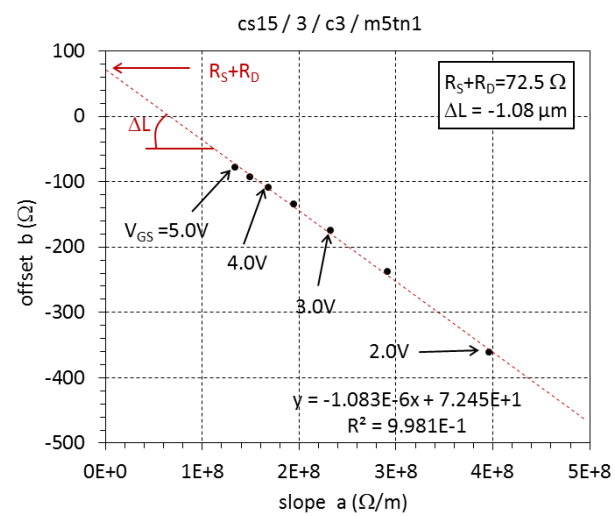


W=50 µm,
L= 50, 10, 5, 3 µm

S. E. Laux, "Accuracy of an Effective Channel Length/External Resistance Extraction Algorithm for MOSFET's", IEEE Trans. Electron Devices, Vol. 31, No. 9, 1984

$$R_{out} = a \cdot (L + \Delta L) + (R_S + R_D) = a \cdot L + b$$

a, b are correlated: $b = a \cdot \Delta L + (R_S + R_D)$



Compact modeling for characterization – parameter extraction methods

- Extraction of fringing capacitances in the MOSFETs: gate-source/drain C_{gso}, C_{gdo} and gate-substrate C_{gbo} with account for channel size variation

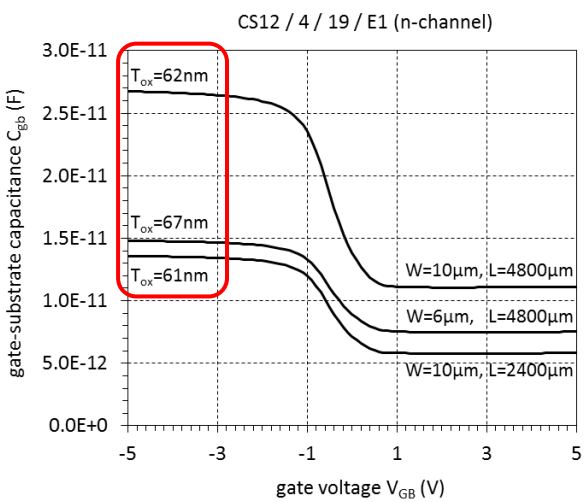
D. Tomaszewski, T. Żebrowski, W. Jung, J. Gibki, A. Bąkowski, M. Hornowski, "Methodology of extraction of capacitance parameters in MOSFET models", ITE Reports, No. 5 7, 1992 (in Polish)
M. Sadowski, D. Tomaszewski, "An efficient approach to the measurement and characterization of MOSFET capacitances", Microelectronics Reliability, Vol. 40, No. 6

Example: C_{gbo} & ΔW

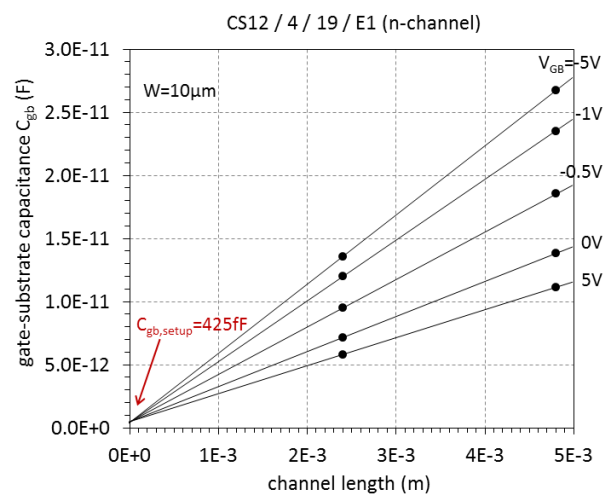
D. Tomaszewski, G. Głuszko, J. Malesińska, "A method for characterization of gate overlap capacitances and effective channel size in MOSFETs", EUROSOI-ULIS, March 19–21, 2018, Granada; selected for publication in SSE

$$C_{gb} = C_{gb,setup} + L \cdot C_{gbo} + (W + \Delta W) \cdot L \cdot C'_{gb}(V_{GB})$$

Data:



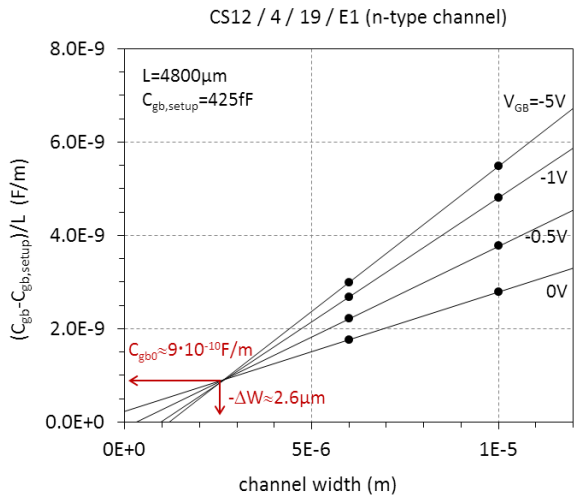
$C_{gb,setup}$:

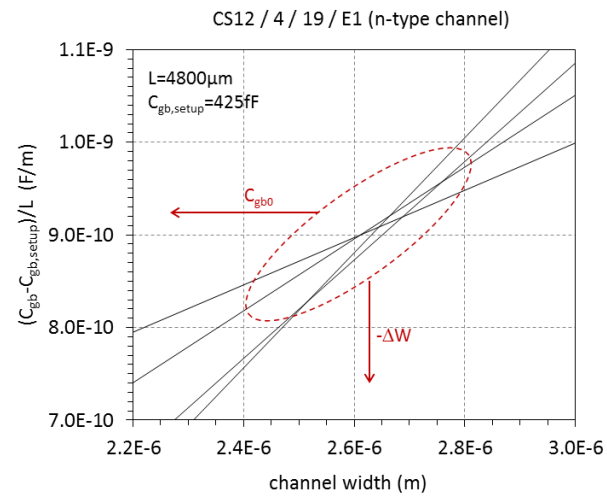


Compact modeling for characterization – parameter extraction methods

- Extraction of fringing capacitances in the MOSFETs: C_{gbo} & ΔW (cont'd)

rough estimation:





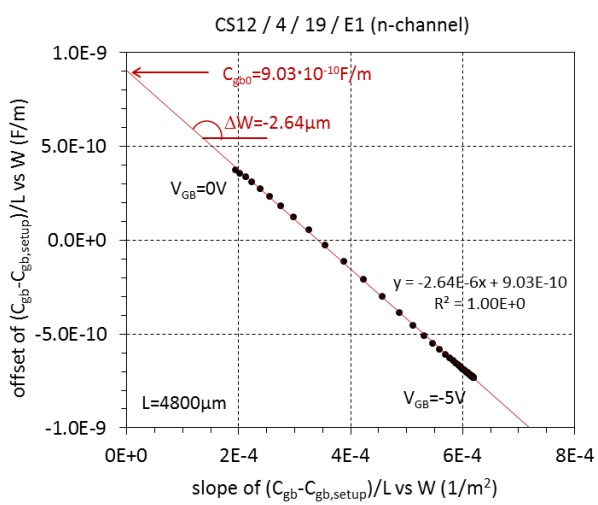
estimation based on

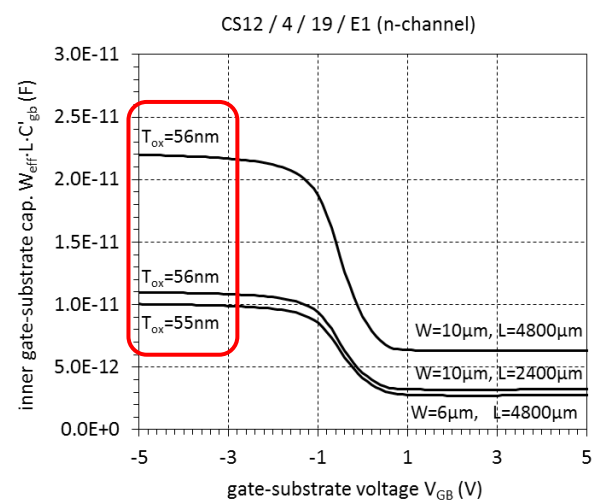
$$(C_{gb} - C_{gb,setup})/L = C'_{gb}(V_{GB}) \cdot W + C'_{gb}(V_{GB}) \cdot \Delta W + C_{gbo} = a \cdot W + b$$

and correlation: b vs a

$a(V_{GB}) \Rightarrow C'_{gb}(V_{GB})$

improved T_{ox} estim.



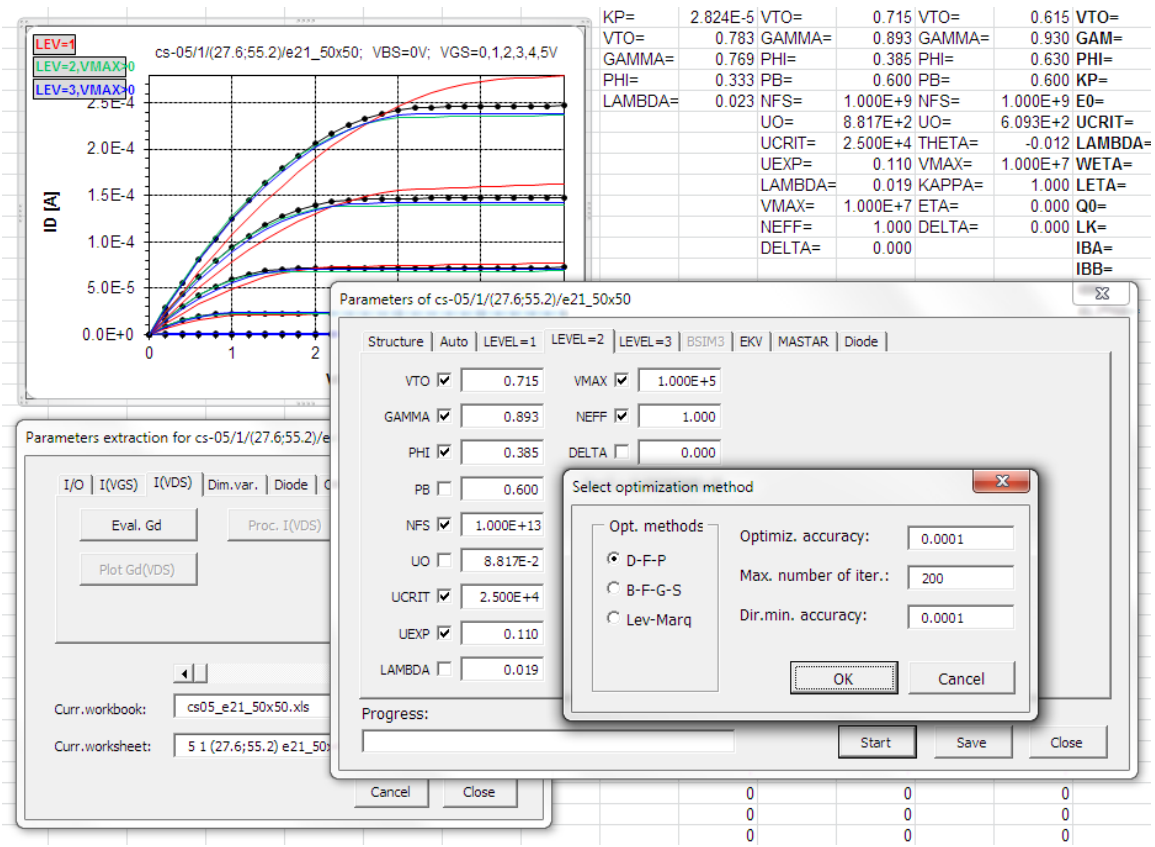


Compact modeling for characterization – parameter extraction methods

- **Methods based on optimization**

$$mse(\boldsymbol{P}) = \sum_{i=1}^{n} \left[I^{mod}(\boldsymbol{V}_i, \boldsymbol{P}) - I^{ref}(\boldsymbol{V}_i) \right]^2$$

- Parameter "local" extraction with use of optimization (MS Excel VBA)



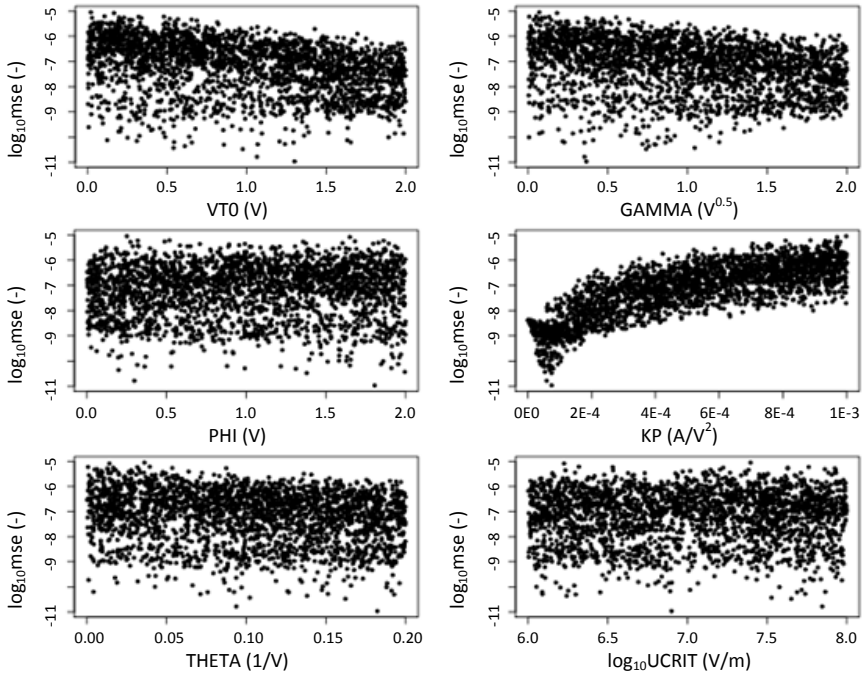
D. Tomaszewski, A. Kociubiński, J. Marczewski, K. Kucharski, K. Domański, P. Grabiec: "A Versatile Tool for Extraction of MOSFETs Parameters", Proc. 6th Symposium "Diagnostics & Yield: Advanced Silicon Devices and Technologies for ULSI Era", Eds. A. Jakubowski, L. Łukasiak, June 22-25, 2003, Warsaw

Compact modeling for characterization – parameter extraction methods

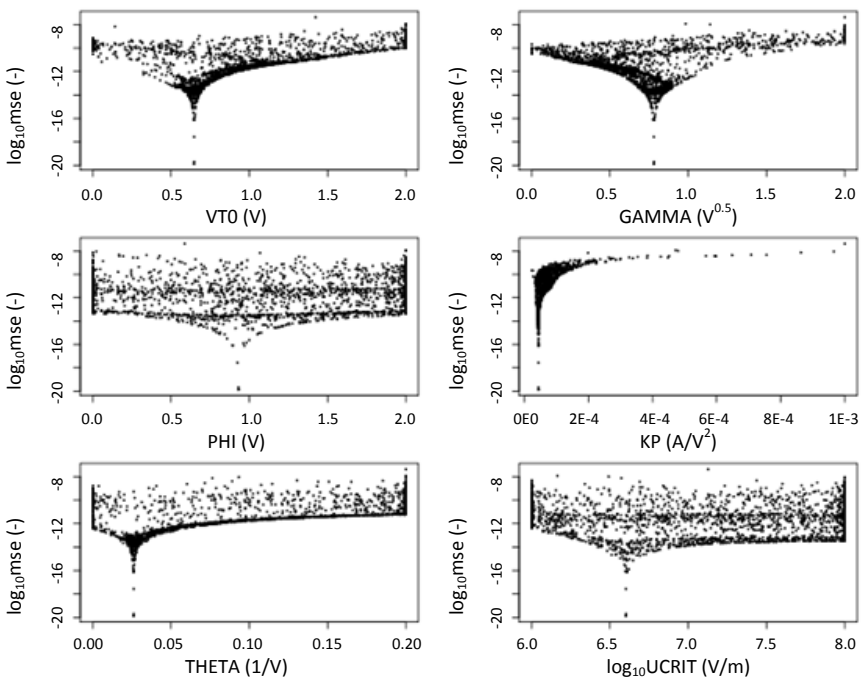
- Parameter "global" extraction with use of evolutionary algorithms

J. Arabas, Ł. Bartnik, S. Szostak, D. Tomaszewski, "Global Extraction of MOSFET Parameters Using the EKV Model: Some Propertiesd of the Underlying Optimization Task", Proc. 16th Int. Conf. Mixed Design of Integrated Circuits and Systems MIXDES, Łódź, June 25-27, 2009

Evolutionary algorithms have a "tendency" to look for the global minimum of mse



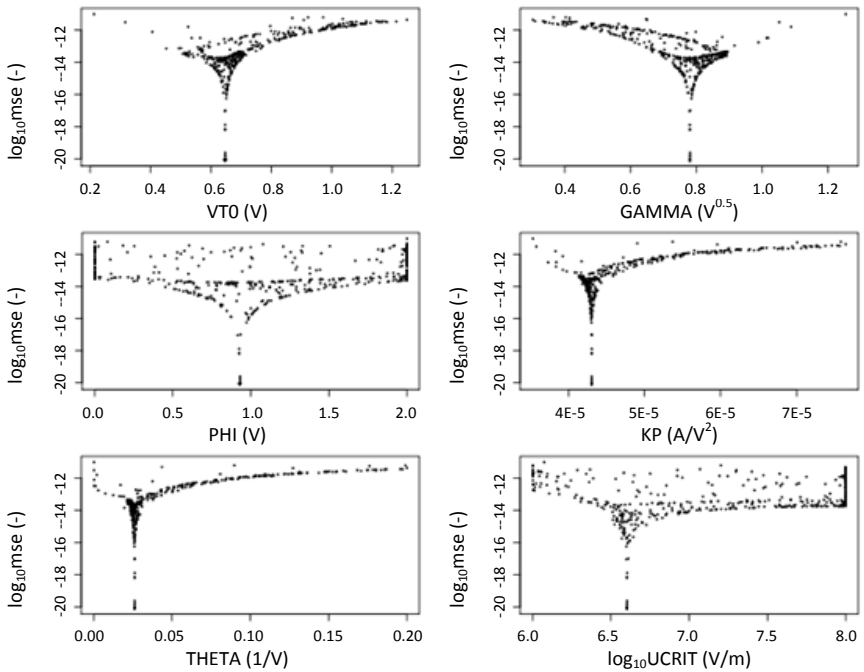
random exploration
of parameter space



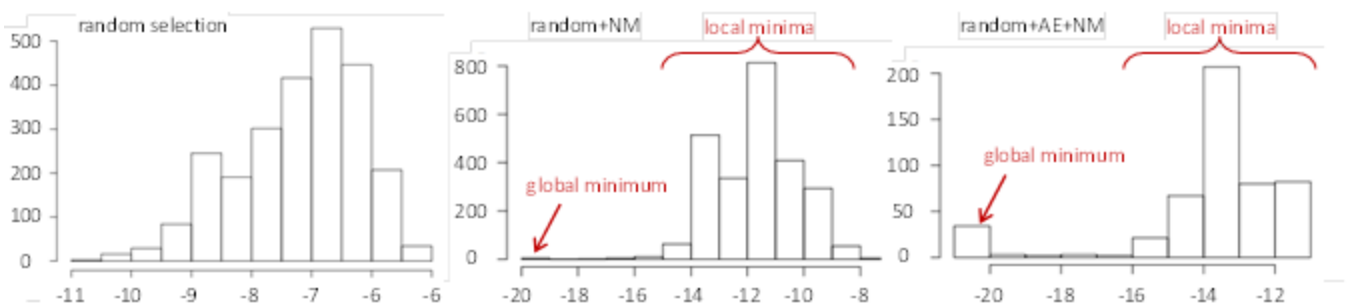
random exploration
of parameter space + N-M

Compact modeling for characterization – parameter extraction methods

- Parameter "global" extraction with use of evolutionary algorithms (cont'd)



random exploration of param. space +
evolutionary algorithm +
N-M



Compact modeling for characterization – parameter extraction methods

▪ Methods for variability characterization

- Global variability
  - Principal component analysis (PCA)
  - Forward propagation of variances (FPV)
  - Backward propagation of variances (BPV)

C. C. McAndrew, "Statistical Modeling for Circuit Simulation", Proc. Fourth Int. Symposium on Quality Electronic Design (ISQED'03)
C. C. McAndrew, "Statistical Modeling Using Backward Propagation of Variance (BPV)" w "Compact Modeling: Principles, Techniques and Applications", G. Gildenblat (Ed.), Springer 2010

$$\mathbf{X}(\mathbf{P},\mathbf{M},\mathbf{V}) = \mathbf{X}(\mathbf{P}_{\mathbf{nom}} + \boldsymbol{\delta}\mathbf{P},\mathbf{M},\mathbf{V}) - \mathbf{X}(\mathbf{P}_{\mathbf{nom}},\mathbf{M},\mathbf{V}) = \mathbf{S}(\mathbf{P}_{\mathbf{nom}},\mathbf{M},\mathbf{V})\cdot\boldsymbol{\delta}\mathbf{P}$$

$$\sigma^2(\delta X_i) = \sum_{j=1}^{NP}\left[S_{ij}(\mathbf{P}_{\mathbf{nom}},\mathbf{M},\mathbf{V})\right]^2 \cdot \sigma^2(\delta P_j);\ \ i = 1,2,\ldots,N_X \rightarrow \sigma^2(\delta P_j);\ \ j = 1,2,\ldots,N_P$$

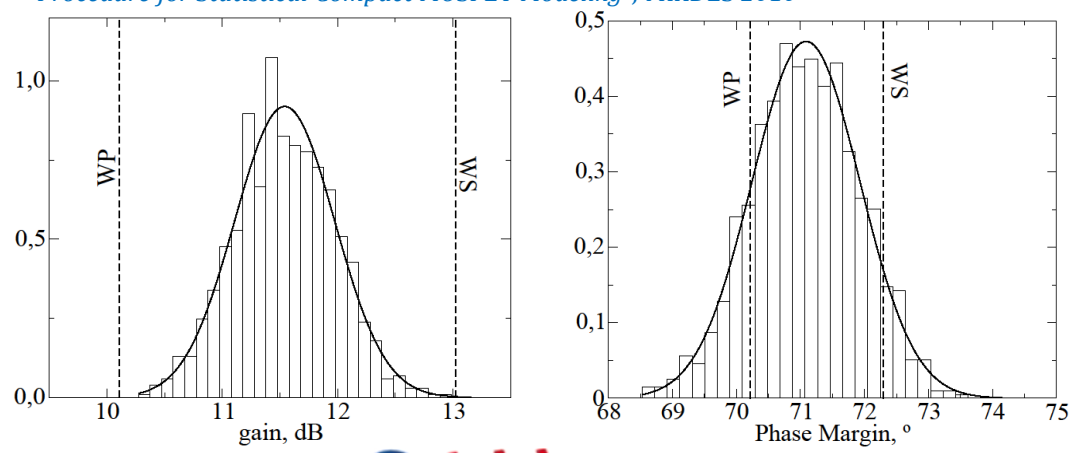
M. Yakupov, D. Tomaszewski, W. Grabiński, "Process Control Monitor Based Extraction Procedure for Statistical Compact MOSFET Modeling", MIXDES'2010

FDSOI CMOS process (UCL)

process parameters:
ln(NSUB), TOX, UO, DW, DL

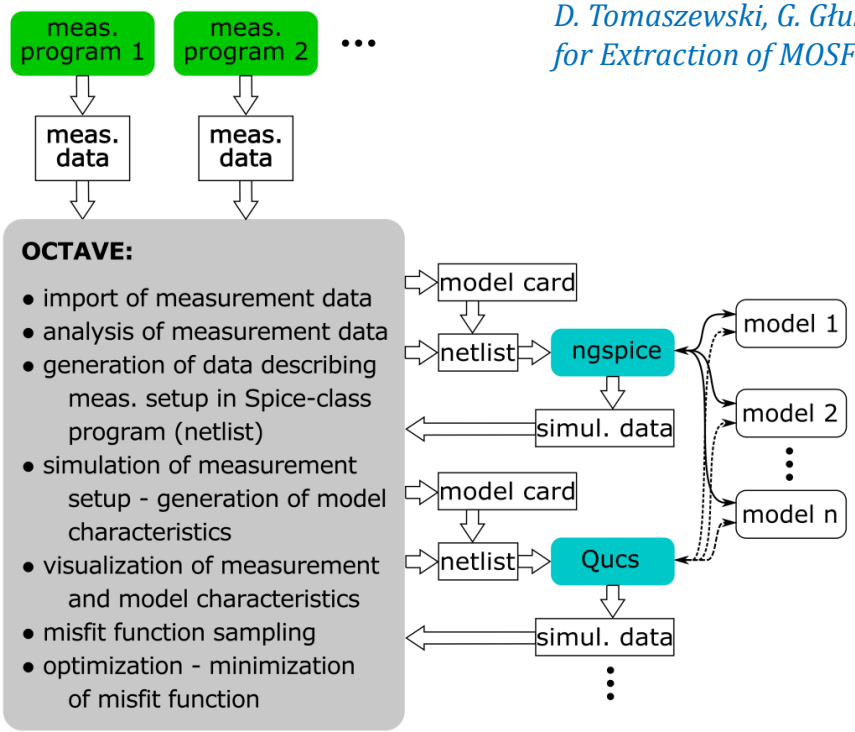
six-transistor op-amp

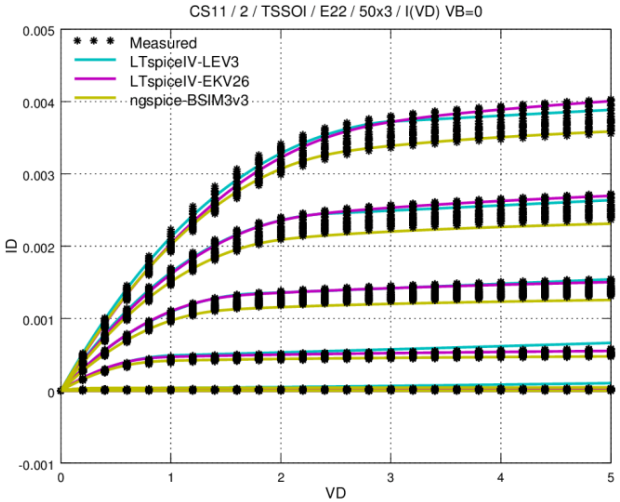
M-C simulations

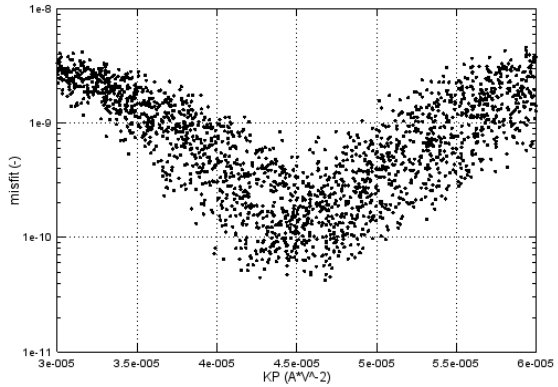


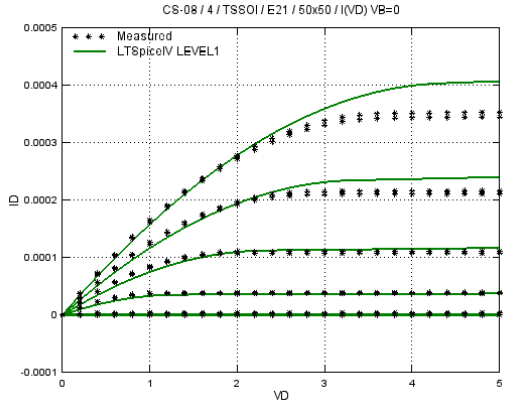
Integrated tools for modeling and parameter extraction

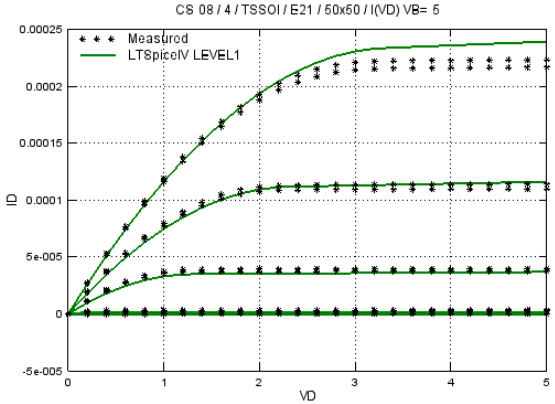
D. Tomaszewski, G. Głuszko, M. Brinson, V. Kuznetsov, W. Grabinski, "FOSS as an Efficient Tool for Extraction of MOSFET Compact Model Parameters", MIXDES'2016











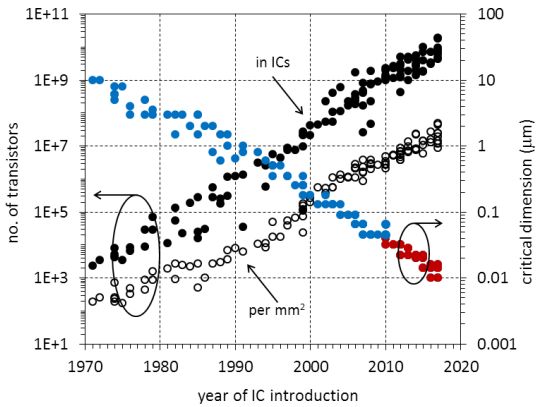
Compact modeling for IC design

- **Nominal design**

- **Design with account for process variability**

- Corner/PVT (Process, Voltage, Temperature) method
- Monte-Carlo (MC) method
- Worst-Case Distance (WCD) method: yield maximization

K. J. Antreich, H. E. Graeb, C. U. Wieser, "Circuit Analysis and Optimization Driven by Worst-Case Distances", IEEE TCAD-ICAS, Vol. 13, No. 1
H. E. Graeb, "Analog Design Centering and Sizing", Springer, 2007



after https://en.wikipedia.org/wiki/Transistor_count

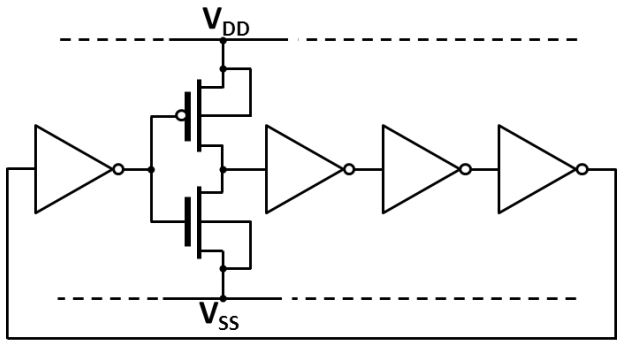
- Cummulative distribution function (CDF) – based approach: yield maximization

M. Yakupov, D. Tomaszewski, "Analysis of selected methods for CMOS integrated circuit design for yield optimization", MIXDES'2011
M. Yakupov, D. Tomaszewski, "Parametric Yield-oriented IC Design Based on Cumulative Distribution Function and Open-Source EDA Tools", MOS-AK/GSA Workshop at ESSDERC/ESSCIRC, 2012

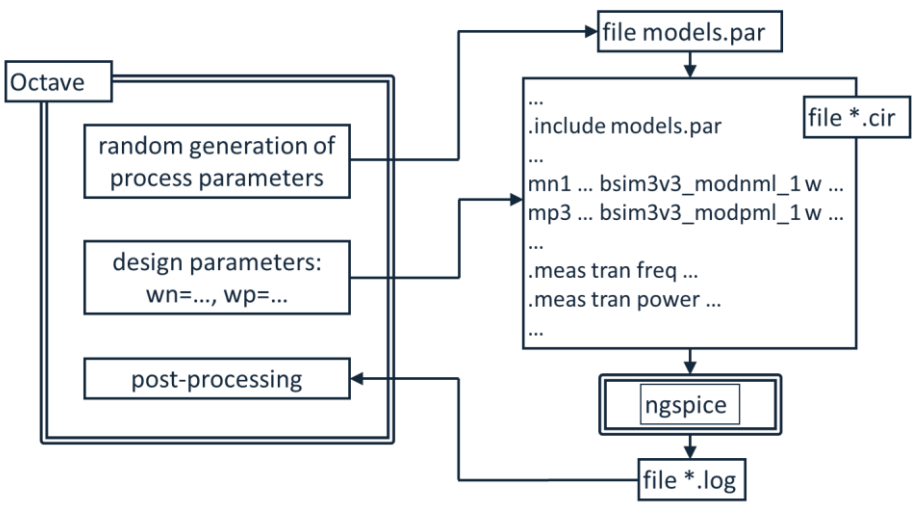
$$Z_i = \sum_{j}^{NP} (\partial X_i / P_j) \cdot \delta Pj \,;\, i = 1, \dots, N_X; j = 1, \dots, N_P$$

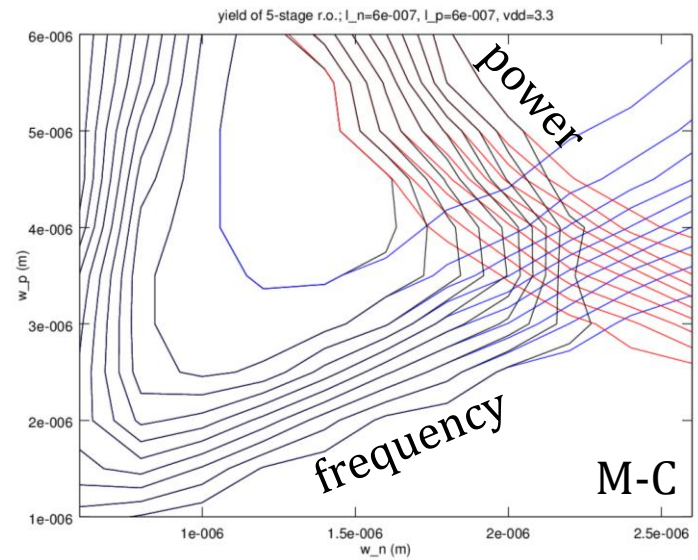
$$Y_{joint} = \prod_{i=1}^{NX} Y_i = \prod_{i=1}^{NX} \left\{ F_{Zi}\left[X_{i,max} - X_i(\mathbf{D}, \mathbf{M}, \mathbf{P_{nom}})\right] - F_{Zi}\left[X_{i,min} - X_i(\mathbf{D}, \mathbf{M}, \mathbf{P_{nom}})\right] \right\}$$

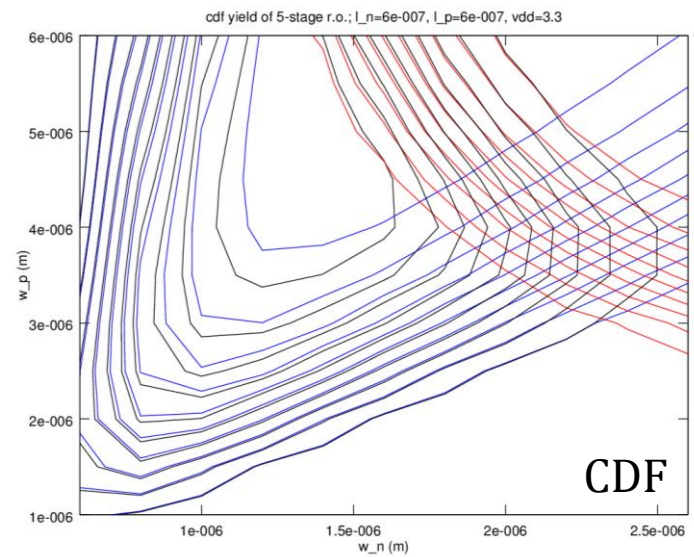
Compact modeling for IC design – a simple example



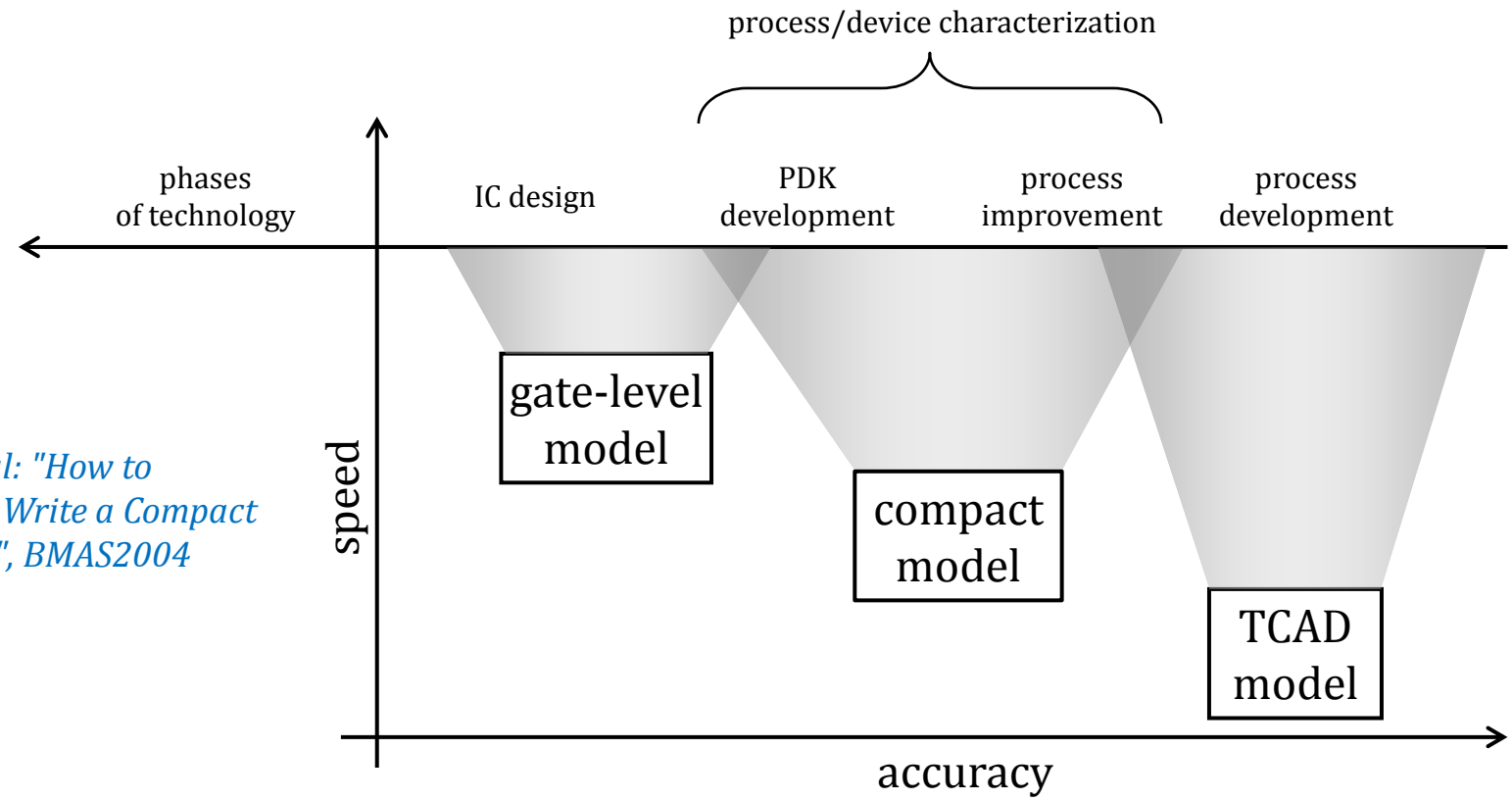
- CMOS process; V_{DD}=3.3 V
- Globar variability taken into account
- **Aim:** design 5-stage RO ($P \le P_{max}$; $f_{min} \le f \le f_{max}$) for the maximum yield; $L_{n,p}$=0.6µm; W_n, W_p=?
- BSIM3v.3 model used







Semiconductor device compact modeling - summary



G.J. Coram, Tutorial: "How to (and How NOT to) Write a Compact Model in Verilog-A", BMAS2004

What is a Compact Model ?

- A model of transistor currents & voltages
- Built from physically-motivated equations
- Intended for use in an analog circuit simulator

Compact modeling is a versatile tool for development/application of micro- and nanoelectronic technologies

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