

TCAD-Based Statistical Modelling Methodology for Nanoscale FinFET Variability

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- **Introduction**
- **TCAD Simulation & Base SPICE Model**
- **FinFET Variabilities & Statistical Model**
- **Summary**

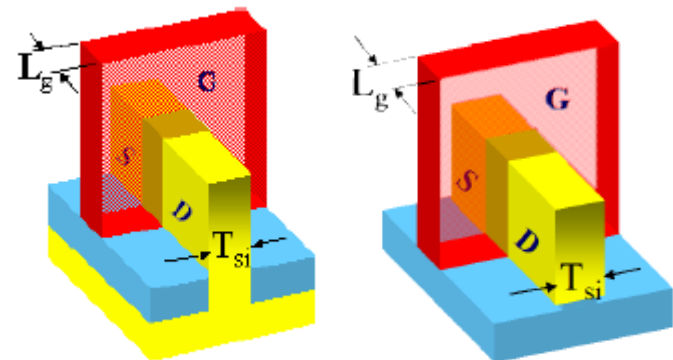
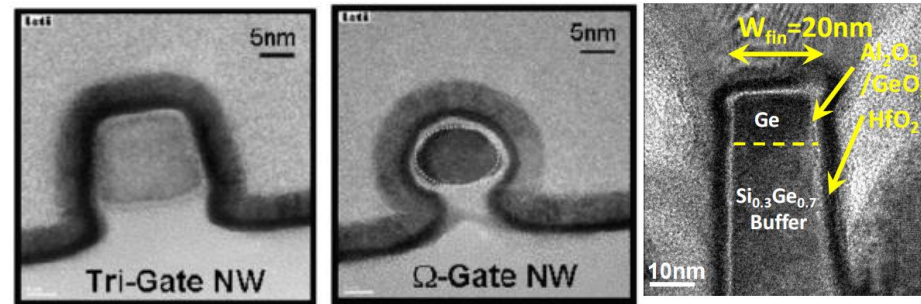
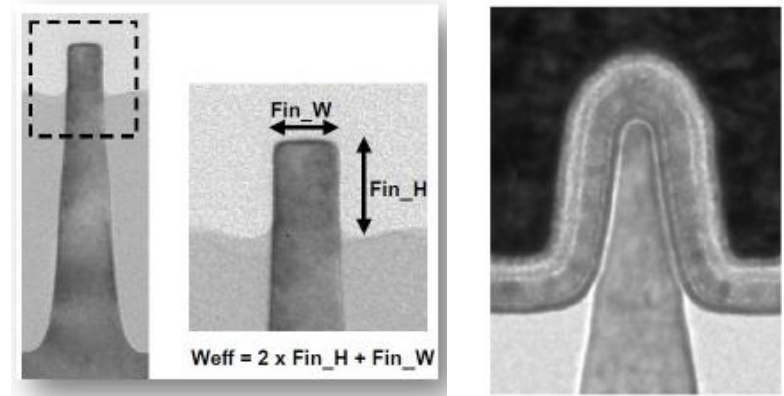
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➤ Various Structures

➤ Technology

- Substrate: Bulk and SOI
- Channel: Si, SiGe, Ge, InGaAs, ...

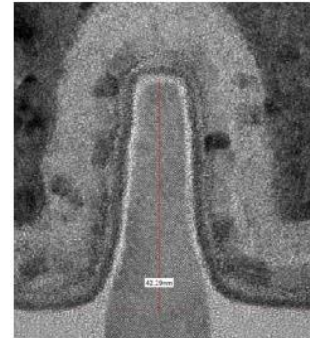
➤ Production Adoption for 16/14/10/7nm



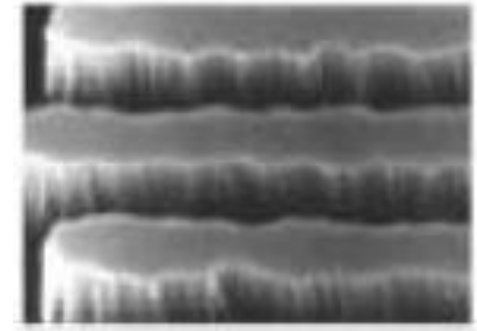
Bulk vs. SOI

➤ Various sources

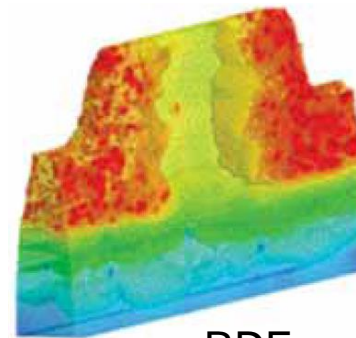
- Random:
 - RDF, LER, MGG
- Systematic:
 - Fin dimension (width/height/pitch)
 - Gate dimension (width/length/pitch)
 - Epi/Spacer/CT...



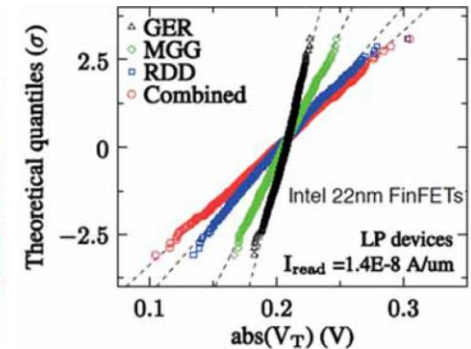
MGG



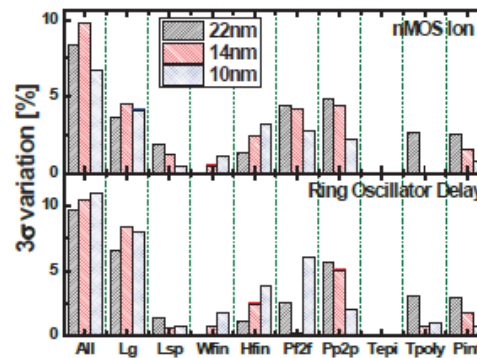
LER



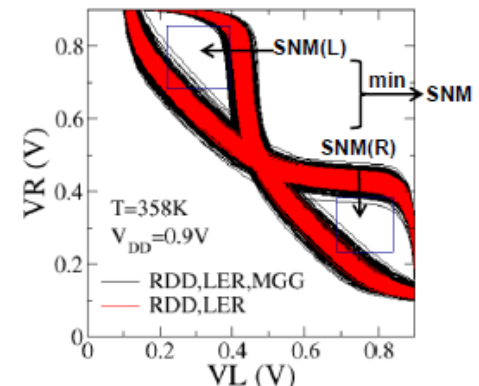
RDF



➤ Serious impacts on circuit performance



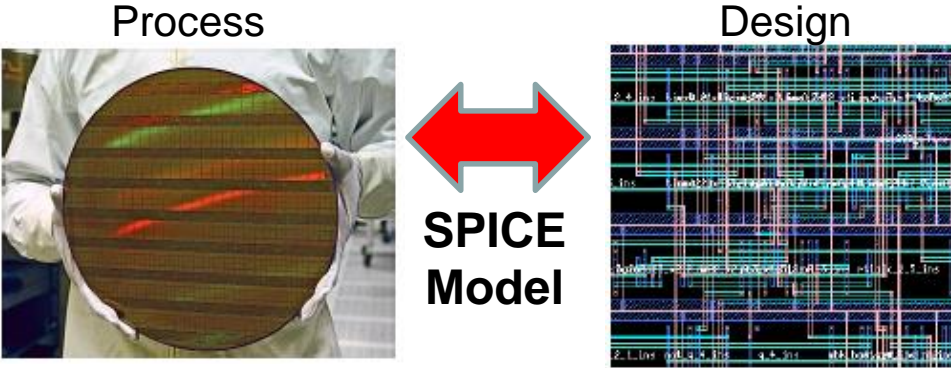
Logic RO delay



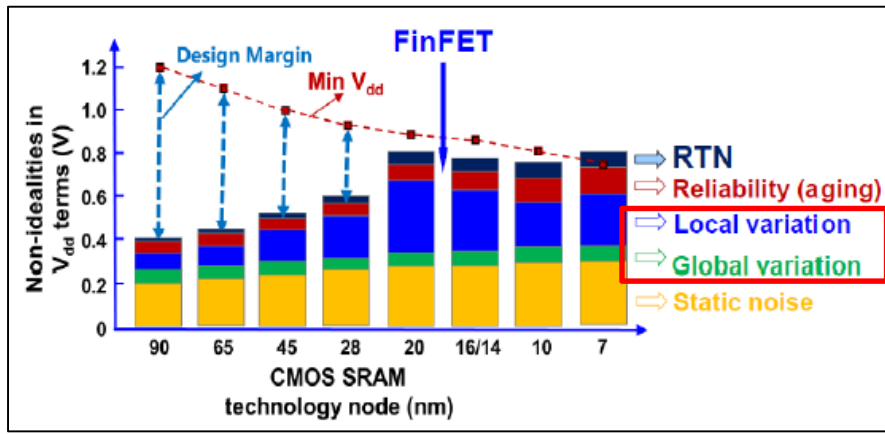
SRAM SNM

Critical Role of Statistical Model

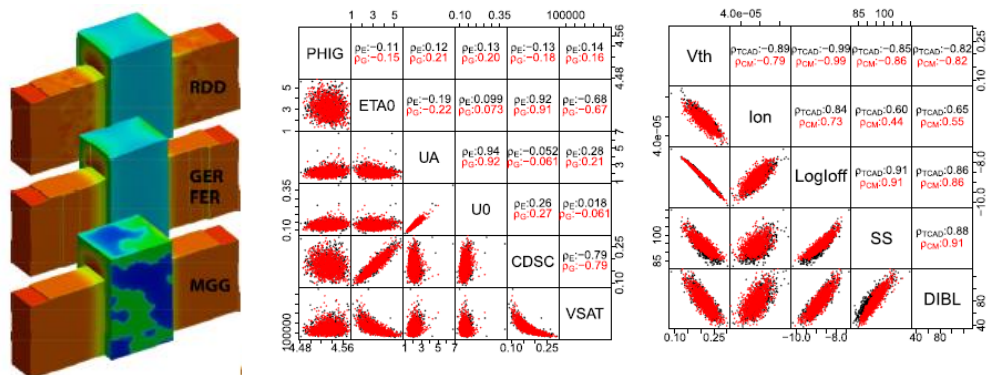
➤ SPICE model is the bridge b/w Process and Design



- FinFET process variability
➔ More challenges for circuit design
- Accurate statistical model is critical



➤ TCAD is widely used for variation analysis and model study

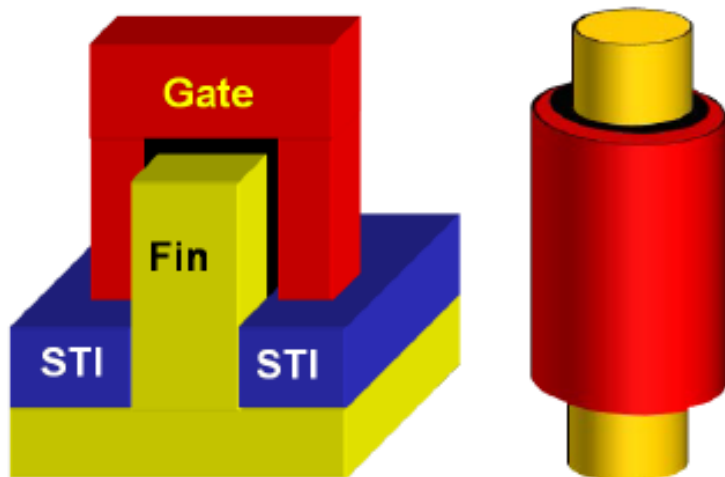


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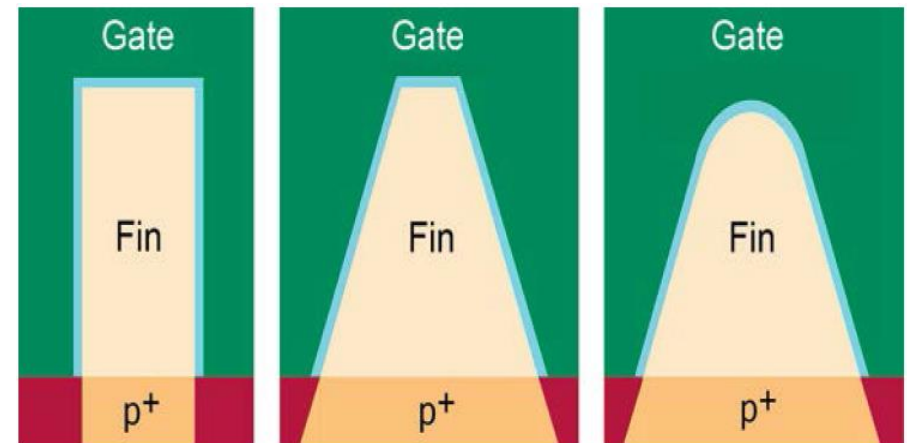
➤ Selected as Industry standard since 2012

- Surface-potential-based core I-V and C-V model
- Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates
- Supports various Fin shapes

Various Gate Types

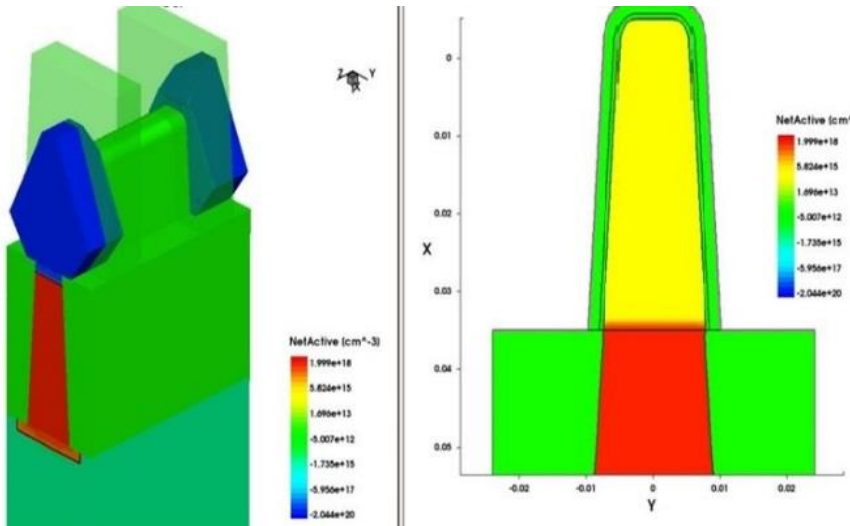


Various Fin Shapes

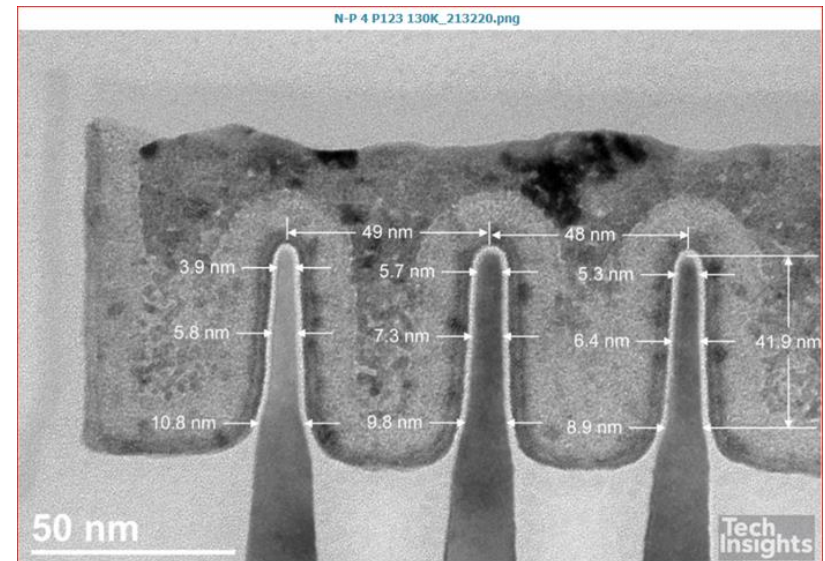


- **Strain consideration: 4 regions**
 - source/drain、STI、Metal Gate and contact metal
- **Key parameters:**

Fin Height	Fin Pitch	Fin Width	Gate Length	Gate Pitch	EOT
42nm	48nm	8nm	20nm	90nm	10.4Å

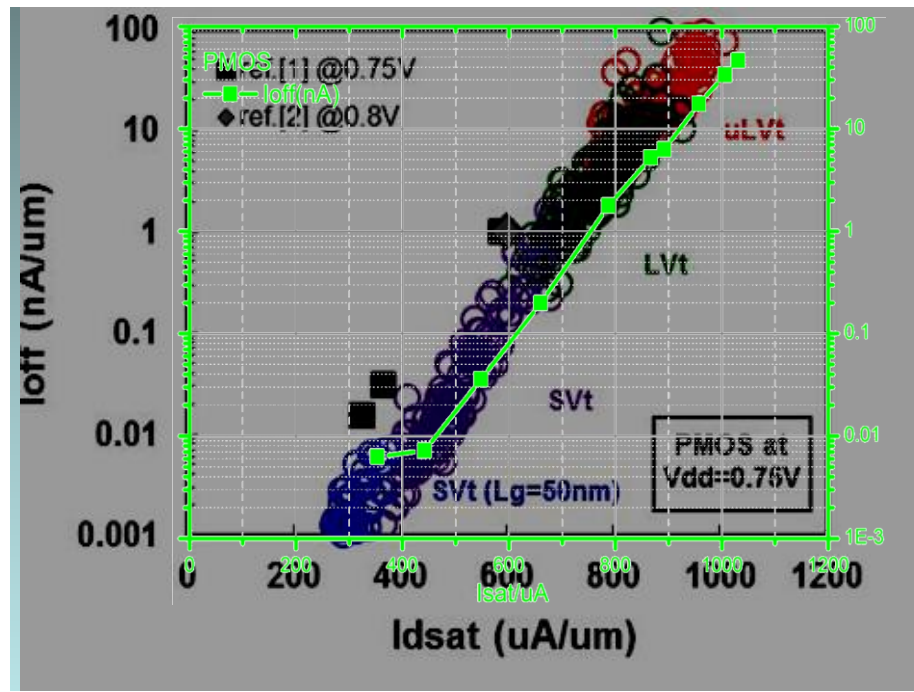


TCAD Structure

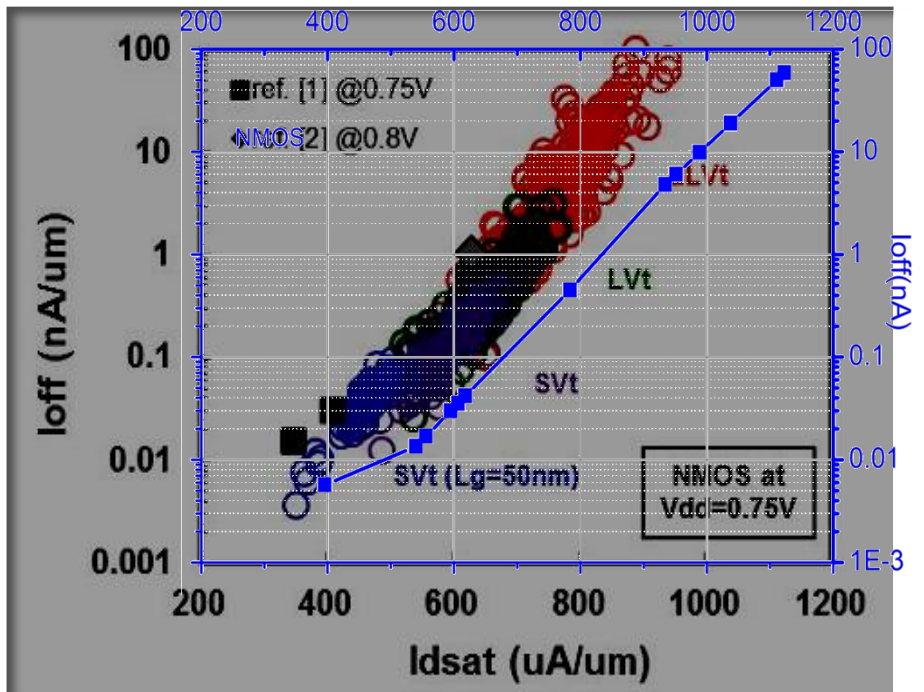


Reference

PMOS Ion vs. Ioff



NMOS Ion vs. Ioff



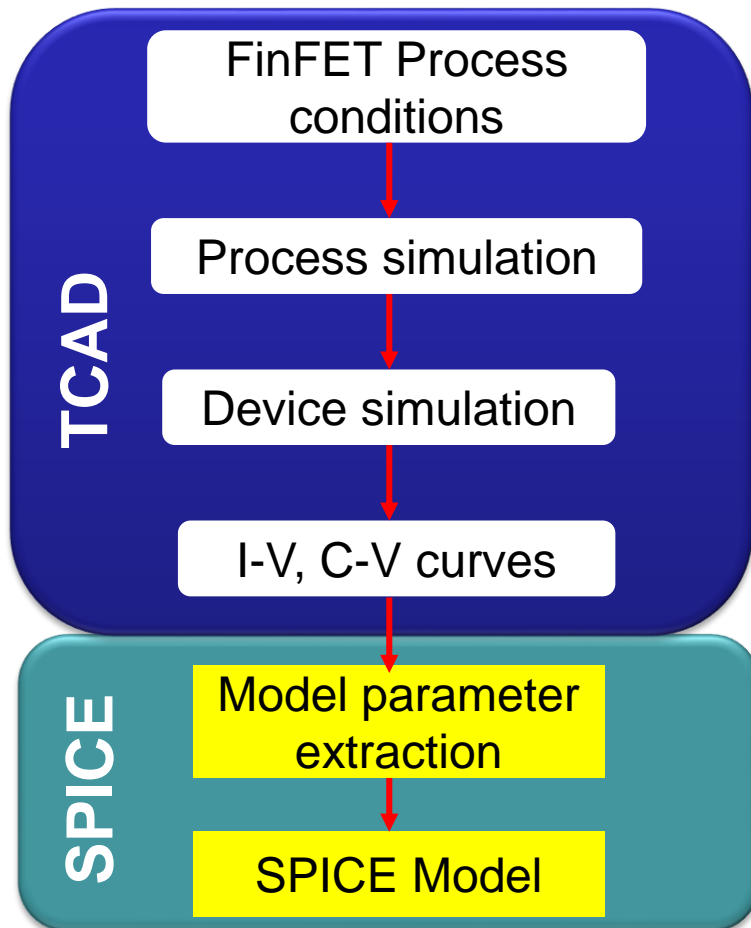
Ref: S-Y. Wu, et.al, IEDM (2013)

- **PMOS performance is well match with Ref (<10%).**
- **NMOS is slightly boosted than Ref (~15%).**

Type	Our Work (Ion)	Ref. (Ion)
PMOS	1031uA @ Ioff=46nA	960uA @ Ioff=50nA
	548uA @ Ioff=36pA	525uA @ Ioff=30pA
NMOS	1111uA @ Ioff=50nA	925uA @ Ioff=50nA
	595uA @ Ioff=30pA	520uA @ Ioff=30pA

➤ Base model extraction based on TCAD data

- Including C-V and I-V data
- Varying L_g and N_{fin}



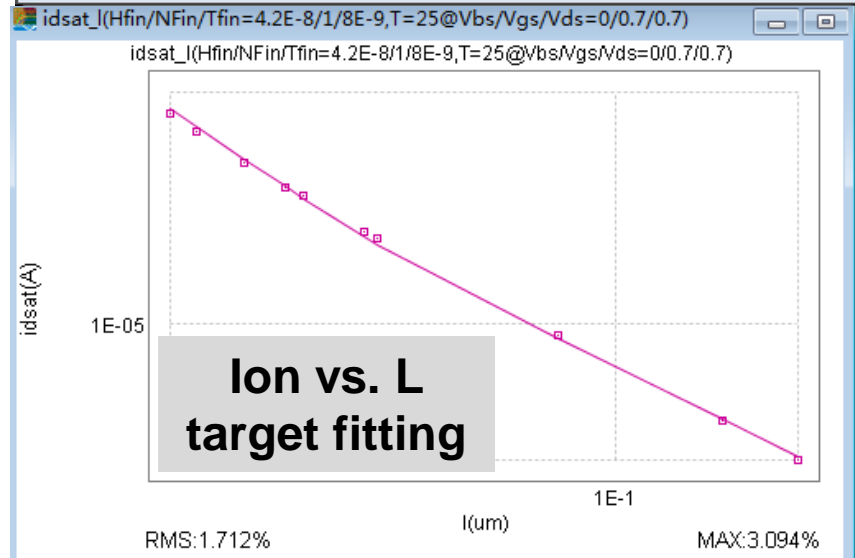
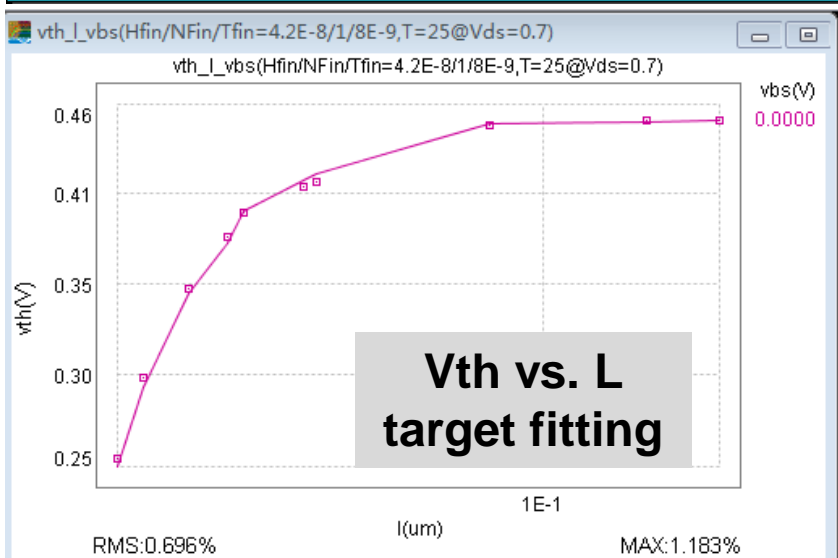
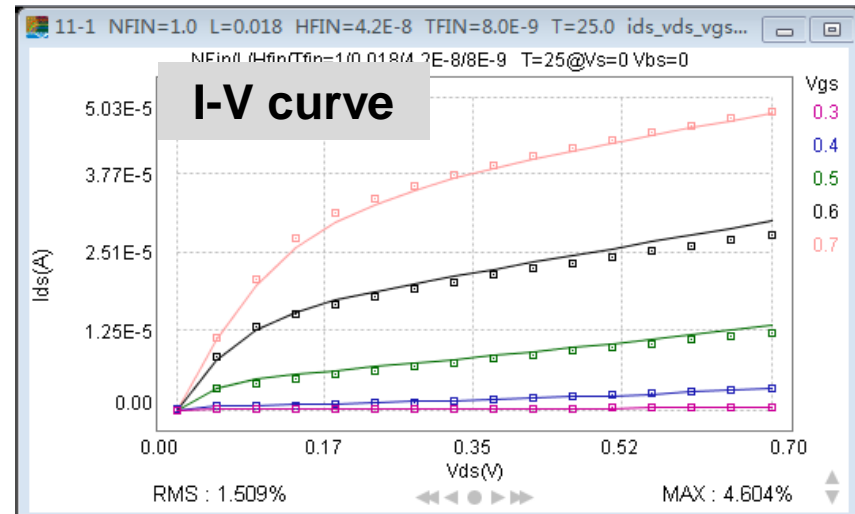
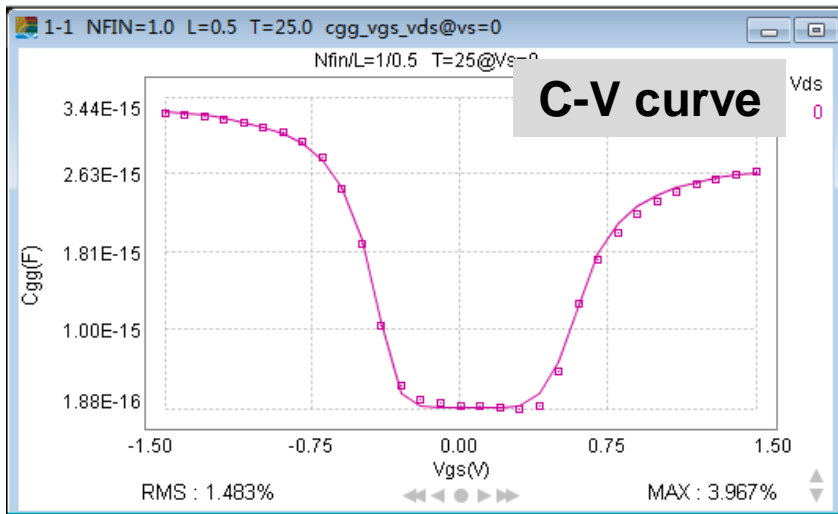
14nm FinFET device list

$L_g(\mu\text{m})$	$H_{fin}(\mu\text{m})$	$W_{fin}(\mu\text{m})$	N_{fin}
0.018	0.042	0.008	1,2,5,10 and 40
0.02	0.042	0.008	1,2,5,10 and 40
0.024	0.042	0.008	1,2,5,10 and 40
0.028	0.042	0.008	1,2,5,10 and 40
0.03	0.042	0.008	1,2,5,10 and 40
0.038	0.042	0.008	1,2,5,10 and 40
0.04	0.042	0.008	1,2,5,10 and 40
0.08	0.042	0.008	1,2,5,10 and 40
0.15	0.042	0.008	1,2,5,10 and 40
0.2	0.042	0.008	1,2,5,10 and 40

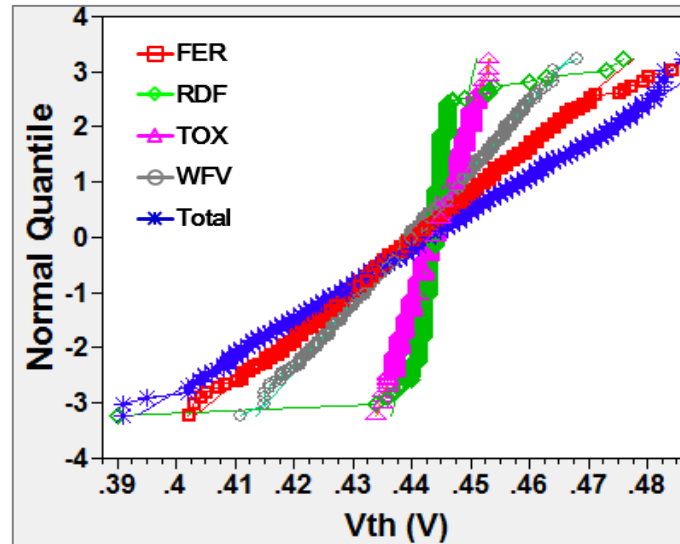
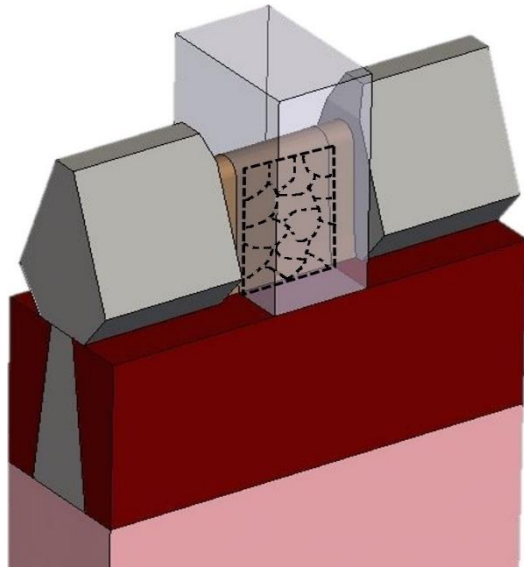
14nm FinFET Base Model Extraction

➤ Base model extraction based on BSIMCMG

- Both sweep curve and target trend are well fitted



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Gauss distributions
as-expected

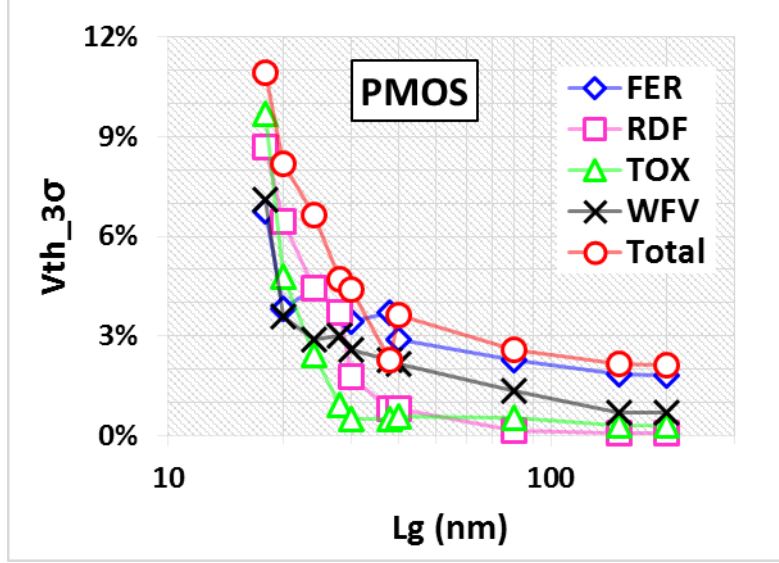
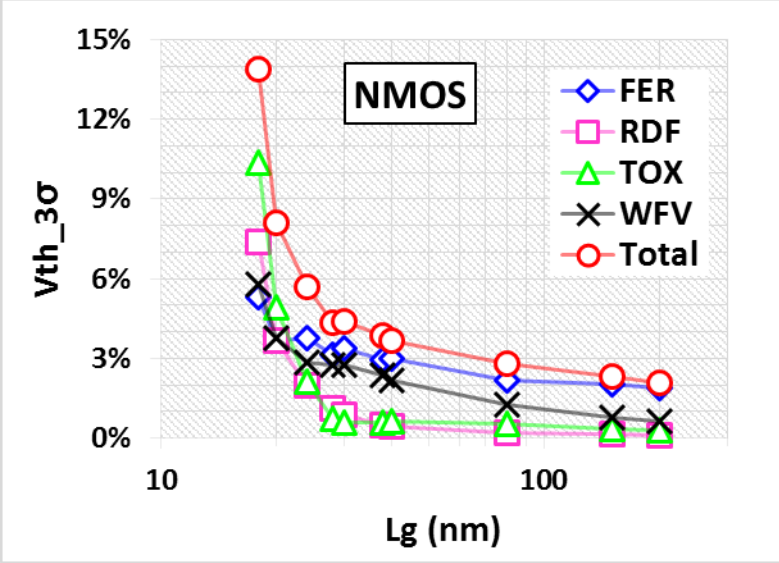
- **FER:** Fin Edge Roughness (Roughness=2.1nm @ Fin width=8nm)
- **RDF:** random doping fluctuation (~18.4 dopants in Fin @ $L_g=20\text{nm}$)
- **TOX:** gate dielectric roughness (HK-MG interface, AverageGrainSize=15nm)
- **WFV:** gate work function variation (AverageGrainSize =5nm with probability 50%(4.3), 30%(4.7) and 20%(5.2) @ work function=4.6)

AverageGrainSize: small grain formed with same orientation in ALD process

14nm FinFET Vth Variation

Factor Lg(nm)	fer		rdf		tox		wfv		sum	
	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS
18	-6.77%	5.31%	-8.69%	7.37%	-9.69%	10.38%	-7.09%	5.80%	-10.89%	13.86%
20	-3.83%	3.68%	-6.44%	3.66%	-4.80%	4.92%	-3.58%	3.78%	-8.18%	8.10%
24	-4.45%	3.77%	-4.43%	1.98%	-2.45%	2.12%	-2.89%	2.87%	-6.63%	5.69%
28	-3.72%	3.15%	-3.72%	1.11%	-0.93%	0.75%	-3.02%	2.77%	-4.71%	4.34%
30	-3.44%	3.39%	-1.78%	0.88%	-0.50%	0.59%	-2.60%	2.77%	-4.40%	4.42%
38	-3.71%	2.96%	-0.82%	0.49%	-0.53%	0.57%	-2.27%	2.38%	-2.27%	3.85%
40	-2.88%	2.97%	-0.84%	0.43%	-0.60%	0.62%	-2.17%	2.18%	-3.65%	3.66%
80	-2.27%	2.16%	-0.18%	0.22%	-0.53%	0.52%	-1.36%	1.28%	-2.59%	2.83%
150	-1.87%	2.04%	-0.09%	0.14%	-0.32%	0.36%	-0.70%	0.80%	-2.18%	2.33%
200	-1.83%	1.88%	-0.09%	0.12%	-0.31%	0.32%	-0.69%	0.64%	-2.14%	2.08%

$Vt_3\sigma\%: Vt_3\sigma/Vt \times 100\%$



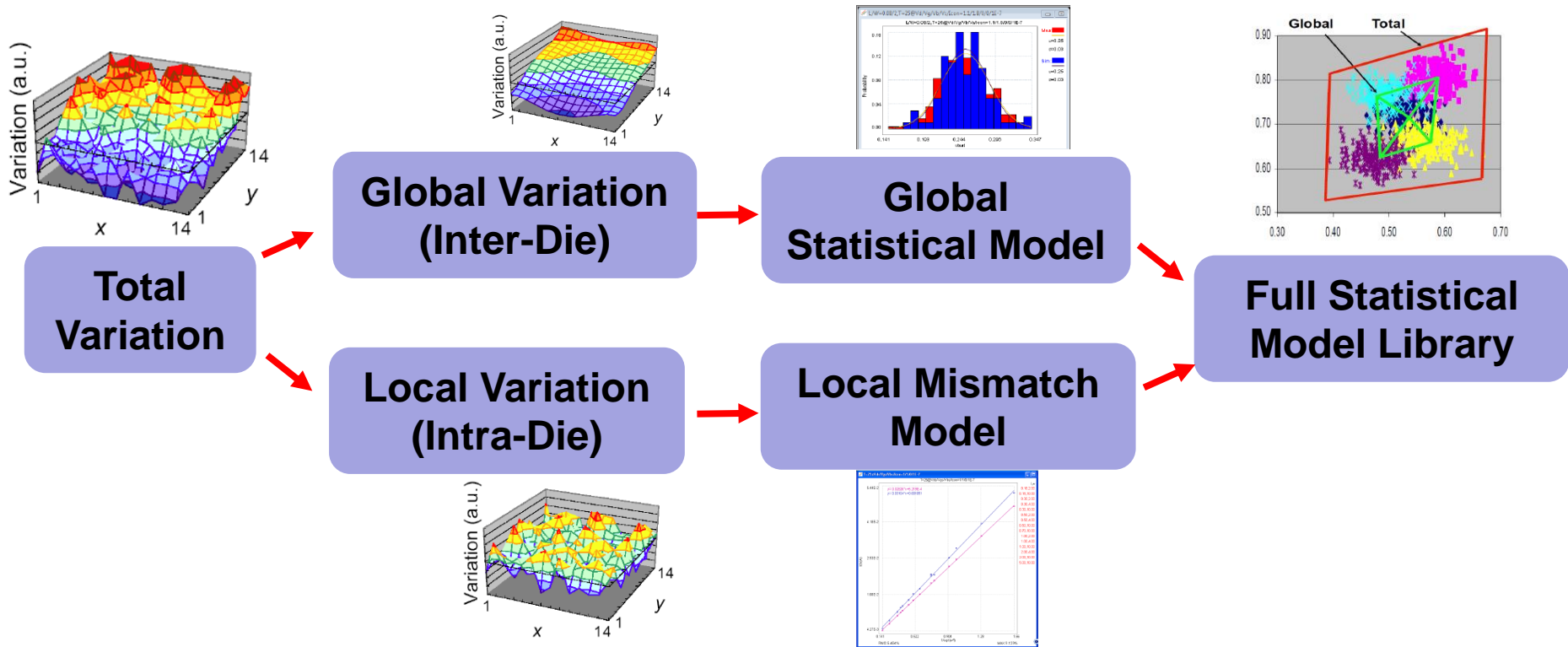
➤ **Vth variation increases with Lg scaling**

- FER/WFV dominated for larger devices, RDF/TOX increasing for smaller devices ➔ Need careful process optimization strategy

➤ Industry Standard Methodology:

- **local** mismatch model + **global** statistical model = Statistical model library
- Need to decouple total variation data into global and local components

$$\sigma_{Total}^2 = \sigma_{Global}^2 + \sigma_{Local}^2$$

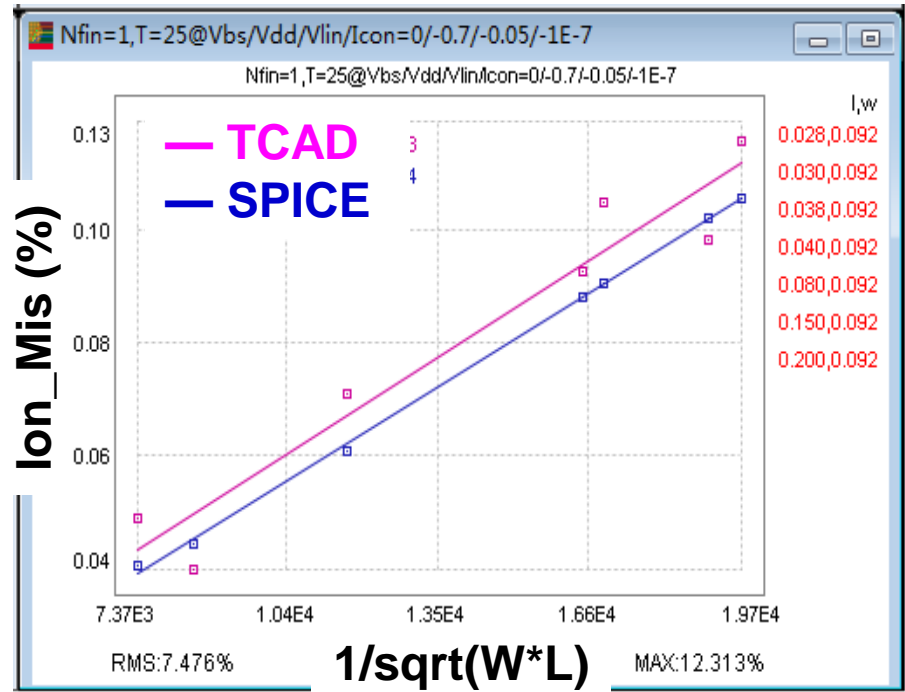
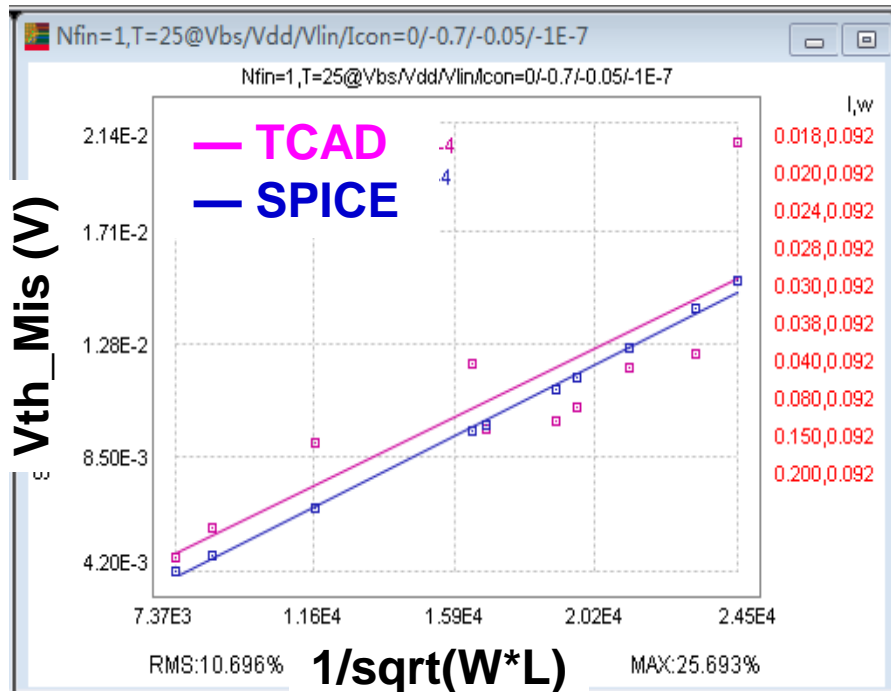


➤ Using subckt model to fit Pelgrom's plot

– Local variation data from RDF and WFV

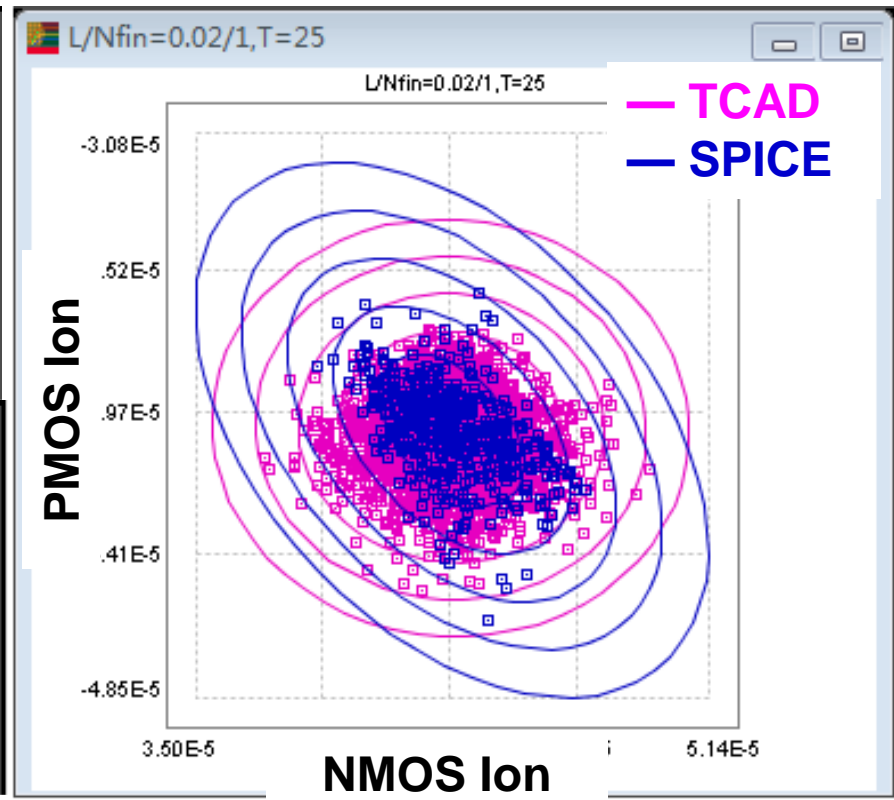
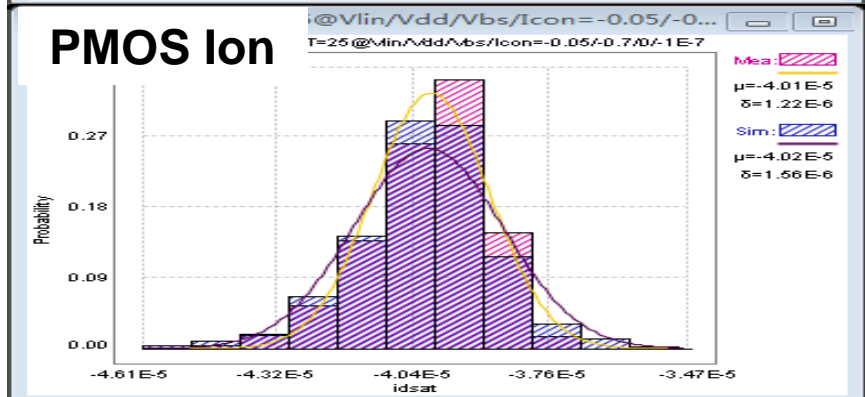
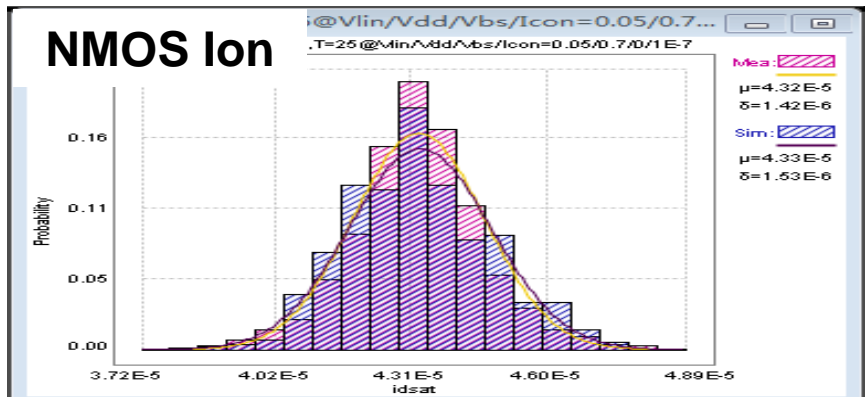
$$\sigma(\Delta V_t) = A_{V_t} / \sqrt{WL} \quad [\text{V}]$$

$$\sigma(\Delta I_d / I_d) = A_{I_d} / \sqrt{WL} \quad [\%]$$

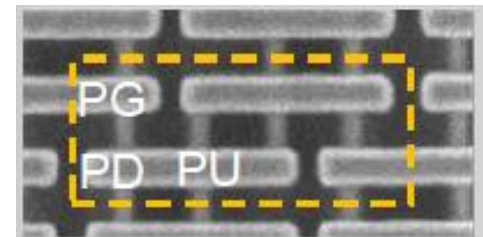
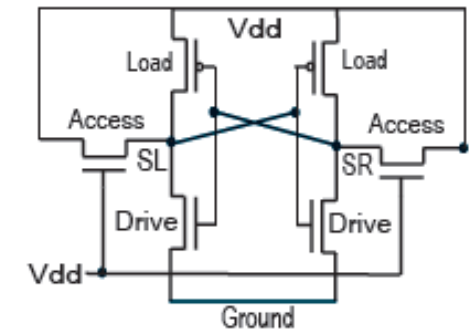
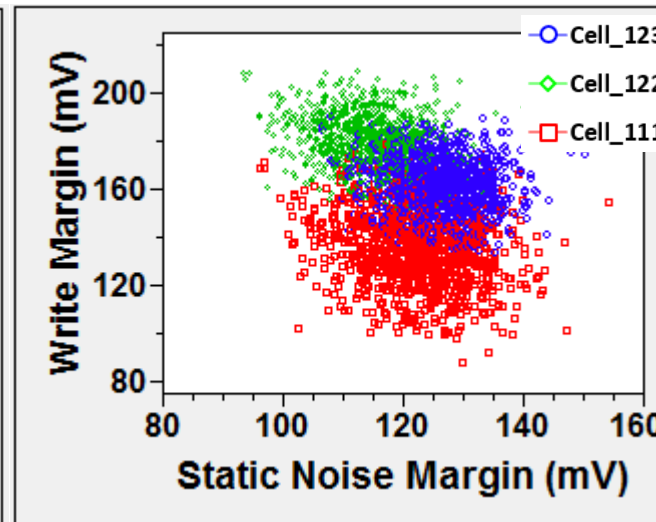
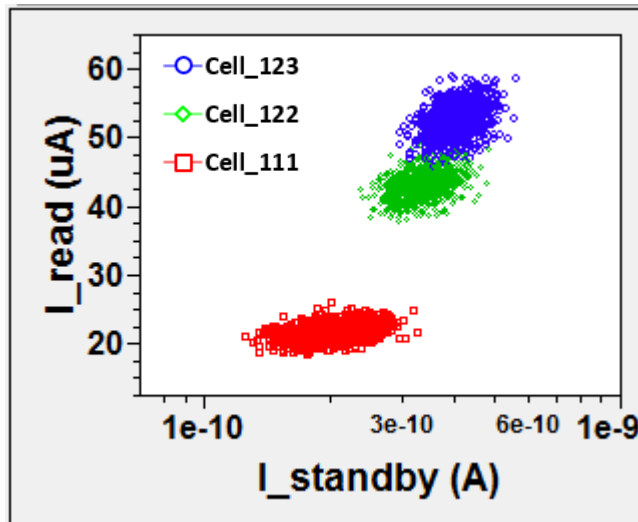


➤ Using subckt model to fit Vth/Ion distributions and also N/P correlations

– Global variation data from TOX and FER



- **Different 6T-SRAM cells evaluated by using of different # of PG and PD fins**
 - High Density Cell: 1-1-1 (PU-PG-PD)
 - Low Voltage Cell: 1-2-2 (PU-PG-PD)
 - High Speed Cell: 1-2-3 (PU-PG-PD)
- **SRAM design needs tradeoff b/w stability and cell size**

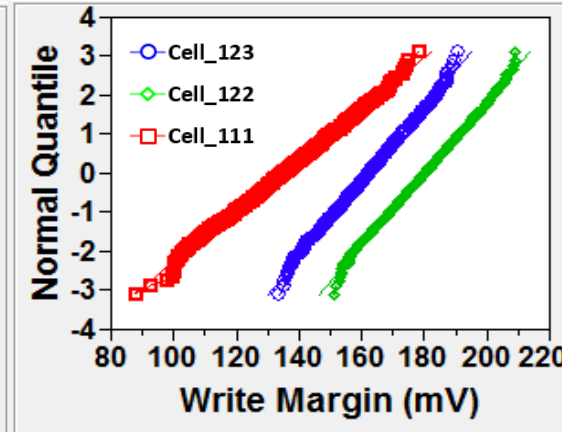
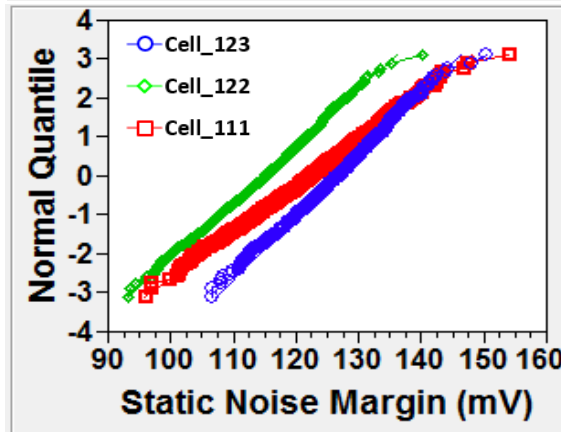
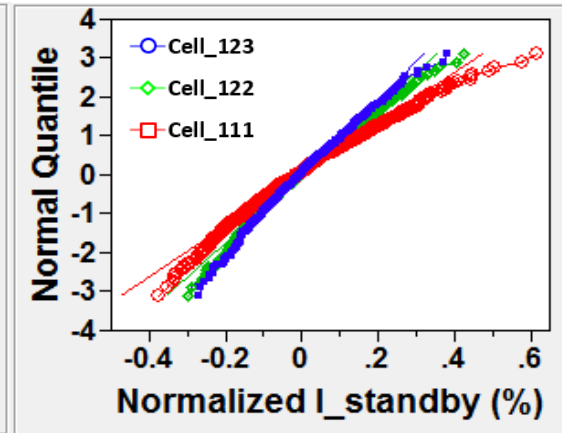
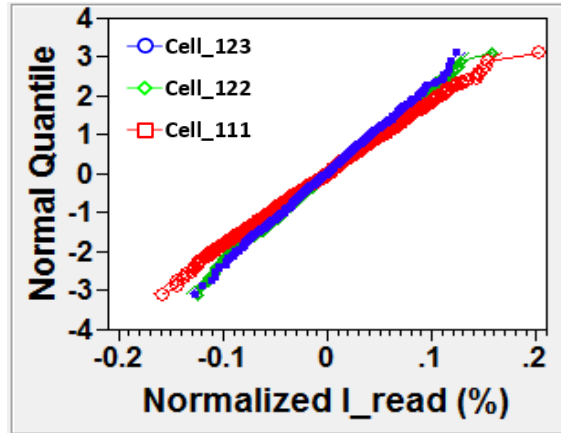


1-1-1 example

3σ variation	Cell_111	Cell_122	Cell_123
SNM (mV)	25.1	20.6	19.2
WM (mV)	45.8	32.9	31.7
I_read (%)	16.1%	13.1%	12.8%
I_standby (%)	45.7%	34.1%	31.0%

➤ **Significantly larger variations for high density cell (1-1-1)**

- More difficulties for process optimization and yield ramp



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- **Variability is a big challenge for FinFET technology.**
 - Need accurate statistical model to bridge process and design.
 - TCAD is a useful tool for FinFET variation analysis and statistical model investigations.

- **14nm FinFET TCAD platform is set up based on the leading-edge reference.**
 - Base SPICE model is extracted based on TCAD data.
 - FinFET variabilities (FER/RDF/TOX/WFV) are investigated.

- **FinFET statistical modelling methodology is demonstrated based on TCAD variation data.**
 - Statistical model library including local and global models is developed, and verified through SRAM evaluation.
 - The methodology is applicable for DTCO process and early PDK development

Thank You

Q&A