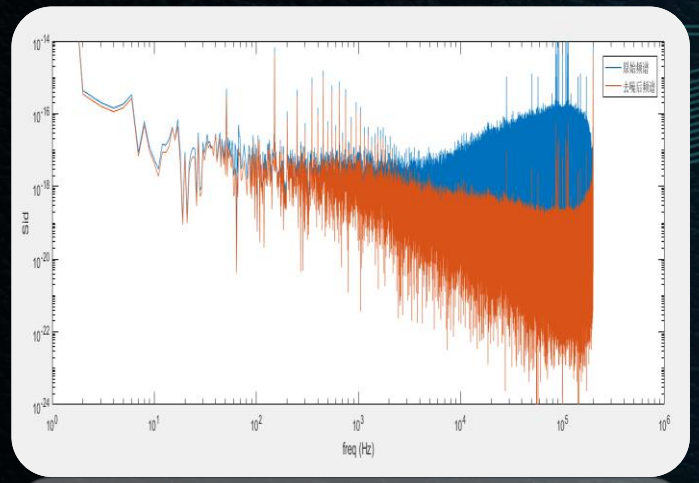
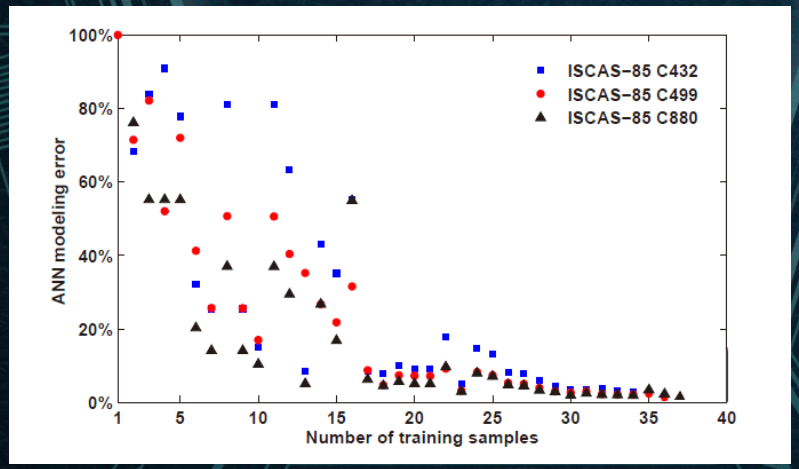
PLATFORM DESIGN AUTOMATION, INC.

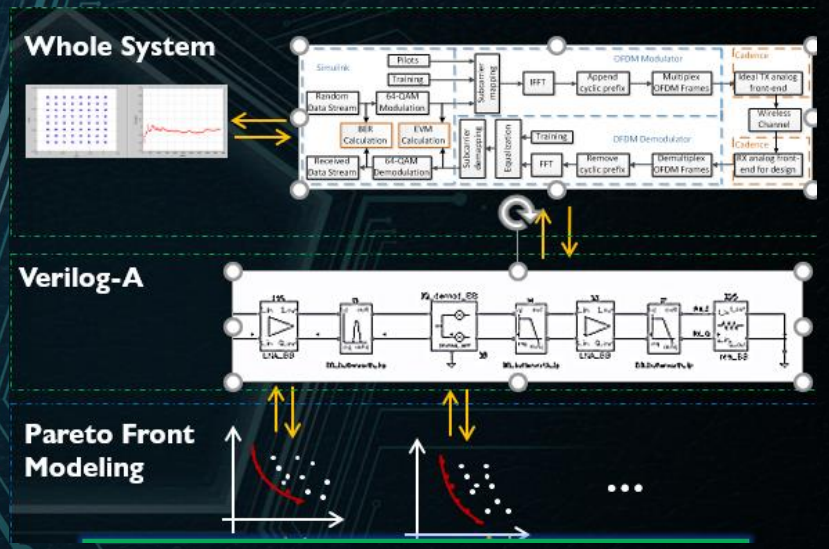
Platform Design Automation, Inc.

Pioneer in AI-Driven Test and Simulation

AI Applications in Semiconductor From Parametric Testing to Design Signoff

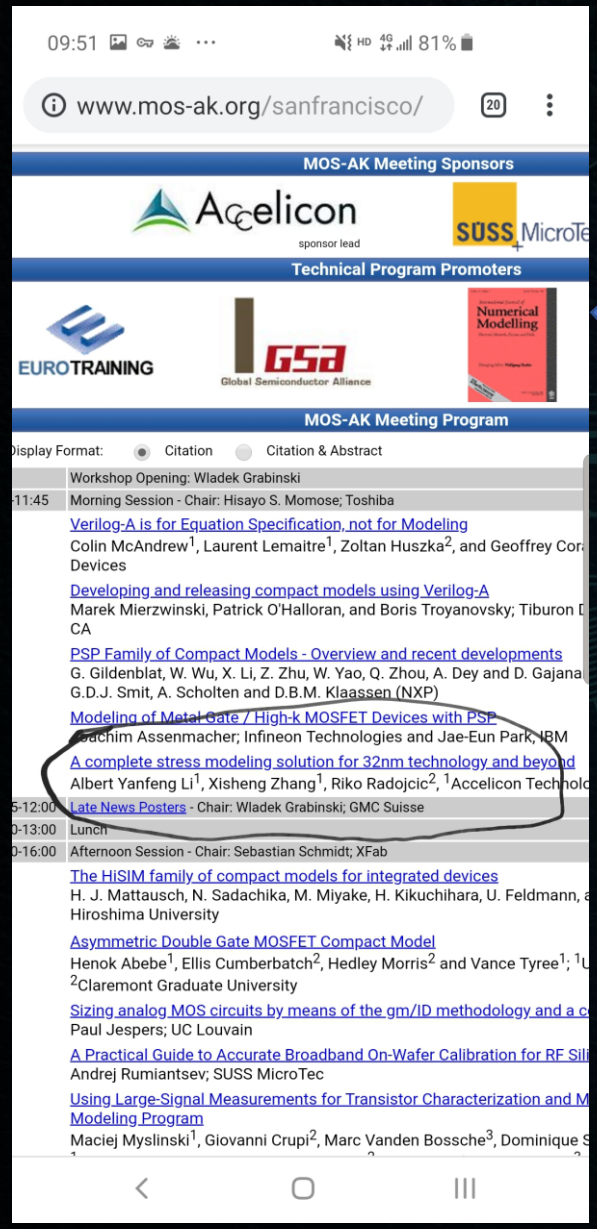






http://www.platform-da.com

11 years of support of MOS-AK



32nm

Stress Modeling (LDE)

Physics Driven

7nm/5nm

AI is hot

Algorithm Driven

博达微科技

MOS-AK Chengdu compact modeling workshop

Training course			
20 JUNE	Topic	Presenter	Presenter Company
9:00-11:45	Modeling of Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wafer circuits	Andreas Pawlak	Infineon AG
13:00-16:15	1. Radar frontends for ranging and speed measurements operating at 24GHz, 60GHz and 122GHz ISM frequency bands 2. Radar frontends for MIMO radars operating at 24GHz, 60GHz, 122GHz and 245GHz ISM frequency bands	Wojciech Debski	Silicon Radar GmbH
21 JUNE	Topic	Presenter	Presenter Company
8:30-9:20	WORKSHOP CHECK IN		
9:30-9:35	Open Speech	TBD	UESTC
9:35-9:40	MOS-AK Review & Outlook	Min Zhang	XMOD&MOS-AK
9:40-10:25	The Model and Algorithm Prototyping Platform (invited talk)	Jaijeet Roychowdhury	U.C.Berkely
10:25-10:50	Device modeling Eco-system Driven by Learning-based algorithms	Yanfeng Li	Platform-DA
10:50-11:05	Tea break		
11:05-11:50	Simulation and Modeling of Dynamic Systems with Time Varying device Characteristics (invited talk)	Masun Chan	HKUST
11:50-12:00	Group photo		
12:00-13:30	Lunch		
13:30-14:00	Advanced TFT Modeling Techniques for GOA Driver Circuit Design Optimization (invited talk)	An-Thung Cho, Lifeng Wu	HuaDa Empyrean software &Chongqing HKC
14:00-14:25	Active Device Channel spice thermal modeling and parameter extraction	Fujiang Lin	USTC
14:25-14:50	Simulation-Based Reliability Analysis for Advanced Designs and Applications	Xugang Shen	Synopsys,Inc
14:50-15:10	Tea break		
15:10-15:55	Silicon intergrated magneto-optical nonreciprocal photonic devices(invited talk)	Lei Bi	UESTC
15:55-16:20	An Analysis of DG SOI MOSFET Modeling and Simulation with PSP, BSIM-IMG and HiSIM_SOTB	GuoFang Wang, Jun Liu	HDU
16:20-16:45	TCAD-Based Statistical Modelling Methodology for Nanoscale FinFET Variability	Guo Ao	ICRD
16:45-17:10	Characterization and Modeling of the Reverse behavior of a Vertical Power MOSFET	Lixi Yan	Stuttgart University
17:10-17:35	An Industry Standard Model Including Fast and Extended Range Core with Improved Mobility and Noise effect	Chetan Kumar Dabhi	IITK
18:00-20:00	Gala dinner		
22 JUNE	Topic	Presenter	Presenter Company
8:30-9:20	WORKSHOP CHECK IN		
9:30-10:15	Negative Capacitance FET and Nanowire/Nanosheet FET modeling(invited talk)	Yogesh Chauhan	IITK
10:15-10:40	An Simulation Platform for IGBT Module Electrothermal Analysis	Chen Shen	Cogenda
10:40-11:00	Tea break		
11:00-11:45	Artificial Neural Networks for Microwave Modeling and Design(invited talk)	Qijun Zhang	Carleton University
11:45-12:10	A transient ionizing Radiation Spice model for PDSOI MOSFET	Jianhui Bu	IME Chinese Academy
12:10-13:30	Lunch		
13:30-14:15	Quasi-physical Zone division (QPZD) model for microwave wide-band-gap semiconductor technology(invited talk)	Yuehang Xu	UESTC
14:15-14:40	RF GaN Device model survey and Model parameter Extraction flows	Raj Sodhi	Keysight
14:40-15:05	Charaterization and modeling of Memory effects for GaN HEMTs	ZhiFu Hu	HSRI
15:05-15:25	Tea break		
15:25-15:50	Key Technology to GaN-based mm-Wave Devices and MMIC's (invited talk)	Xiaohua Ma	Xidian University
15:50-16:15	A Dimension-Reduction Method for the Thermal Modeling of InGaP/GaAs HBTs	Wenrui Hu, Yongxin Guo	NUS
16:15-16:40	DC and RF Modeling of CMOS Schottky Diodes	Wenyuan Zhang, Yan Wang	Tsinghua University
16:45-17:10	RF GaN Device modeling for MMIC design	Chujun Wang	CETC 55
17:10-17:15	MOS-AK 2020	MOS-AK 2020	MOS-AK 2020

PLATFORM DESIGN AUTOMATION, INC.

AI vs. DA

CNN, RNN, GAN
DNN….
Many Machine Learning terms…
…….

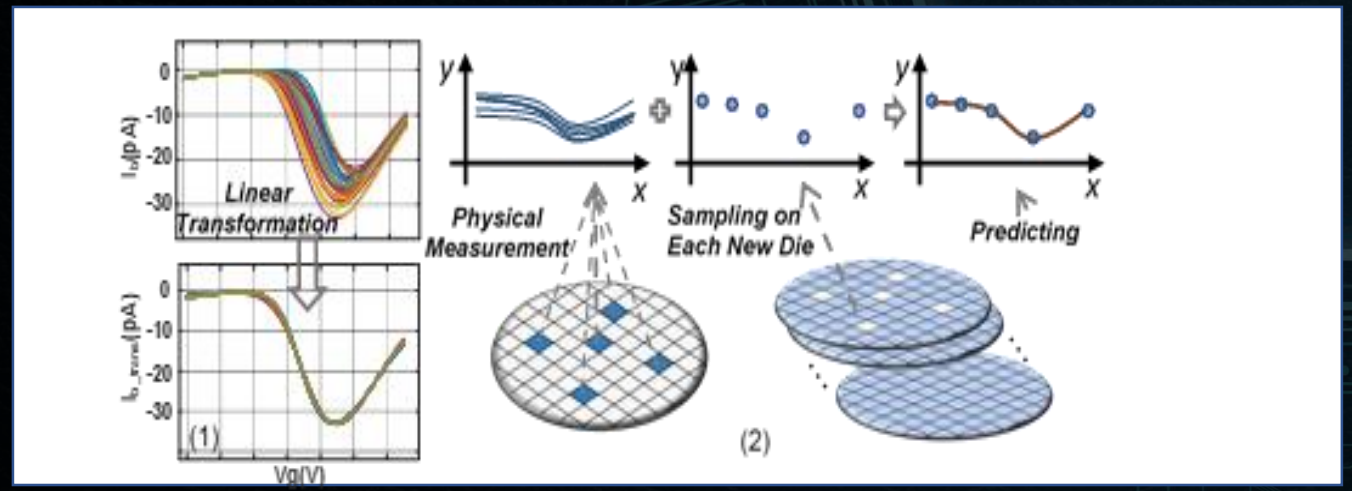
Recent hot AI terms

FFT
PCA
OLS
Spline
Bayesian….
Genetic Algorithms
Machine Learning
NN….

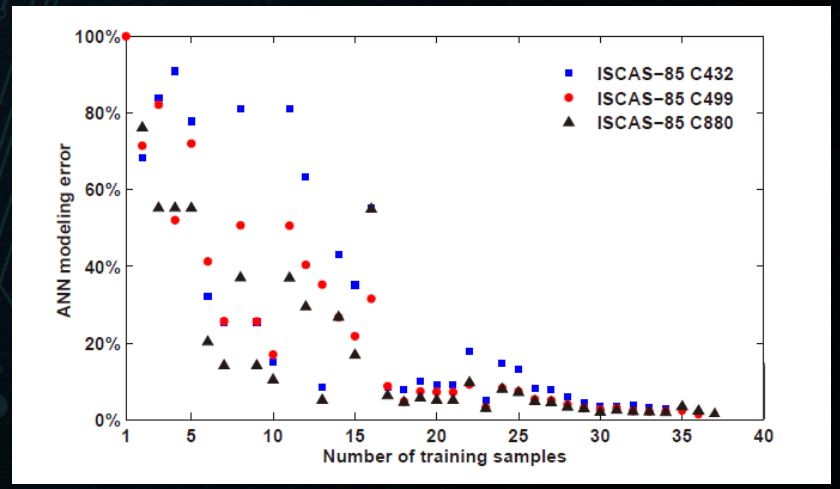
What used often in EDA

- Signal and Systems
- Stochastic process
- Numerical Analysis

DATE 2018 Best Paper on Speeding up Test with Learning Algorithms



TNS2012 paper on Soft Error Using ANN

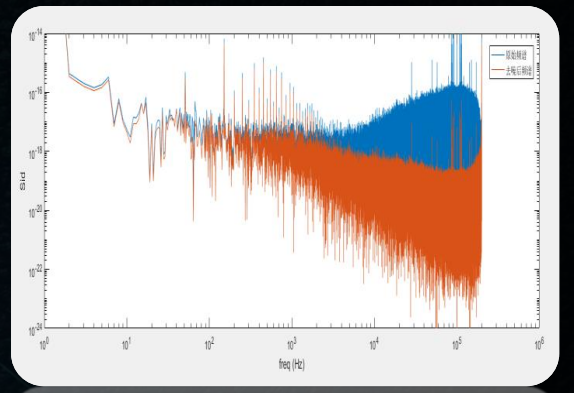


AI and DA are related

What's AI Application and Why do we need it?

- **Prediction** through different modeling approaches（RSM，NN，etc.)，and discover the "real world"
  - Use less efforts to achieve similar accuracy and performance
  - Break Hardware boundries
- **Regression**：effectively construct the network between parameters and targets and reduce the labor of tweaking parameters to achieve targets
- **Ultimate Goal**: Better Pay, **Less Working Hours**

Separate Different Noise



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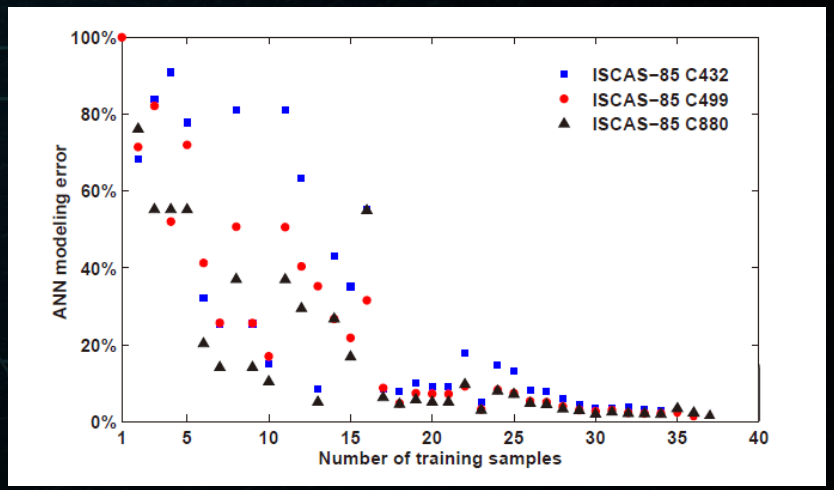

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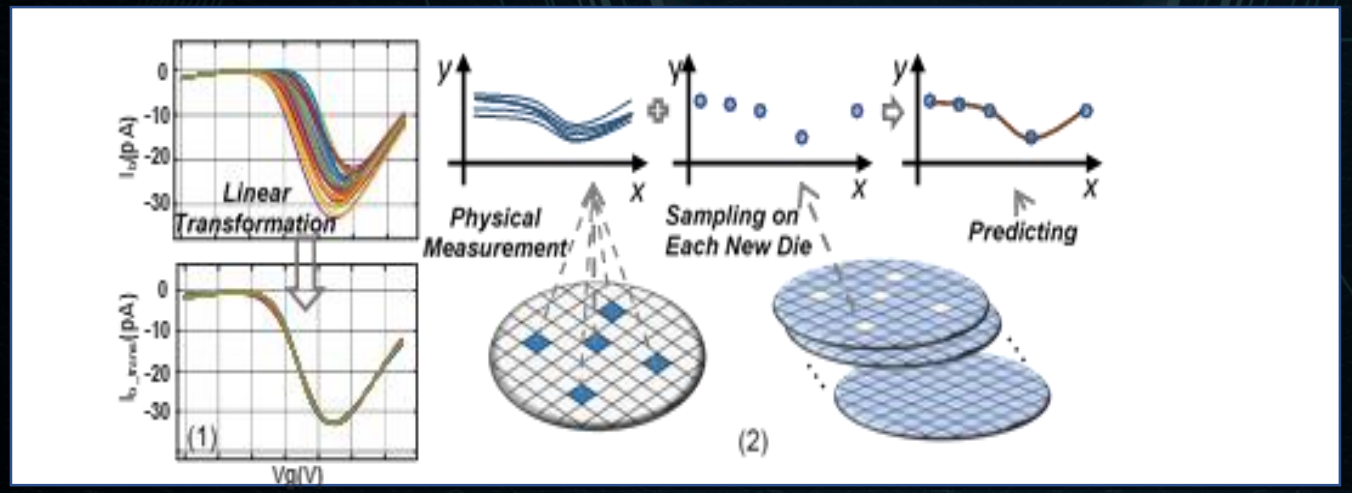

Agenda

- **AI Application : Consumer vs. Semiconductor**
  - Problem Scope, Algorithm, Expertise， Data
  - Key FOM

Concept & Key FOM

- **AI Driven Modeling Eco-system**
  - Test – Faster and More Powerful Test
  - Modeling – Automatic Extraction
  - Design – tough mission requires long term efforts

Daily Exercise in Semiconductor

- **Challenges down the road**
  - Challenges
  - Applications
- **Conclusion**

Faster, Safer and More Powerful

Scope Matters

Self-driving Cars

Self-driving Trains

HPC – Generic SW

HPC – ASIC Anton2

- **Narrow Scope**
- **Optimize Based on knowhow**

Narrowed scope, Less contamination, Higher accuracy requirement

A lot work repeatably done daily in Semiconductor have contained Scope

Rely on Expertise

- **Siri gives definitive answers**
  - Poor accuracy leads to **low usage**
- **Search Engine gives multiple answers**
  - Reply on expertise to filter, we use it **everyday**

If targets are difficult to define, give multiple answers

Data Availability

- In engineering world, most of us are dealing with low data problems
  - physics provides a shortcut
  - High quality data availability
- Low Data not necessarily a bad thing as long as it gives you enough information to extract features
  - PCA – more data doesn't give you more value
- Consumer applications requires big data, which are own by the tech giants

Most semiconductor companies owe quality data

Revisit Key FOM - DARK

Algorithms → We are optimization experts, daily exercises with different neural networks

Knowledge → Modeling background give us the best knowledge in device/IC behaviors

Data → Accumulated millions of curves from different foundry/process

Risk → We expect error in simulation or measurement

AI Has Potentials in Semi

Agenda

- AI Application : Consumer vs. Semiconductor
  - Problem Scope, Algorithm, Expertise， Data
  - Key FOM

Concept & Key FOM

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  - Test – Faster and More Powerful Test
  - Modeling – Automatic Extraction
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Daily Exercise in Semiconductor

- Challenges down the road
  - Challenges
  - Applications
- Conclusion

Faster, Safer and More Powerful

Why Device/IC Test Is a Good Machine Learning Application?

Time is $$$: Increasing Pain

Volumes: Increasing wafer volumes, increasing variability, but reducing test time = Faster **TTM**

Emerging Technologies: Micro-LED, VCSEL, Optical Module reducing testing time = saving $

IC/Device Test: Confined Scope

- Self-driving cars are difficult with current algorithms/computing, but trains are easy
- IC/Device behaviors are highly regulated, often by well-know physics, similar to "trains", with very contained scopes

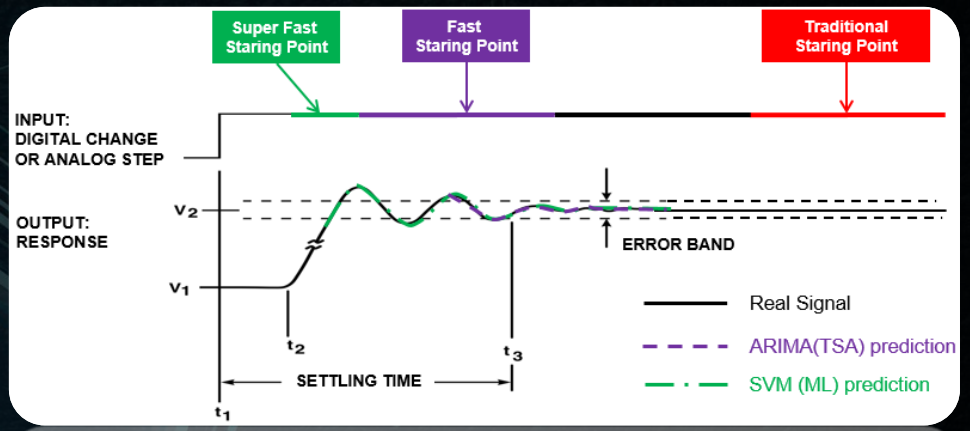
PDA's DARK

- **Data**: Owned a lot of data from many foundries
- **Algorithms**: Optimization gurus, applied machine learning in EDA for years
- **Risk**: Testing facility itself brings in error, as long as ML error <system errors, applying ML can also reduce these instabilities
- **Knowledge**: Modeling/Simulation Folks own the best behavior knowledge

Learning Based Test Methodologies

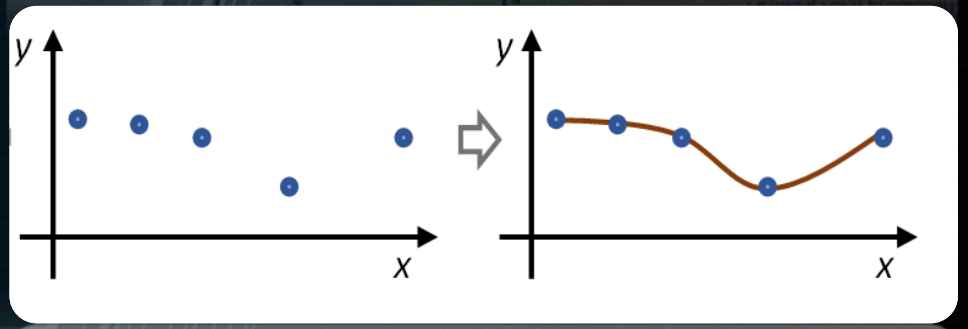
Accelerating Hardware

Testing Behavior Prediction Algorithm
Use *Time Series Analysis* to reduce settling time of the hardware



DUT - Level Test

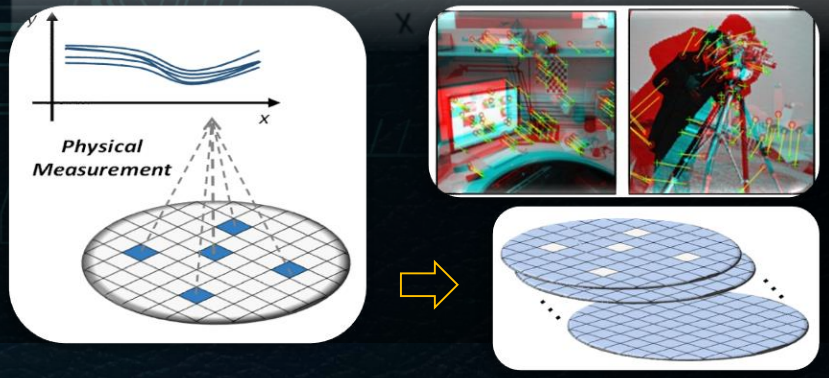
Information Redundancy Removal Algorithm with *Machine Learning*



- **Best Paper at DATE 2018**

Product-Test

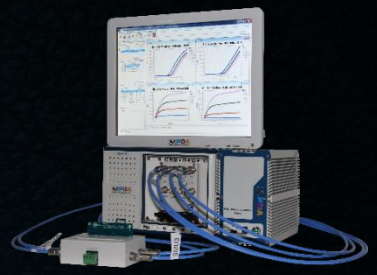
Process Variation Awareness Algorithm
Apply *Deep Learning* to extract data structure and pattern for some dies to know the behavior of other dies for smarter testing



Outcomes of Smart Test

Much Faster

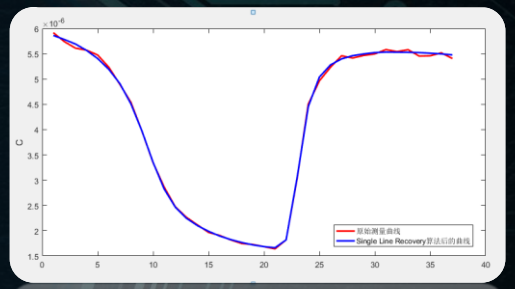
Parametric Test system can achieve **10-100X acceleration** compared to traditional IC/device while retaining same accuracy



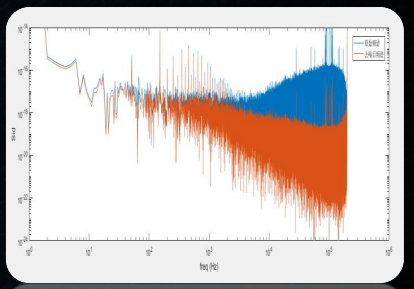
Learning Based FS Series
Parametric Analyzer In Production
The fastest on the market

Safer & Reliable

Testing noise and **testing structure drawbacks** can be internally considered and removed by learning techniques



CV Testing Noise Removal



1/f Noise Testing Repairment

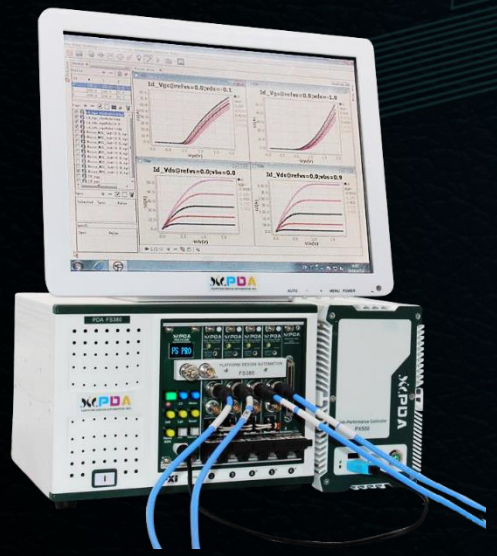
Powerful & Smarter

With 5G and MMW, current hardware based testing will soon hit a wall, "AI-driven" is the only way to break the hardware boundary.

Revolutionary in test industry: Shift from labor & capital-intensive to knowledge & technology-intensive. Align with the strategic direction of "Made in China 2025".

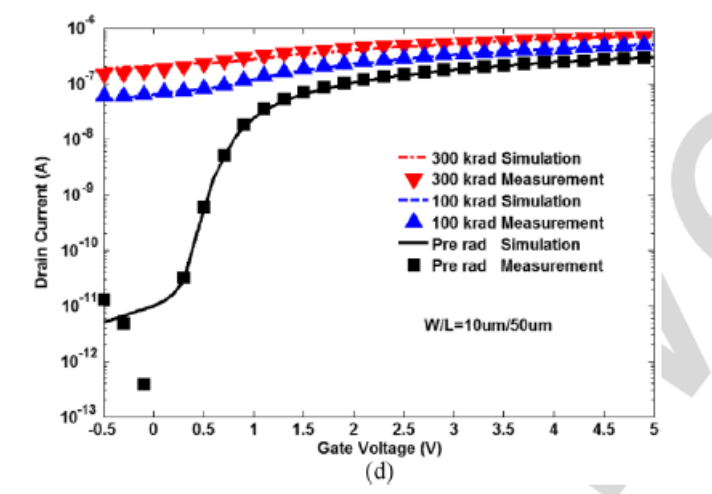
Test Methodologies

- Traditional Instruments are “Analog” heavy
- “Digital” heavy, apply similar methodologies from computer vision to extract features and recover data
  - Signal can be noisy
  - On board data processing and signal processing
- Like ASIC, test instruments are made to meet specific requirements



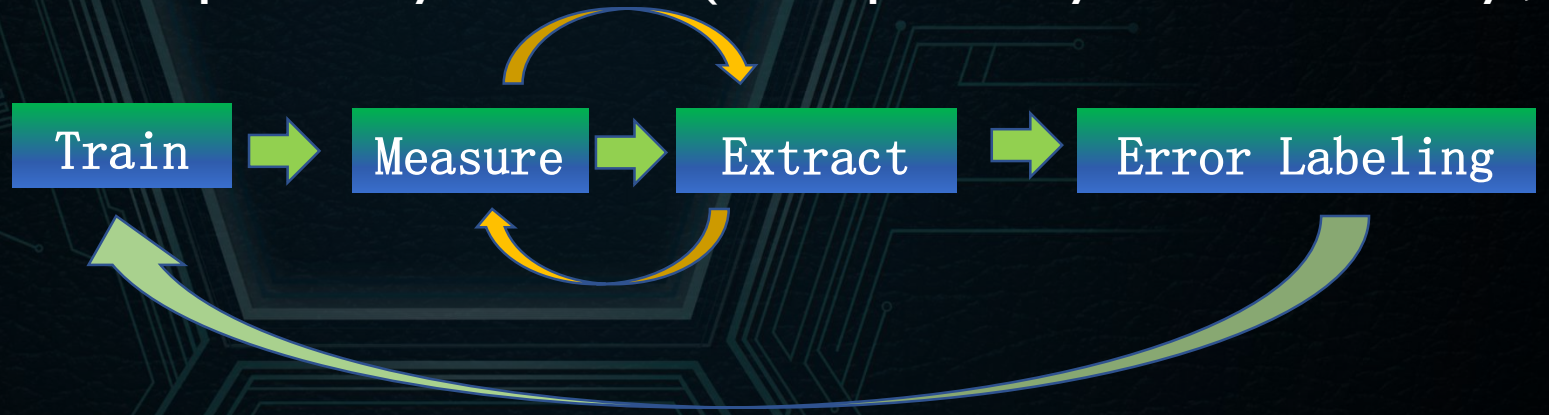
Modeling and Simulation

- Binning Is More AI Friendly (Less Parameters)
  - BSIM4 has around 200 parameters, Binning can reduce to 10-20 parameters
- TID Model Can Be Fully Automated (<10 Parameters, 1 or 2 targets)



TNS2011 TID SPICE Modeling Paper

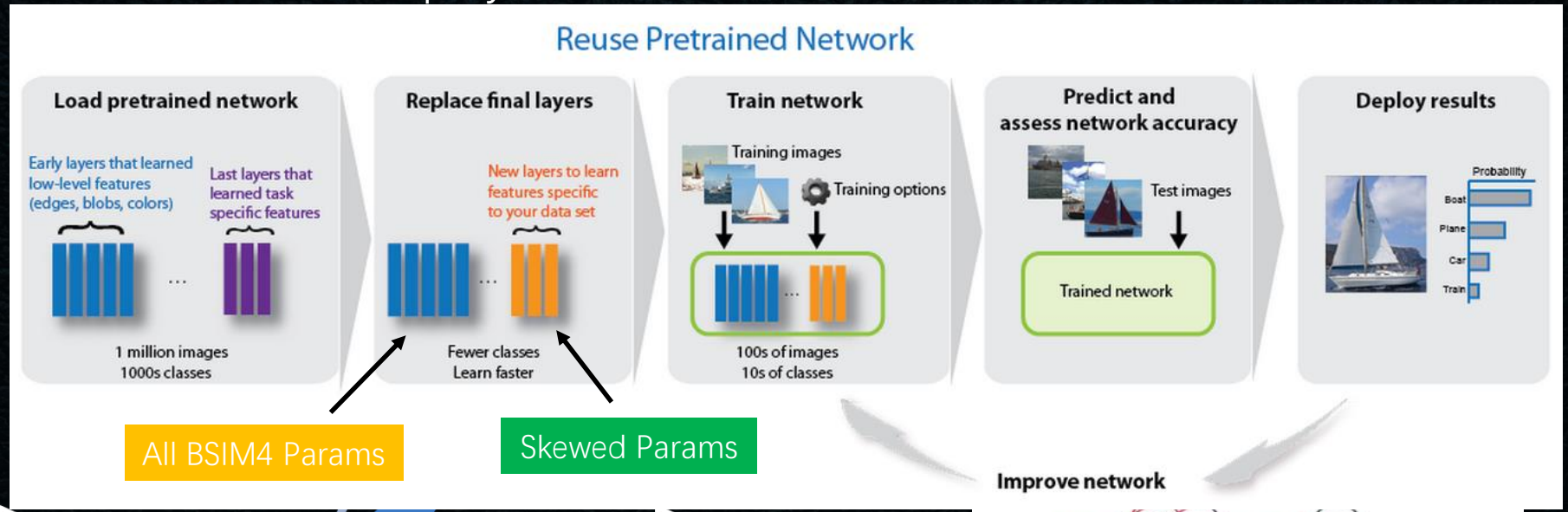
Human Experts: 3 days , Local x86(i7) +expert :1-day Pure Cloud: 10 days, ~ ¥ 30K

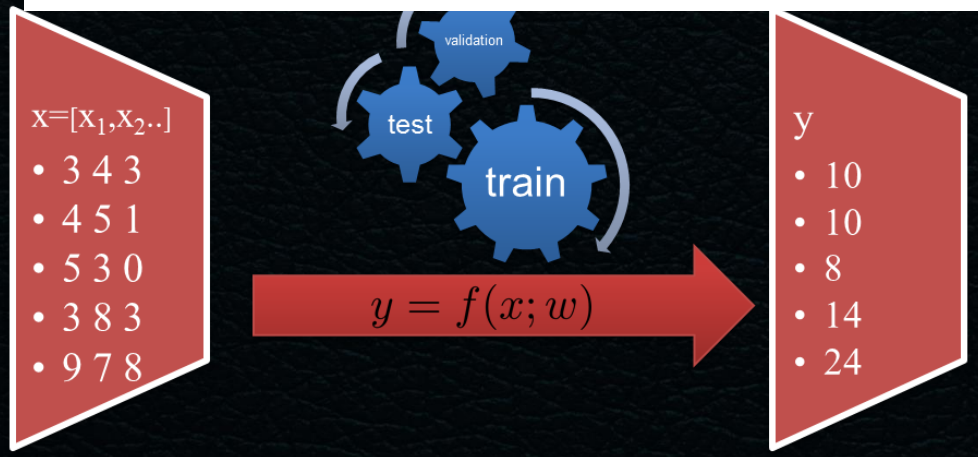


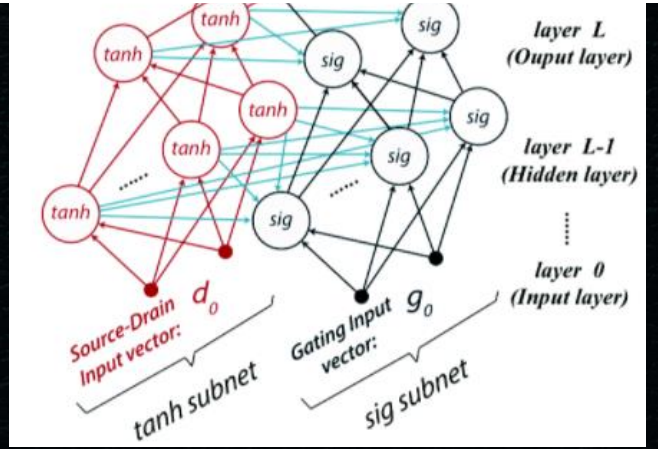
The Biggest Challenge is how to define targets

Case Study: Bi-Direction Network for Modeling

- Similar methods deployed







[1] Li, Mingda, et al. "Physics-Inspired Neural Networks (Pi-NN) for Effcient Device Compact Modeling." IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (2016).

Circuit Design

- Front end design automation: possible
- Physical layout: very difficult

Construct Correlations of System, Circuit, Device and Process

Blocks (e.g. LNA)

Circuit Specs
RO delays in consideration of LPE

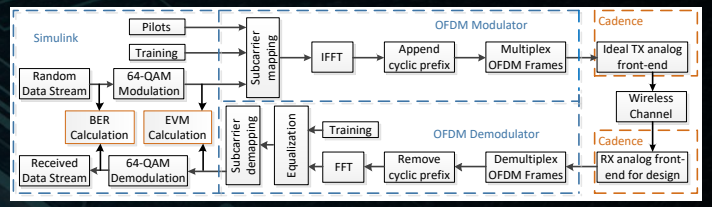
Analog Front-end

IV/CV Specs

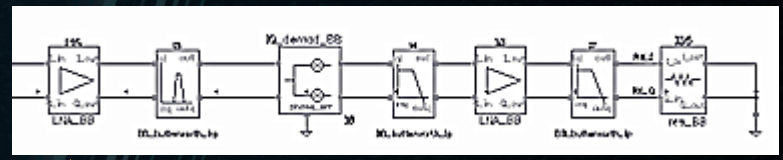
Whole System

Model/Process Params

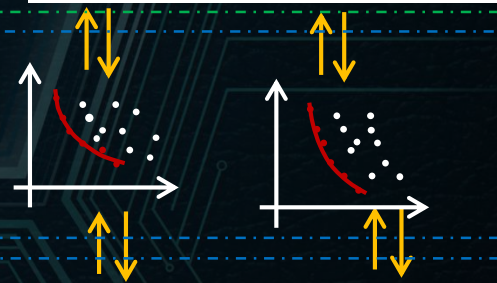
Whole System



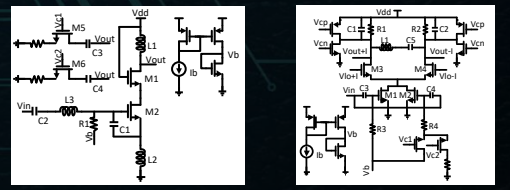
Verilog-A



Pareto Front Modeling



Circuits

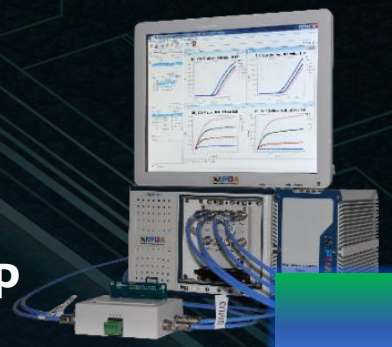


Challenges Down The Road

- **Measurement Expensive**
  - New technologies such as Micro-LED
  - 5G
- **Simulation Costly**
  - Memory and Logic ICs are already simulation costly
  - More corners

AI-Driven Parametric Test Applications I

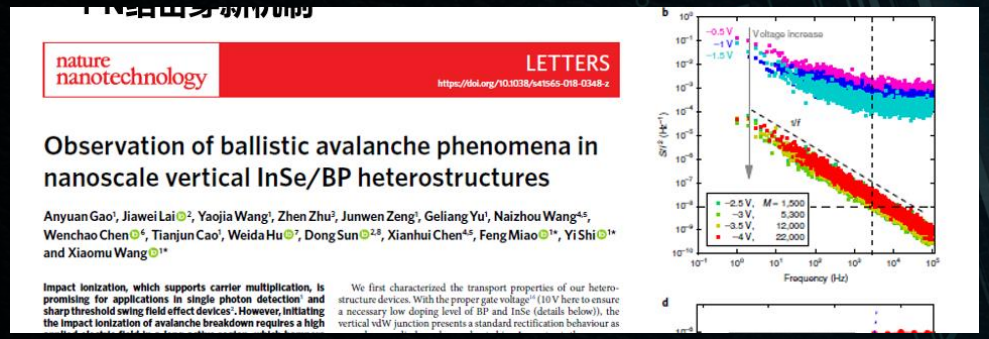
- **AI Application : IV and 1/f Noise Combined Test**
  - ☐WAT level flicker noise test is in increasing need
  - ☐Proven by leading semiconductor companies and top tier research



IV,CV,1/f Noise All-in-One
Only 8.2 Kg

Modular Architect Flexible

清華大學 Tsinghua University | 南京大學 | 中国工程物理研究院 CHINA ACADEMY OF ENGINEERING PHYSICS | FUDAN UNIVERSITY 1905 | HISILICON | winbond | nuvoTon



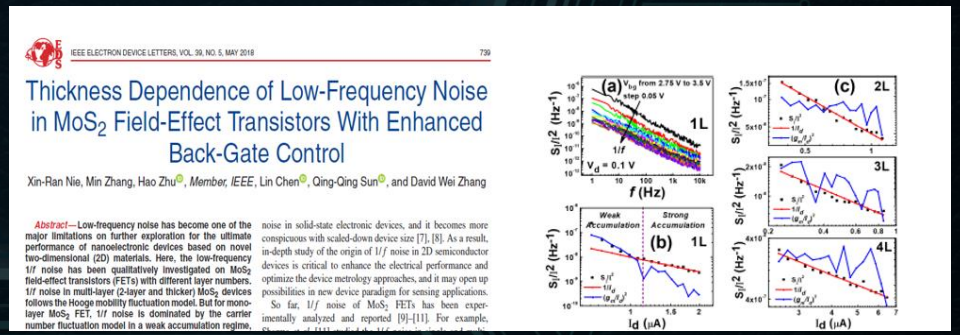
nature nanotechnology LETTERS

Observation of ballistic avalanche phenomena in nanoscale vertical InSe/BP heterostructures

Anyuan Gao, Jiawei Lai, Yaojia Wang, Zhen Zhu, Junwen Zeng, Geliang Yu, Naizhou Wang, Wenchao Chen, Tianjun Cao, Weida Hu, Dong Sun, Xianhui Chen, Feng Miao*, Yi Shi* and Xiaomu Wang*

Impact ionization, which supports carrier multiplication, is promising for applications in single photon detection and sharp threshold swing field effect devices. However, initiating the impact ionization of avalanche breakdown requires a high

We first characterized the transport properties of our heterostructure devices. With the proper gate voltage (10 V here to ensure a necessary low doping level of BP and InSe (details below)), the vertical vdW junction presents a standard rectification behaviour as



IEEE ELECTRON DEVICE LETTERS, VOL. 39, NO. 5, MAY 2018 739

Thickness Dependence of Low-Frequency Noise in MoS_2 Field-Effect Transistors With Enhanced Back-Gate Control

Xin-Ran Nie, Min Zhang, Hao Zhu, *Member, IEEE*, Lin Chen, Qing-Qing Sun, and David Wei Zhang

Abstract—Low-frequency noise has become one of the major limitations on further exploration for the ultimate performance of nanoelectronic devices based on novel two-dimensional (2D) materials. Here, the low-frequency 1/*f* noise has been qualitatively investigated on MoS_2 field-effect transistors (FETs) with different layer numbers. 1/*f* noise in multi-layer (2-layer and thicker) MoS_2 devices follows the Hooge mobility fluctuation model. But for monolayer MoS_2 FET, 1/*f* noise is dominated by the carrier number fluctuation model in a weak accumulation regime,

noise in solid-state electronic devices, and it becomes more conspicuous with scaled-down device size [7], [8]. As a result, in-depth study of the origin of 1/*f* noise in 2D semiconductor devices is critical to enhance the electrical performance and optimize the device metrology approaches, and it may open up possibilities in new device paradigm for sensing applications.

So far, 1/*f* noise of MoS_2 FETs has been experimentally analyzed and reported [9]–[11]. For example,

MXIC | HLMC | PSC 力晶半導體 Powerchip Semiconductor Corp | UMC

Nature Nano and EDL Papers

The only solution for production level 1/f Noise Test

PDA PLATFORM DESIGN AUTOMATION, INC.

AI-Driven Parametric Test Applications II: FCPro

- High speed， high density, accurate capacitance tester
  - UPH = 40,000 devices (32 channel system)

0.1pF accuracy

Modular

200V

Up to 64 channels

Conclusion

- AI in Semi is not just AI Chips, AI applications have a lot of potential.
- Design and Manufacture should invest more on Algorithms
- AI is the answer for future challenges in Test and Simulation

PDA At A Glance

- **PDA: Unique Integration of All the Critical Elements that connect Process Technology with Product Design**

EDA

Test

EDU

Scale by designs

Scale by wafers

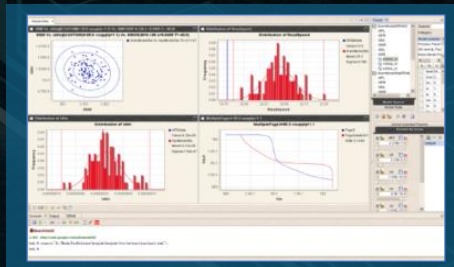
Scale by people

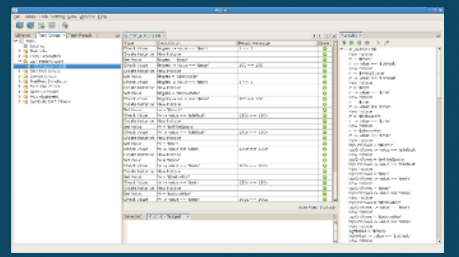
Engineering Center

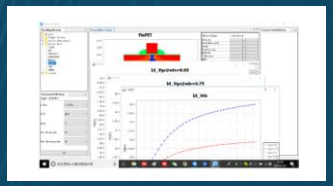
100

Embrace Data

Faster Test and Faster Simulation







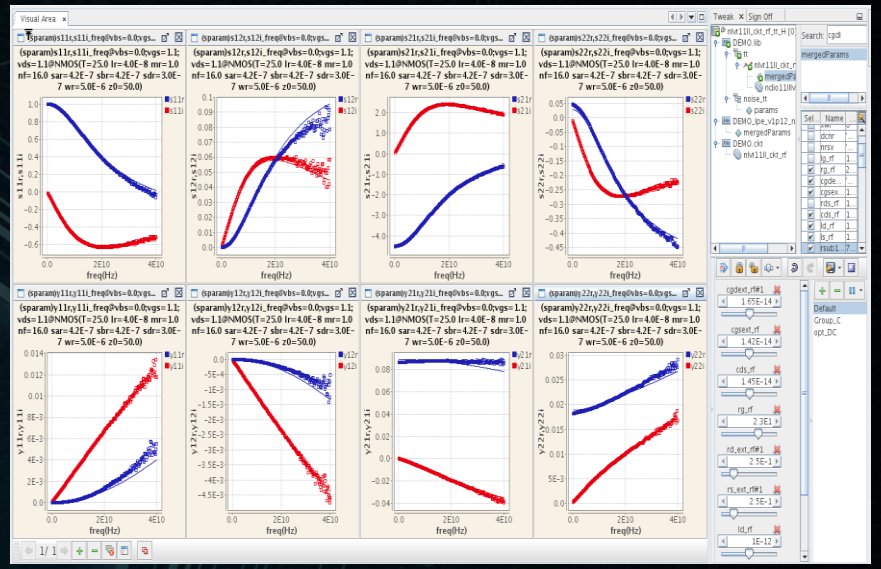
Technology Driven, Innovation is our Key Competence

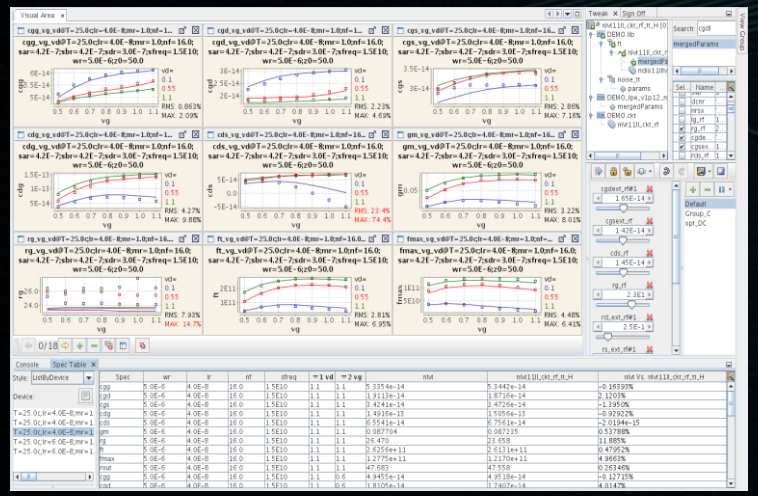
PDA
PLATFORM DESIGN AUTOMATION, INC.

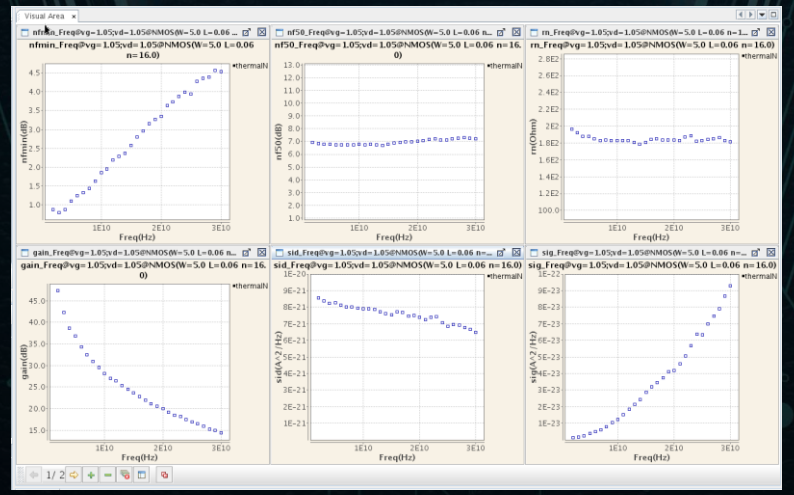
MQRF – Complete CMOS RF Modeling Platform

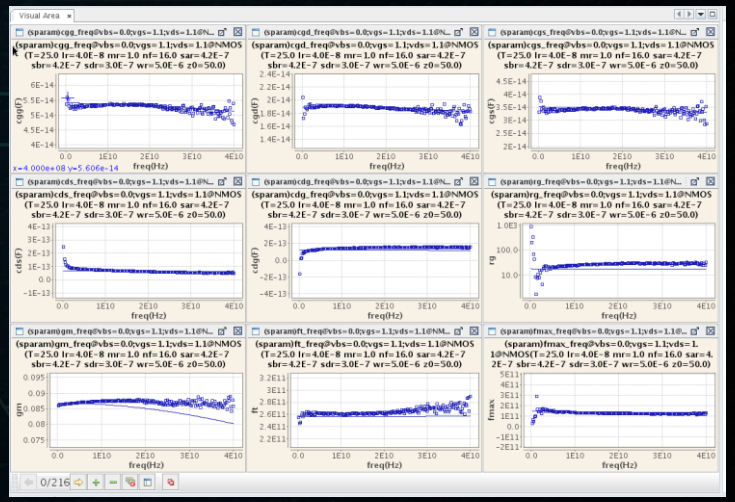
MQ-RF – Integrate BB modeling, QA and RF to a single platform

- **Unique integration of the whole RF Flow**
  - DC, AC, LDE, Statistical, 1/f noise, RF and Thermal noise
- **Comprehensive Model Support**
  - **BSIM3、BSIM4、BSIM6、BSIM-CMG、BSIMSOI、PSP**
- **RF Model Extraction Technology up to 110GHz**
  - **Internal QA**
- **Built-in RF data QA, de-embedding, extraction and model QA**









FSPro+ - Complete Semiconductor Analyzer Production Test

Modular architect

10fF CV Accuracy

0.1fA sensitivity

200V, 3A

5X Faster

Compact
8.2Kg

As many channels as desired

1/f noise integrated (all channels)

High precision IV, and 1/f noise test in one box w/o cabling change (e.g. 5X CP than competition)

1/f noise Production test ready (down to 2s/bias)

Support WAT 1/f noise test

Built-in MeQLab to form a complete modeling system