Recent Enhancements in BSIM-IMG

BSIM-IMG: Industry Standard Model with Fast and Extended Range Core Including Improved Mobility and Noise models

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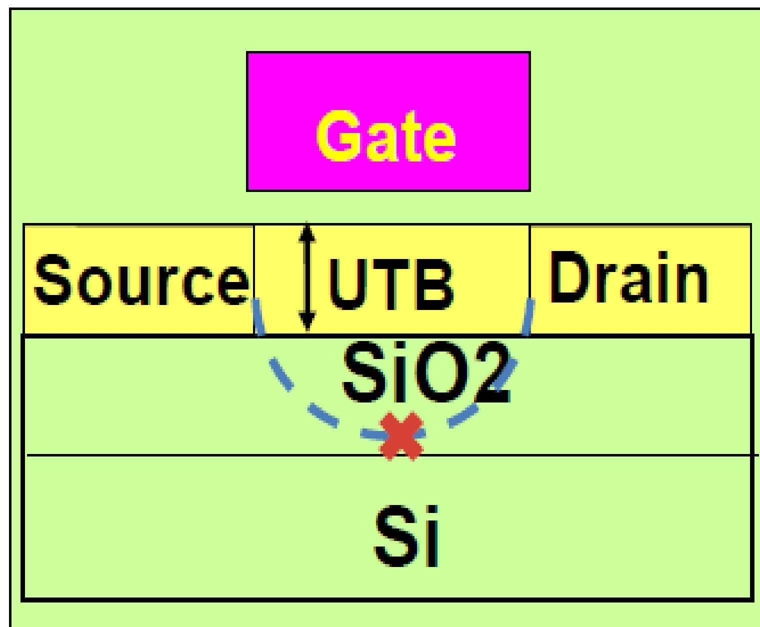
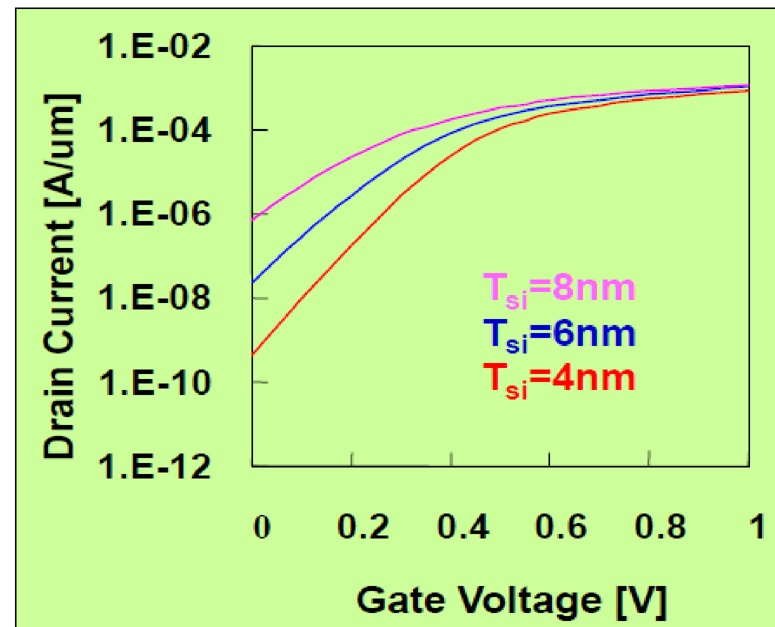
Difficult to suppress leakage in Scaled MOSFET





- Need a thinner Oxide to suppress the leakage
- Gate Leakage is the Issue !

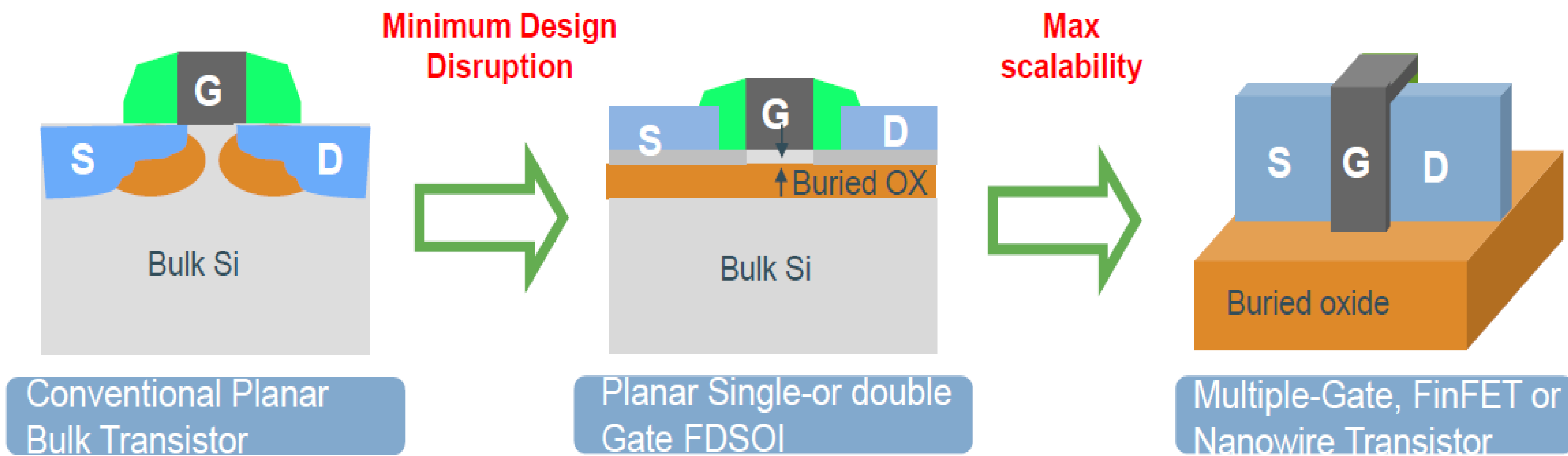
Solution:

Leakage is suppressed by multi-gates

Scale body thickness instead of Oxide thickness

Yang-Kyu Choi et.al, "*Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era*", IEEE electron device letters, vol. 21, no. 5, may 2000

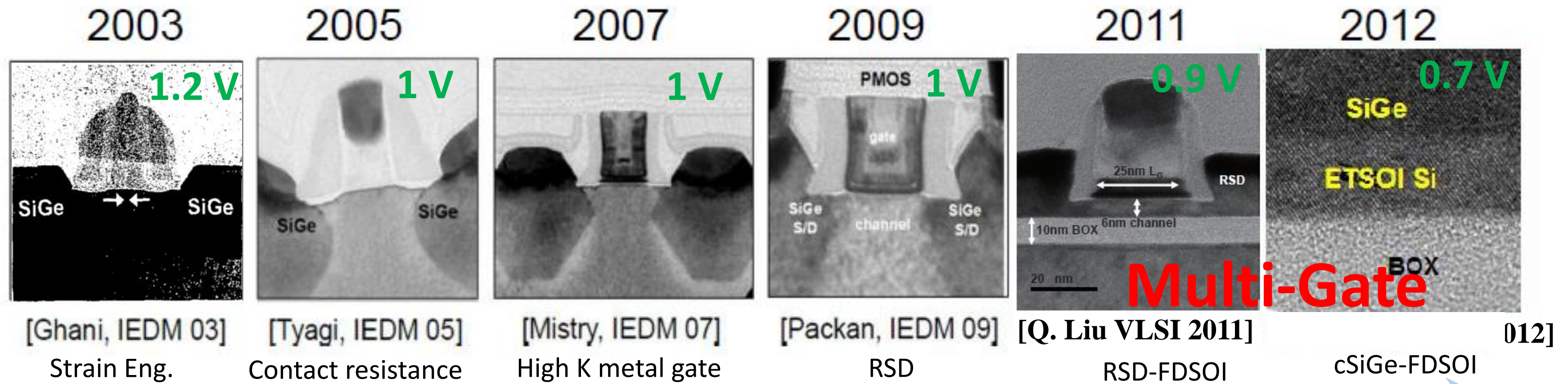
Examples of Multi-Gate



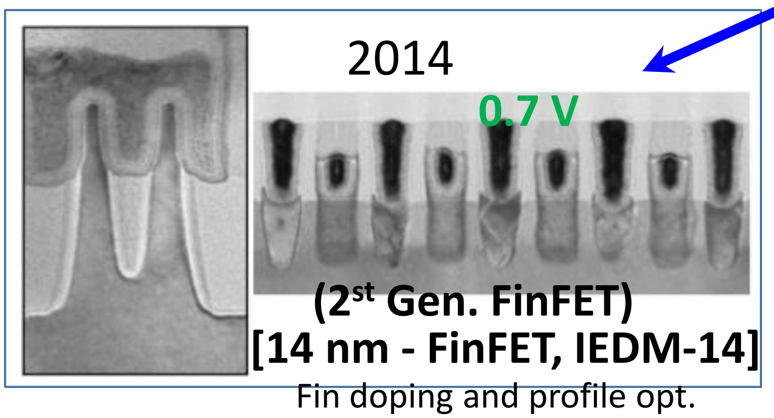
FDSOI : Fully Depleted Silicon-on Insulator

- Thin channel for (fully depleted) better gate control and Short channel effect (SCE)
- Better gate control ⇒ Better transistor scaling

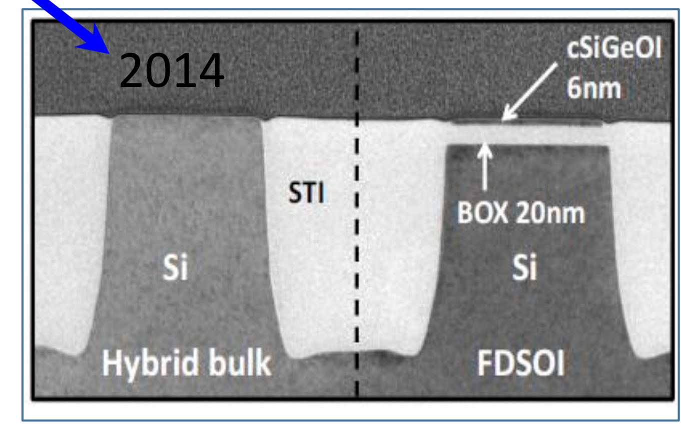
Scaling: CMOS Solution



Multi-Gate



Fin doping and profile opt.



[14 nm - FDSOI, VLSI-TSA]

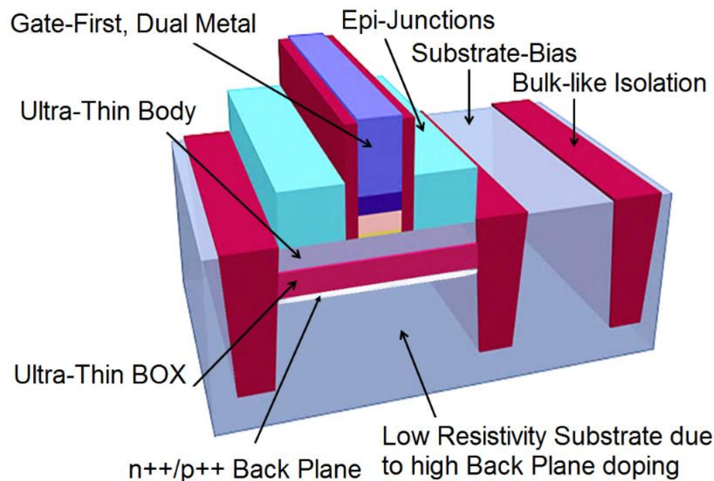
BSIM-IMG Developed for FDSOI Multi-gate MOSFET

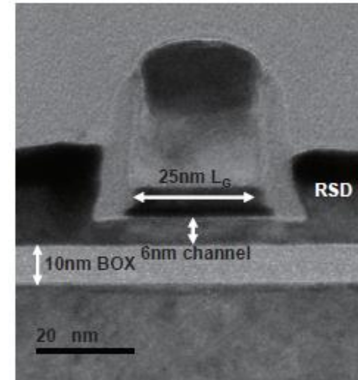
Outline

- **BSIM-IMG: Independent Multi-gate MOSFET Model**
  - **Fast core Model**
  - **Extended Range Core Model**
- **Channel current, Charge and Capacitance Model**
- **Dual Mobility Model: g_m Double Hump Behavior**
- **Developed Noise Models in BSIM-IMG**

BSIM-IMG: Independent Multi-gate MOSFET Model

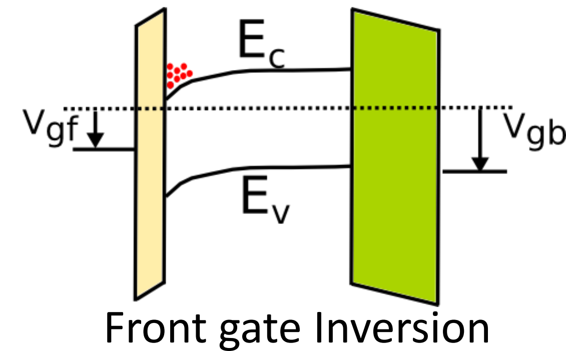
- Separate front and back gates
- Asymmetrical gate stack: T_{ox}, Work-function etc.



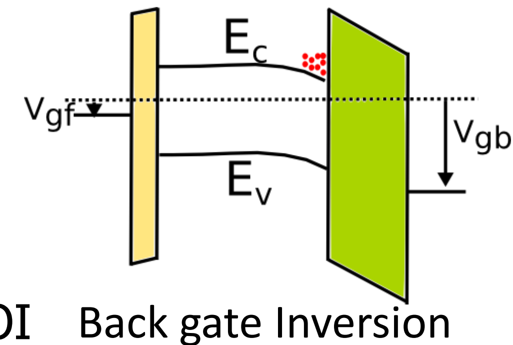


[Q. Liu VLSI 2011]

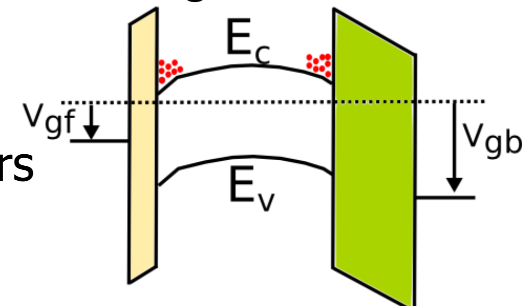
Target Device: UTBB SOI



Front gate Inversion



Back gate Inversion



Both gates are in Inversion

Physical surface-potential-based core I-V and C-V model agrees with Numerical Solution without fitting parameters for surface potential

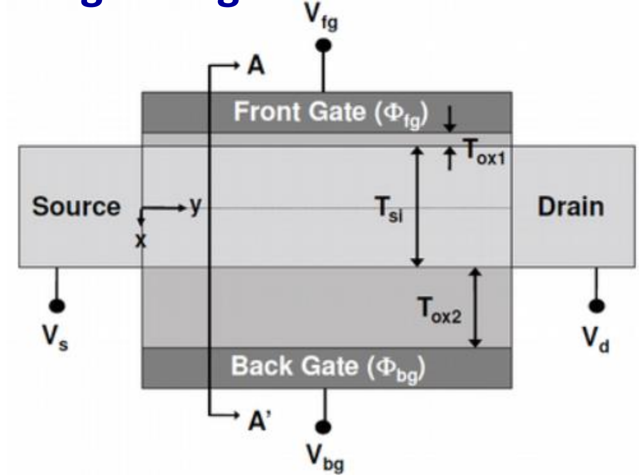
Fast Core Model

Solving Poison's eq. in silicon body

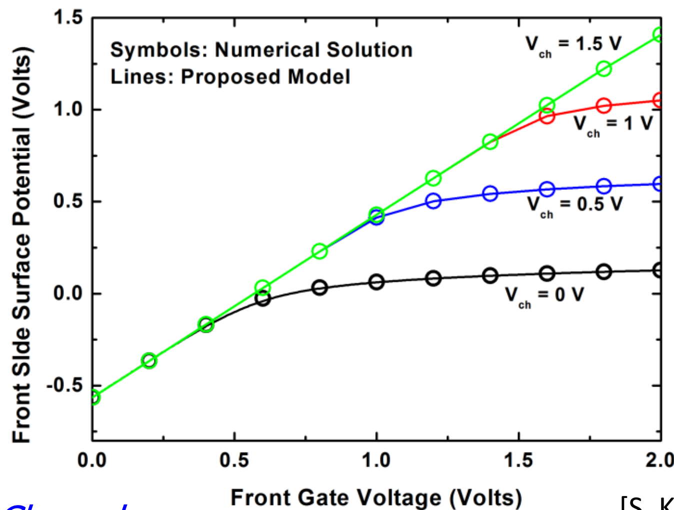
$$\left(C_{\text{ox1}}\frac{V_{\text{fg}}-\Delta\phi_1-\psi_{s1}}{\epsilon_{\text{Si}}}\right)^2-\left(C_{\text{ox2}}\frac{V_{\text{bg}}-\Delta\phi_2-\psi_{s2}}{\epsilon_{\text{Si}}}\right)^2 = \frac{2qN_cV_{\text{th}}}{\epsilon_{\text{Si}}}\left[\exp\frac{\psi_{s1}-V_{\text{ch}}}{V_{\text{th}}}-\exp\frac{\psi_{s2}-V_{\text{ch}}}{V_{\text{th}}}\right]. \quad \text{....(1)}$$

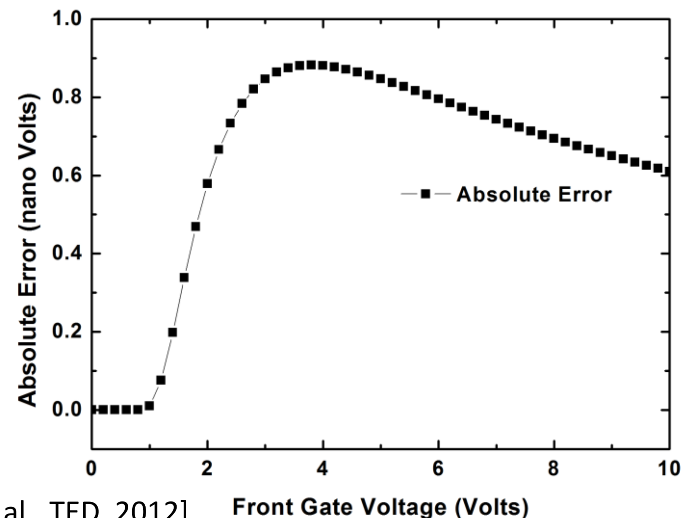
$$\psi_{s2}=\frac{C_{\text{Si}}}{C_{\text{Si}}+C_{\text{ox2}}}\psi_{s1}+\frac{C_{\text{ox2}}}{C_{\text{Si}}+C_{\text{ox2}}}(V_{\text{bg}}-\Delta\phi_2) \quad \text{....(2)}$$

Considering back gate in weak inversion



Solving (1) with proper initial guess, and using Helly's algorithm: Analytical Surface potential





[S. Khandelwal et. al., TED, 2012]

Extended Range Core Model

Solving Poison's eq. for undoped silicon body

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{\rho(\psi)}{\varepsilon_{\text{ch}}} = \frac{qn_i}{\varepsilon_{\text{ch}}} e^{\frac{\psi - V_{ch}}{v_T}} \quad ....(1)$$

Integrating Poison's for front and back gate

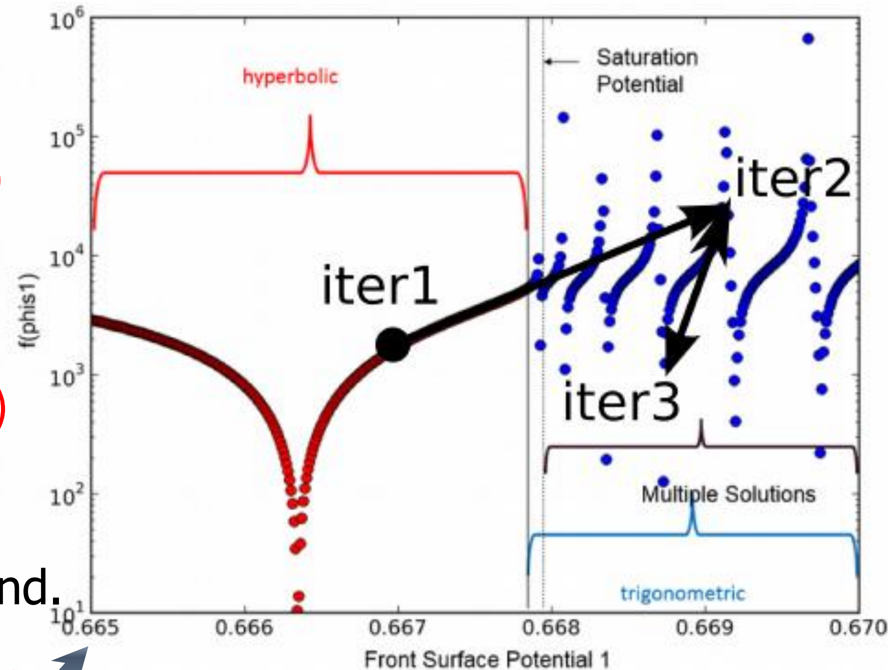
$$\left.\begin{aligned} \alpha^2 &= k_f(x_f - \varphi_f)^2 - A_0 e^{\varphi_f} \\ \alpha^2 &= k_b(x_b - \varphi_b)^2 - A_0 e^{\varphi_b} \end{aligned}\right\} ....(2)$$

Integrating electric field and using boundary cond.

$$\alpha \coth(\alpha/2)(k_f(x_f - \varphi_f) + k_b(x_b - \varphi_b)) + k_f k_b (x_b - \varphi_b)(x_f - \varphi_f) + \alpha^2 = 0 \quad ....(3)$$

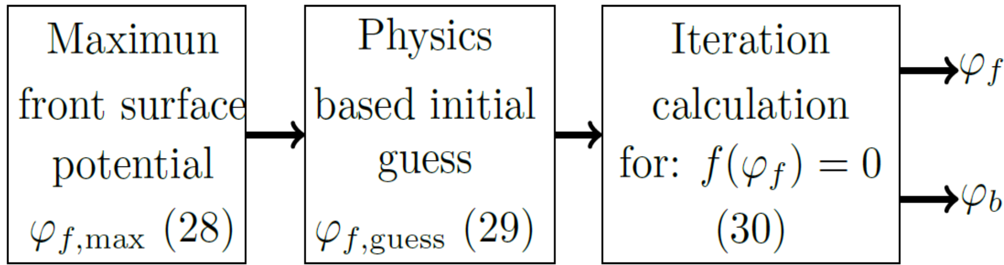
$$f(\varphi_f) = (k_f(x_f - \varphi_f) + \alpha \coth(\alpha/2))(k_f(x_f - \varphi_f) + k_b(x_b - \varphi_b)) - A_0 e^{\varphi_f} = 0$$

$$\varphi_b = \varphi_f - \ln(k_f(x_f - \varphi_f) + \alpha \coth(\alpha/2)) + \ln\left(\frac{\alpha}{\sinh(\alpha/2)}\right)^2 \quad ....(4)$$



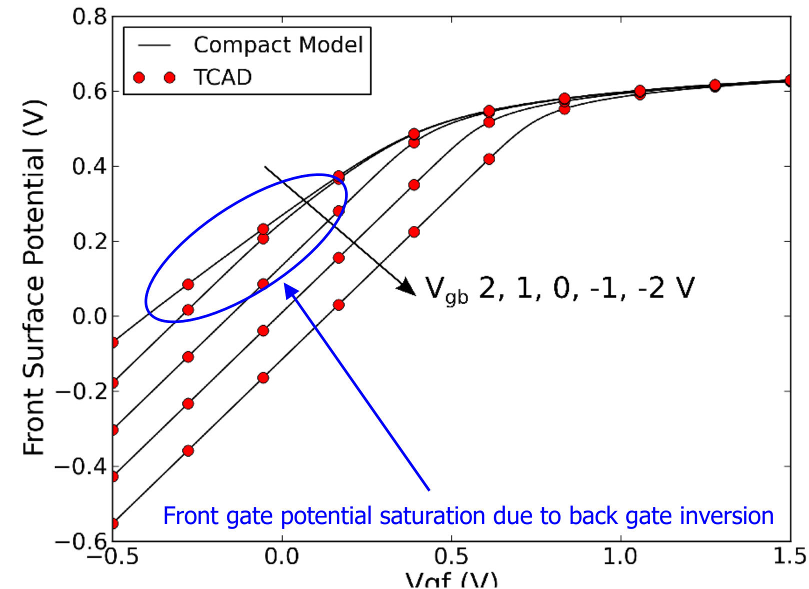
Variable	Definition
x_f, x_b, v_T	$\frac{V_{GF} - \Delta\Phi_f}{v_T}, \frac{V_{GB} - \Delta\Phi_b}{v_T}, \frac{kT}{q}$ (thermal voltage)
φ_f, φ_b	$\frac{\phi_f}{v_T}, \frac{\phi_b}{v_T}$
$C_{ox,f}, C_{ox,b}, C_{ch}$	$\frac{\varepsilon_{ox,f}}{EOT_f}, \frac{\varepsilon_{ox,b}}{EOT_b}, \frac{\varepsilon_{ch}}{T_{cg}}$
$k_f, k_b, k_{eq,f}, k_{eq,b}$	$\frac{C_{ox,f}}{C_{ch}}, \frac{C_{ox,b}}{C_{ch}}, \frac{k_b}{k_f k_b + k_f + k_b}, \frac{k_f}{k_f k_b + k_f + k_b}$
A_0	$\frac{2qn_i\varepsilon_{ch}}{C_{ch} v_T}$
q_m	$\frac{Q_m}{v_T C_{ch}}$

Extended Range Core Model: Analytical Solution

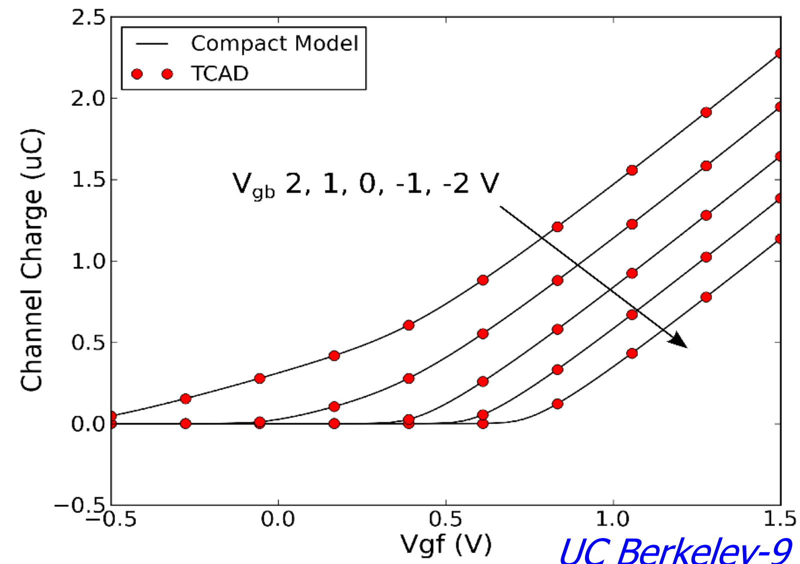


$$-4\pi^2 = k_f(x_f - \varphi_{f,\max})^2 - A_0 e^{\varphi_{f,\max}} \quad \text{....(5)}$$

$$\varphi_{f,\text{guess}} = \max_s\left(\frac{rEOT_f(x_f - x_b)}{T_{fin} + r(EOT_f + EOT_b)} + x_b, \varphi_{f,\max}\right) \quad \text{....(6)}$$

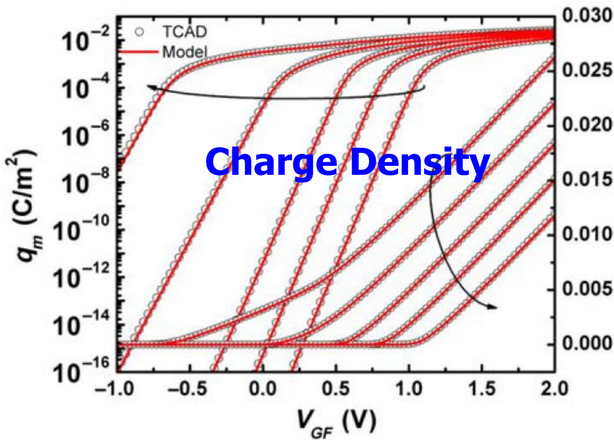


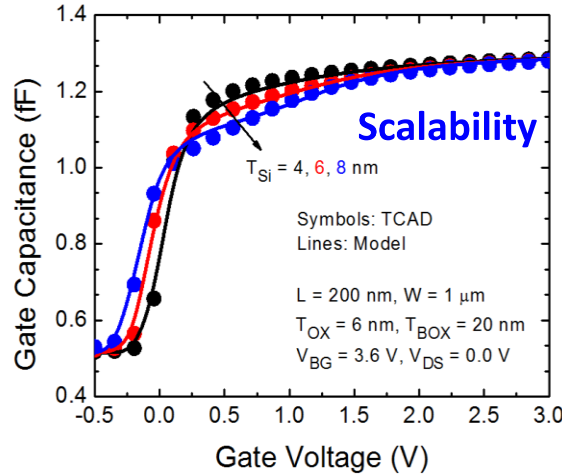
Solving (6) and using proper initial guess in Newton raption algorithm:
Analytical Surface potential of (4) is obtained

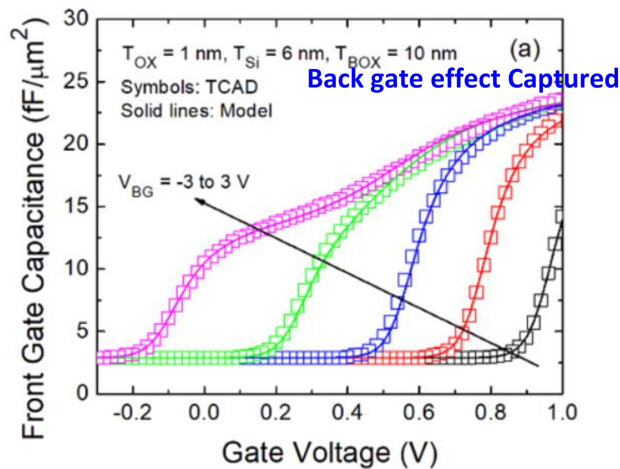


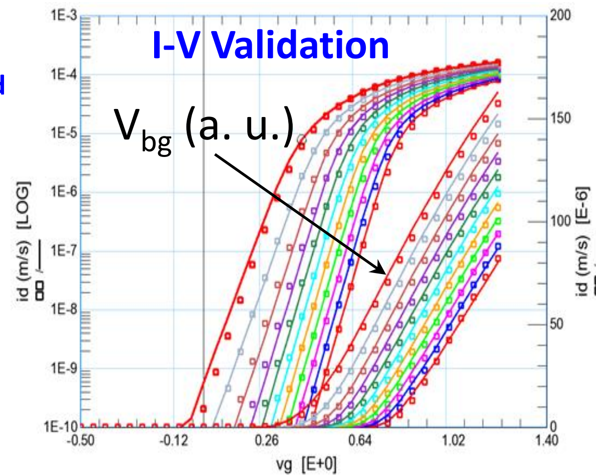
Channel current, Charge and Capacitance Model

Extended Range Core Model



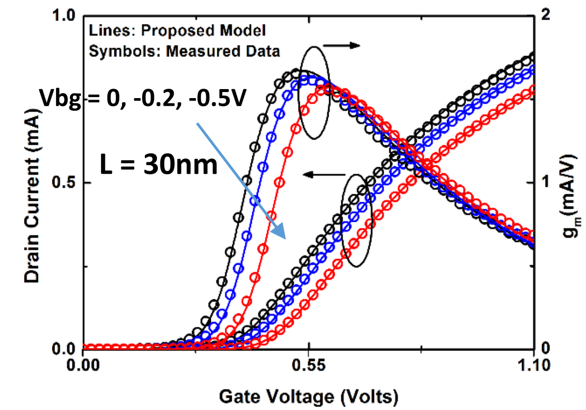




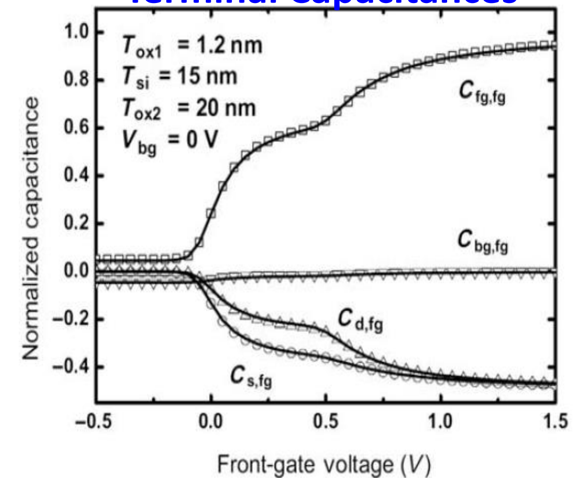


Fast Core Model

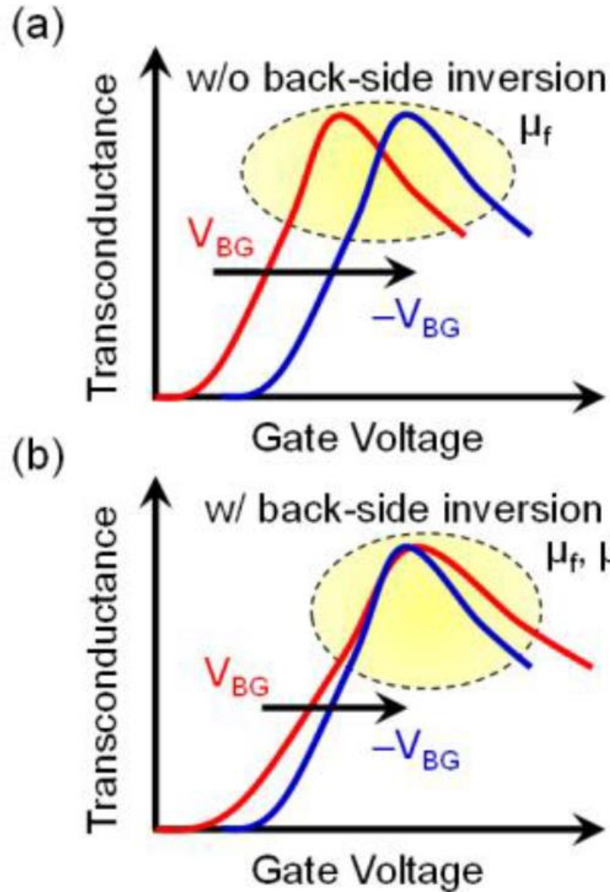
I-V Validation

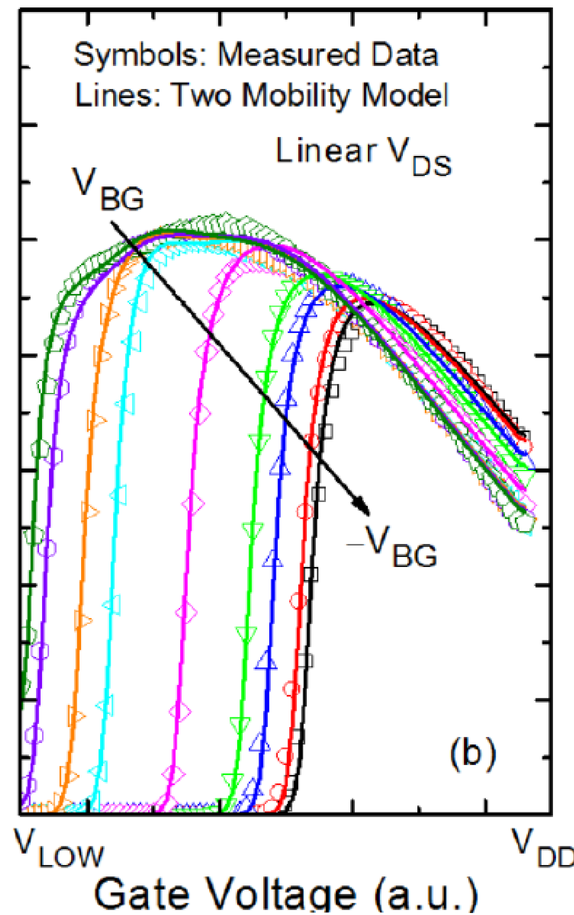


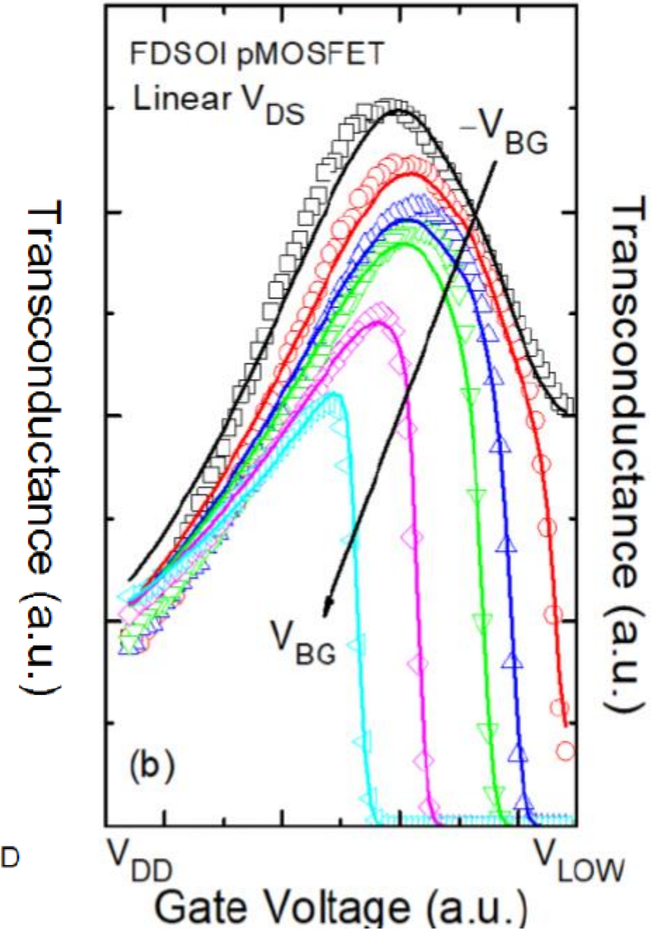
Terminal Capacitances



Dual Mobility Model: gm Double Hump Behavior







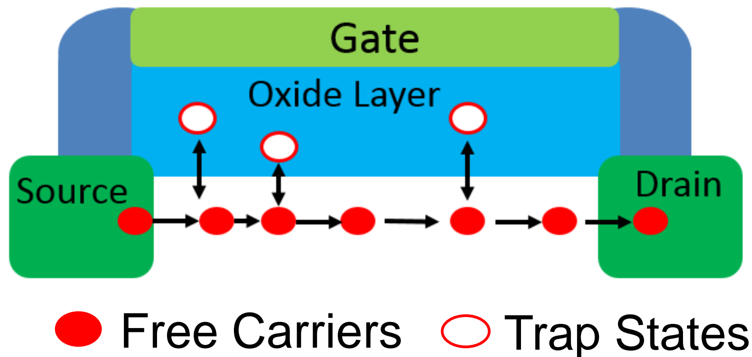
$$\mu_{t,\mathrm{eff}} = w \cdot \mu_{\mathrm{eff,fg}} + (1 - w) \cdot \mu_{\mathrm{eff,bg}}$$

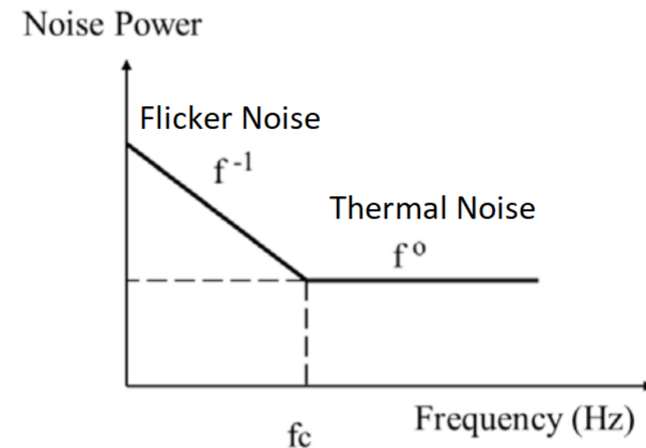
W is the weighting function

Thermal Noise Models in BSIM-IMG

- The major sources of noise in a transistor are the thermal noise and the flicker noise.

- Flicker Noise: Created by carrier trapping and de-trapping.



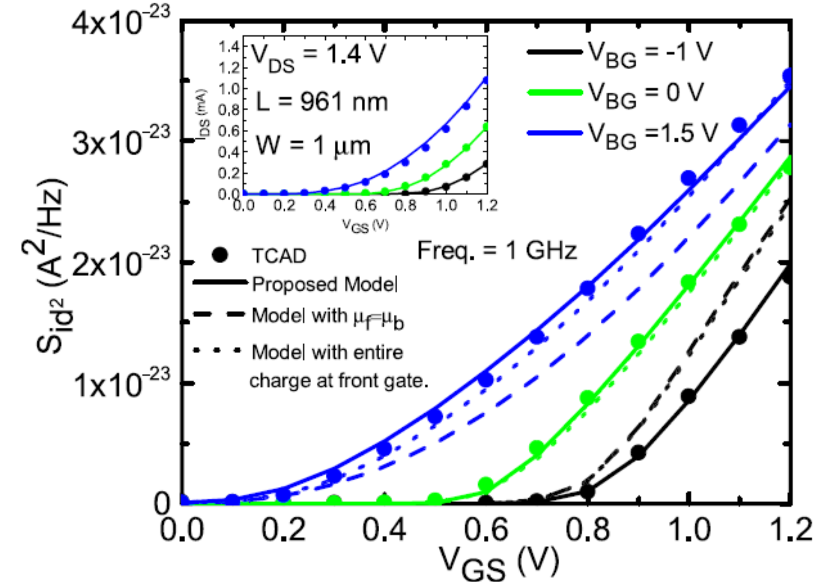


- Thermal Noise: Created by random motion of carriers due to thermal excitation.

Thermal Noise Models in BSIM-IMG

Earlier models only uses front gate for thermal noise PSD calculation

$$S_{id^2} = \frac{4K_BT}{I_DL_{vsat^2}} \int_0^{V_{DS}} g^2(V) \cdot dV$$ KP equation



Considering both front and back gate interface

$$g(V) = wC_{ox1}V_t(\mu_f q_f(v) + K\mu_b q_b(v))$$

Performing integration

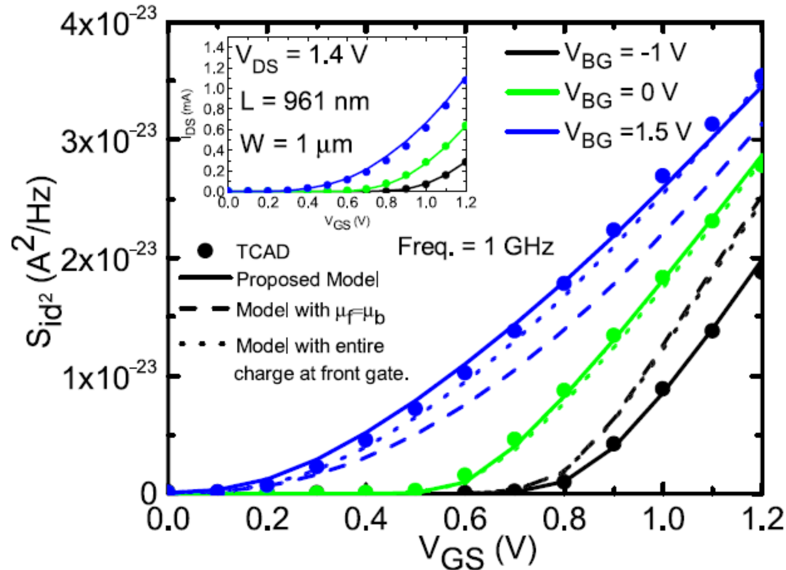
$$S_{id^2} = \frac{4K_BTC_{OX1}Vt^3}{I_DL_{vsat^2}}(A_1 + B_1 + C_1)$$

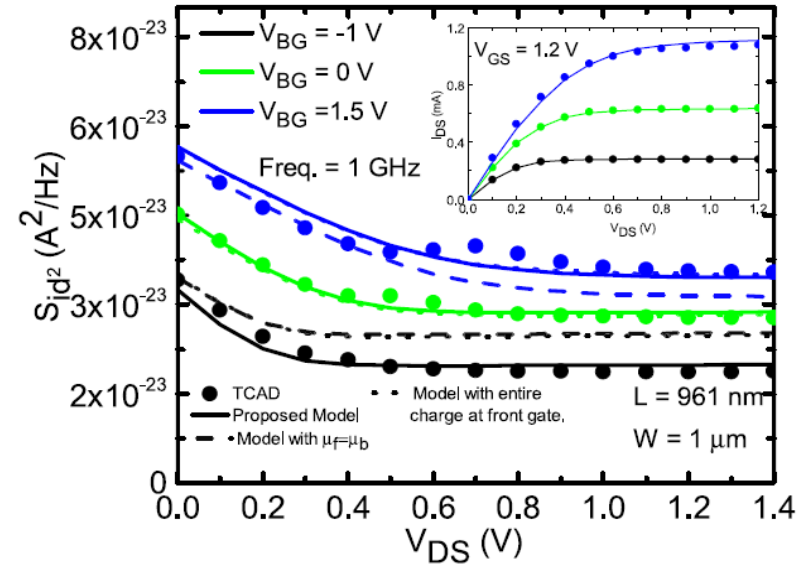
$$A_1 = \mu_f^2(q_{fs} - \beta q_{fd})\left(\frac{q_{fs}^2 + q_{fs}q_{fd} + q_{fd}^2}{3} + \eta_f \frac{q_{fs} + q_{fd}}{2}\right)$$ Front gate contribution

$$B_1 = K^2\mu_b^2(q_{bs} - \beta q_{bd})\left(\frac{q_{bs}^2 + q_{bs}q_{bd} + q_{bd}^2}{3} + \eta_b \frac{q_{bs} + q_{bd}}{2}\right)$$ back gate contribution

$$C_1 = 2K\mu_f\mu_b q_{b_{av}}(q_{fs} - \beta q_{fd})\left(\frac{q_{fs} + q_{fd}}{2} + \eta_f\right)$$ coupling contribution

Thermal Noise Models in BSIM-IMG





More inversion charges as V_{gs} increases, more scattering, thermal noise

Sid is maximum @ V_{ds} = 0 V, starts to decrease as operating point move towards saturation (charge decreases)

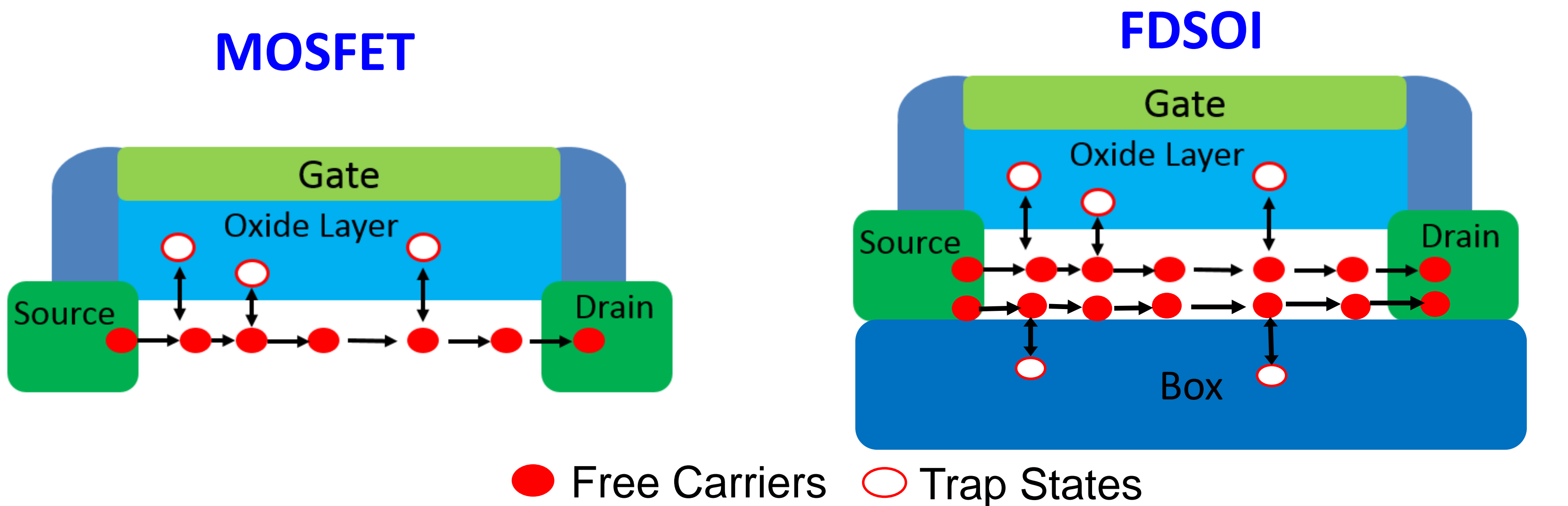
- + V_{bg} -> Vt ↓ -> more carriers -> noise ↑
- + V_{bg} -> Vt ↑ -> more carriers -> noise ↓

- + V_{bg} -> Vt ↓ -> more carriers -> noise ↑
- + V_{bg} -> Vt ↑ -> more carriers -> noise ↓

Y. Sahu, et.al. "Compact Modeling of Drain Current Thermal Noise in FDSOI MOSFETs Including Back-Bias Effect," MTT, vol. 65, no. 7, pp. 2261-2270, July 2017.

Flicker noise – FDSOI MOSFET Models

FDSOI transistor faces more carrier fluctuations due to the presence of the front and back interfaces (carrier trapping and de-trapping)



- Single Si-Sio2 interface
- Scaling issues

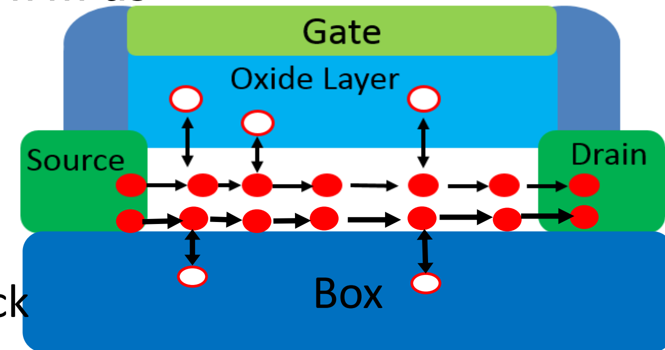
- Dual Si-Sio_2 interface
- Good Scaling solution

P. Kushwaha, et. al. "A Unified Flicker Noise Model for FDSOI MOSFETs Including Back-bias Effect", (CONECCT), Bengaluru, India, Mar. 2018.

Flicker noise – BSIM-IMG Model

The charge fluctuations near both interfaces contribute to total inversion charge fluctuation (*dQinv*) in thin silicon film as

$$dQ_{inv} = \underbrace{\frac{\partial Q_{inv}}{\partial N'_{t1}} dN'_{t1}}_{\text{Front Interface}} + \underbrace{\frac{\partial Q_{inv}}{\partial N'_{t2}} dN'_{t2}}_{\text{Back Interface}} \quad \text{----- (1)}$$



Fluctuation in the amount of trapped oxide charges at front/back interfaces will cause

- Correlated fluctuation in effective mobility
- Correlated fluctuation in carrier number

} ultimately fluctuates the current

$$\frac{dI_{ds}}{I_{ds}} = dN'_{t1}[\underbrace{\frac{1}{N'_{t1}}\frac{\partial N'}{\partial N'_{t1}}}_{R_{front}} + \underbrace{\frac{1}{\mu_{eff}}\frac{\partial \mu_{eff}}{\partial N'_{t1}}}_{\mu_{N_{t1}} * \alpha_1}] + dN'_{t2}[\underbrace{\frac{1}{N'_{t2}}\frac{\partial N'}{\partial N'_{t2}}}_{R_{back}} + \underbrace{\frac{1}{\mu_{eff}}\frac{\partial \mu_{eff}}{\partial N'_{t2}}}_{\mu_{N_{t2}} * \alpha_2}] \quad \text{----- (2)}$$

$$R_{back} = \frac{\delta \Delta N}{\delta \Delta N_{t2}} = \frac{\partial Qinv_{norm}}{\partial V_{bg}} = C_{ox1}\left(\frac{\partial V_{fg,eff}}{\partial V_{bg}} - \frac{\partial \psi_{s1}}{\partial V_{bg}}\right) + \frac{C_{si}.C_{ox2}}{C_{si}+C_{ox2}}\left(1 - \frac{\partial \psi_{s1}}{\partial V_{bg}}\right)$$

$$R_{front} = \frac{\delta \Delta N}{\delta \Delta N_{t1}} = \frac{\partial Qinv_{norm}}{\partial V_{fg}} = -\frac{1}{C_{box}}\frac{N}{N+N_1^*}; N_1^* = \frac{KT}{q^2}(C_{ox}+C_{it})$$

Flicker noise – BSIM-IMG Model

From the number fluctuation theory and following assumptions

- Oxide trap have a uniform distribution near the interface
- Tunneling probability decreases exponentially in vertical direction

$$S_{\Delta Ids}(x,f)=\left(\frac{I_{ds}}{W\cdot\Delta x}\right)^2\left(\frac{R_{front}}{N}\pm\alpha_1\mu_{eff}\right)^2 S_{\Delta N_{t1}}(x,f)+\left(\frac{I_{ds}}{W\cdot\Delta x}\right)^2\left(\frac{R_{back}}{N}\pm\alpha_2\mu_{eff}\right)^2 S_{\Delta N_{t2}}(x,f) \quad (3)$$

→ PSD of local current fluctuation

$$S_{\Delta N_{t1/t2}}(x,f)=N_{t1/t2}(x,f)\left(\frac{kT\cdot W\cdot\Delta x}{\gamma\cdot f}\right)$$

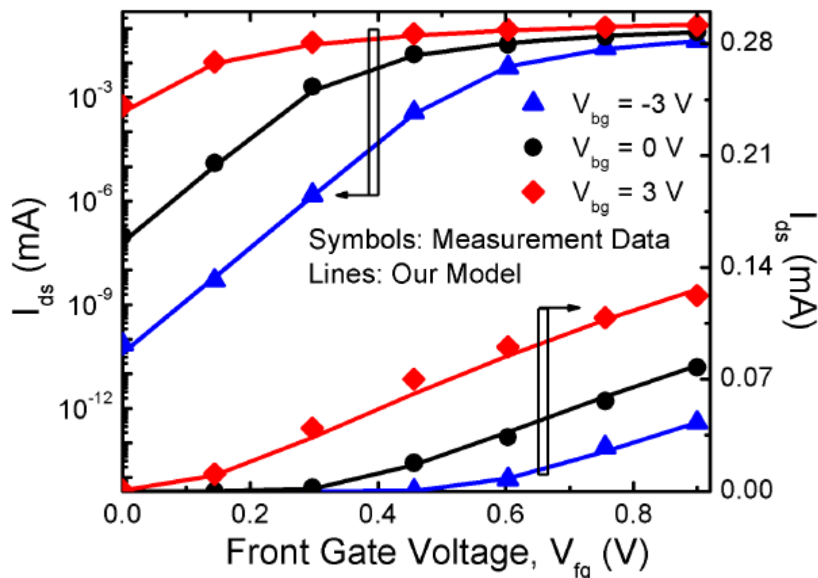
→ PSD of mean square fluctuation

→ Total drain current noise PSD

$$S_{Ids}(f)=\frac{1}{L^2}\int_0^L S_{\Delta Ids}(x,f)\cdot\Delta x\cdot dx =\frac{kT\cdot q\cdot I_{ds}\cdot\mu_{eff}}{\gamma\cdot f\cdot L^2}\int_0^{V_{ds}}\left[N_{t1}^*(E_{fn})\frac{R_{front}^2}{N}+N_{t2}^*(E_{fn})\frac{R_{back}^2}{N}\right]dV \quad (4)$$

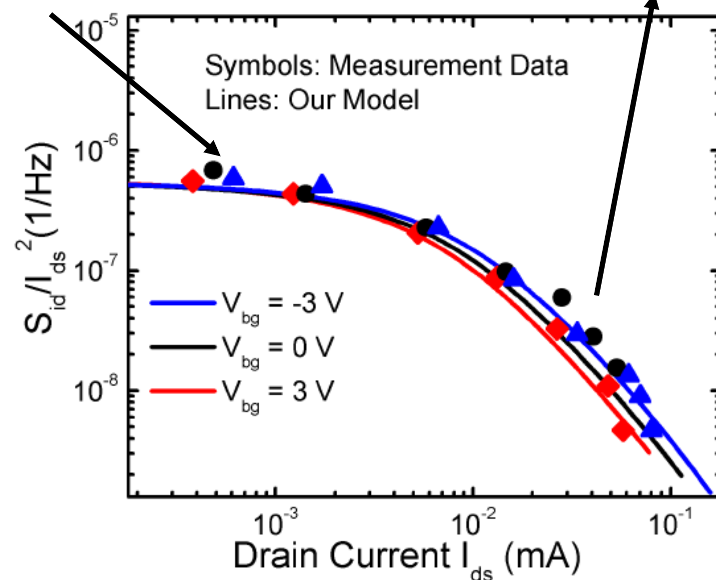
$N_{t1/t2}^*(E_{fn})$ = Trap distribution around quasi Fermi level – Delta function

Flicker noise – BSIM-IMG Model

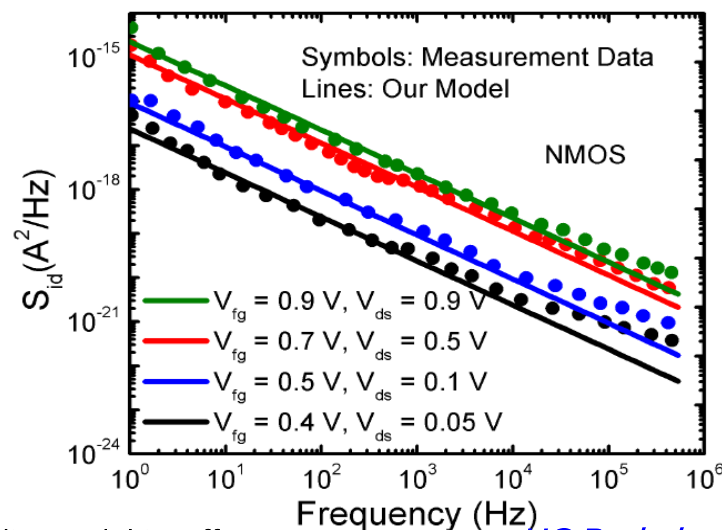


Negligible effect of back-bias (CNF)

Mobility fluctuates With back-bias(CMF)



- **The threshold voltage shift due to different back gate biases is captured very well.**
- **Model is following CNF model in weak inversion region.**
- **Model is following CMF model in strong inversion region.**
- **Model shows correct trends (1/f –like spectra) for all drain biases which implies model's robustness from linear to saturation region.**



P. Kushwaha, et. al. "A Unified Flicker Noise Model for FDSOI MOSFETs Including Back-bias Effect, CONECCT 2018.

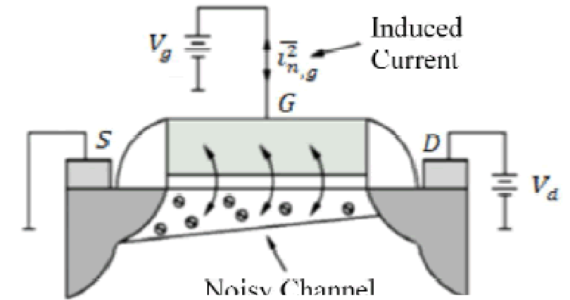
Gate induced noise – BSIM-IMG Model

Channel charge fluctuation cause a redistribution of the channel potential which results in a charge redistribution across the gate capacitor. This fluctuation is capacitively coupled to the gate charge at the RF frequency, and result in a noise current (rate of change of charge) at the gate terminal.

KP equation

$$S_{ig^2} = P_{S_{ig^2}} \int_{V_s}^{V_d} {g_0}^2(v) \left[\int_{V_s}^{V_d} (Q(u) - Q(v)) g_0(u) du \right]^2 dv$$

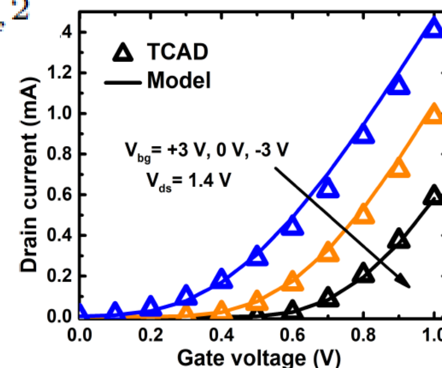
$$S_{ig,id} = P_{S_{ig,id}} \int_{V_s}^{V_d} {g_0}^2(v) \int_{V_s}^{V_d} g_0(u)(Q(u) - Q(v)) du dv$$

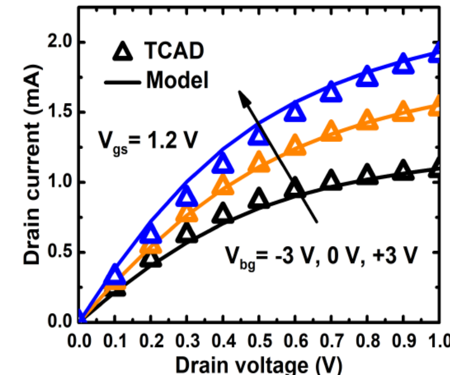


$$P_{S_{ig^2}} = \frac{16\pi^2 kT f^2 W^2}{{I_{ds}}^5 {L_{eff}}^2} \quad P_{S_{ig,id}} = \frac{-j8\pi kT fW}{{I_{ds}}^3 {L_{eff}}^2}$$

$$Q = C_{ox1} V_t \left(q_f + K q_b \right)$$

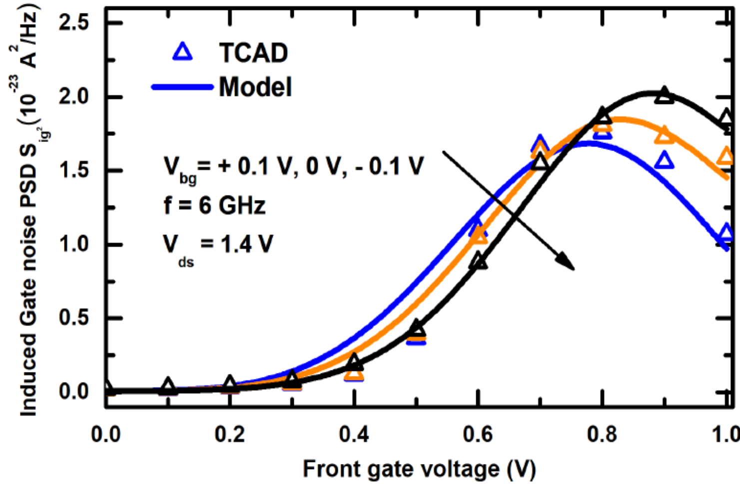
$$Q_{f(b)N} = \frac{q_{f(b)s}^N - q_{f(b)d}^N}{N} + \eta_{f(b)} \frac{q_{f(b)s}^{N-1} - q_{f(b)d}^{N-1}}{N-1}$$

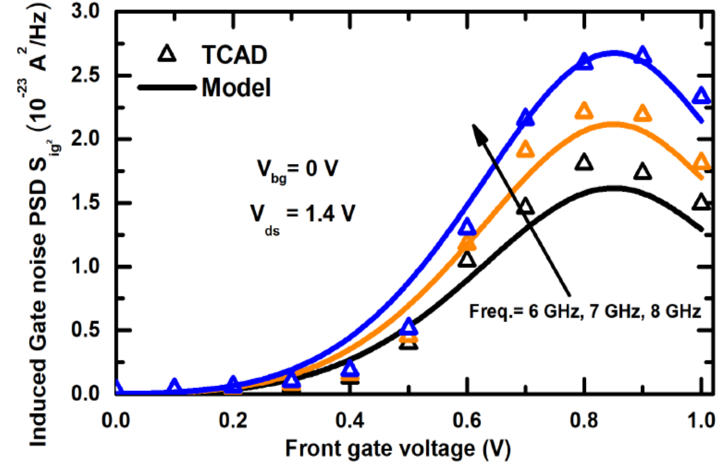




C. K. Dabhi et. al. "Modeling of Induced Gate Thermal Noise Including Back-Bias Effect in FDSOI MOSFET," in *IEEE MWCL*, vol. 28, July 2018.

Gate induced noise – BSIM-IMG Model





- **Increase in semiconductor charge with increasing front gate voltage results in more scattering due to increase in the field and hence more noise.**
- **Increasing the back gate bias also leads to an increase in the total semiconductor charge, resulting in higher noise for higher back gate bias.**

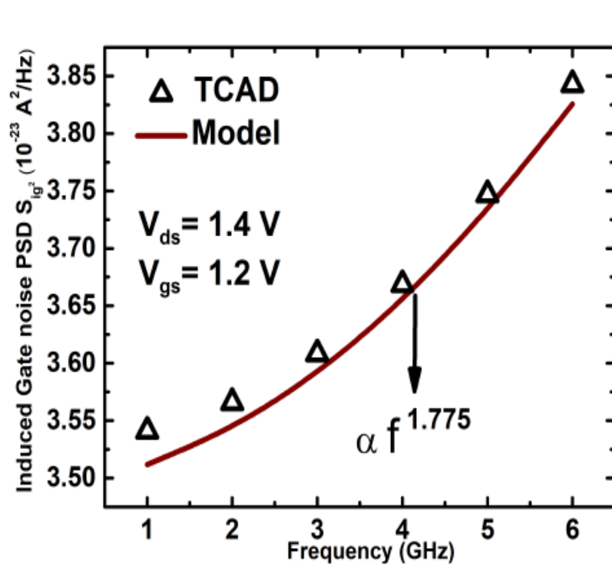
$$S_{ig^2} = \frac{16\pi^2 q f^\theta L_{vsat}{}^3}{W C_{ox}{}^3 V_t{}^9 m_{id}{}^5}(T_I - U_I + X_I)\,;\; S_{ig,id} = \frac{-j8\pi q f L_{vsat}}{C_{ox} V_t{}^3 m_{id}{}^3}\left(\frac{2T_I - U_I}{2P_I}\right)$$

$$T_I = P_I{}^2\left(\mu_f{}^2 Q_{f3} + 2\mu_f\mu_b q_{av} Q_{f2} + \mu_b{}^2 Q_{b3}\right);\; P_I = W C_{ox}{}^2 V_t{}^3\left[\mu_f Q_{f3} + K^2\mu_b Q_{b3} + K q_{av}(\mu_f + \mu_b) Q_{f2}\right]$$

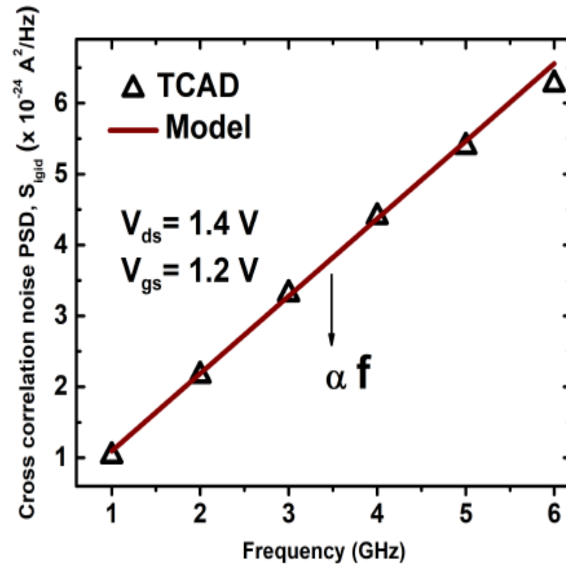
$$U_I = 2P_I W C_{ox}{}^2 V_t{}^3(\mu_f Q_{f2} + \mu_b K Q_{b2})[\mu_f{}^2 Q_{f4} + (\mu_f q_{av} Q_{f3})(\mu_f K + 2\mu_b) + (\mu_b q_{av}{}^2 Q_{f2})(2\mu_f K + \mu_b) + \mu_b{}^2 K q_{av}{}^3 Q_{f1} + \eta_f(log(q_{fs}) - log(q_{fd}))]$$

$$X_I = [W C_{ox}{}^2 V_t{}^3(\mu_f Q_{f2} + \mu_b K Q_{b2})]^2\,[\mu_f{}^2 Q_{f5} + 2q_{av}\mu_f Q_{f4}(\mu_b + \mu_f K) + q_{av}{}^2 Q_{f3}(\mu_b{}^2 + 4\mu_f K\mu_b + K^2\mu_f{}^2) + 2\mu_f\mu_b K^2 q_{av} Q_{f2}(1 + q_{av})]$$

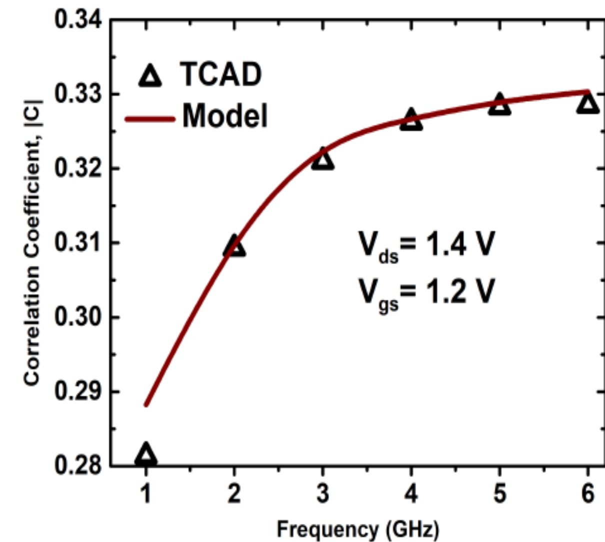
Gate induced noise – BSIM-IMG Model



(a)



(b)



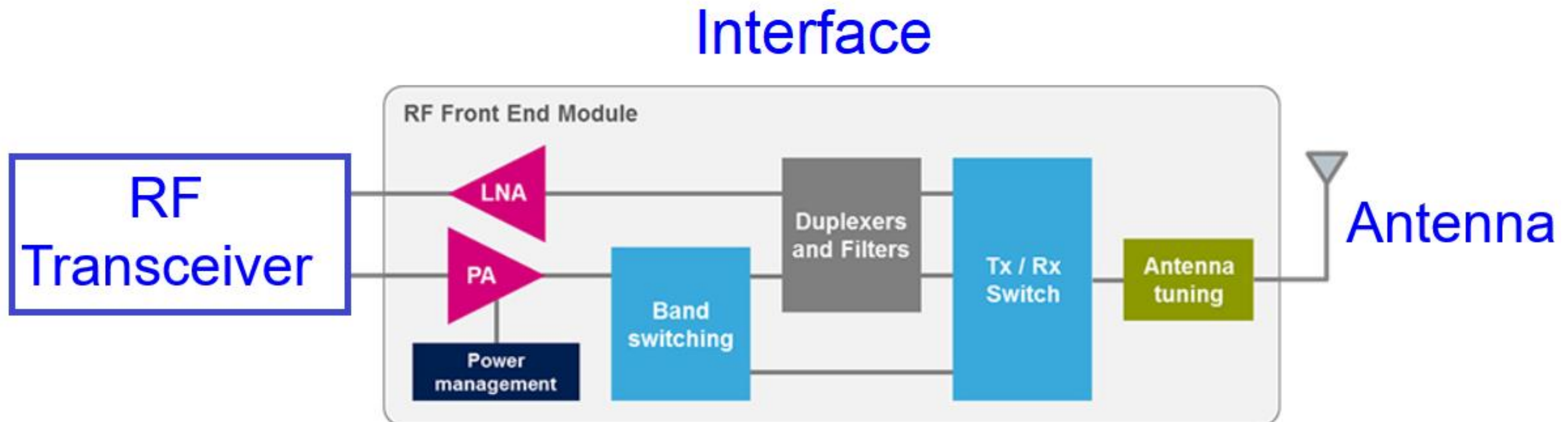
(c)

- **As the frequency increases, the impedance of the effective capacitance coupling between the gate and the channel brings in a frequency dependence**

- **Increase in cross-correlation PSD at higher frequency due to capacitive coupling**

Requirement of RF Modeling of FDSOI MOSFETs

- **In cellular and Wi-Fi systems, the Radio Frequency (RF) Front-End Module is one of the most critical parts.**



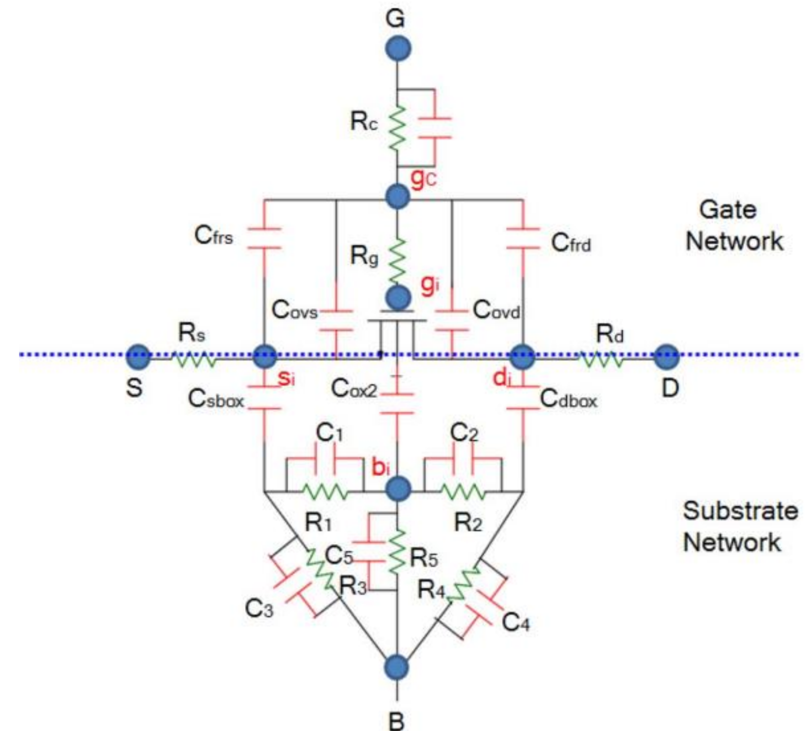
Requirement ⇨ RF circuits

High performance system on chip (SOC), which includes mix signal, complex high power devices, trans-receiver, high resistivity (HR) silicon SOI substrates (RFSOI substrate) make it possible

RF Modeling of FDSOI MOSFETs

- **In MOS devices the effect of parasitic resistances and capacitances showed up at higher frequency.**
- **When MOSFET is operated in gigahertz range, the extrinsic part of the transistor is of more concern than its intrinsic part.**
- **The accurate modeling of the following are highly important.**

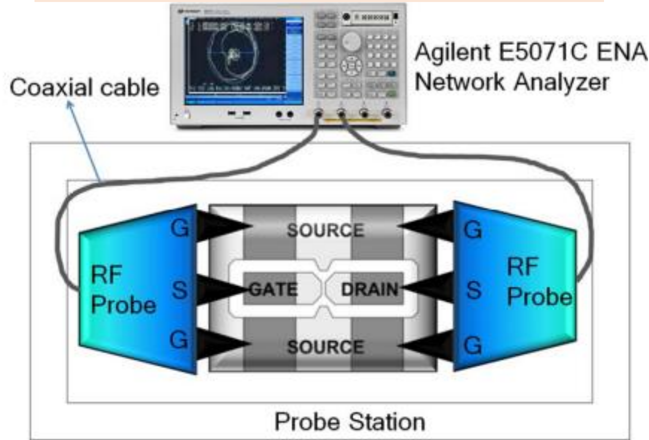
  1: Gate electrode resistance.
  2: Source/Drain series resistance.
  3: Parasitic capacitance.
  4: Substrate resistance.

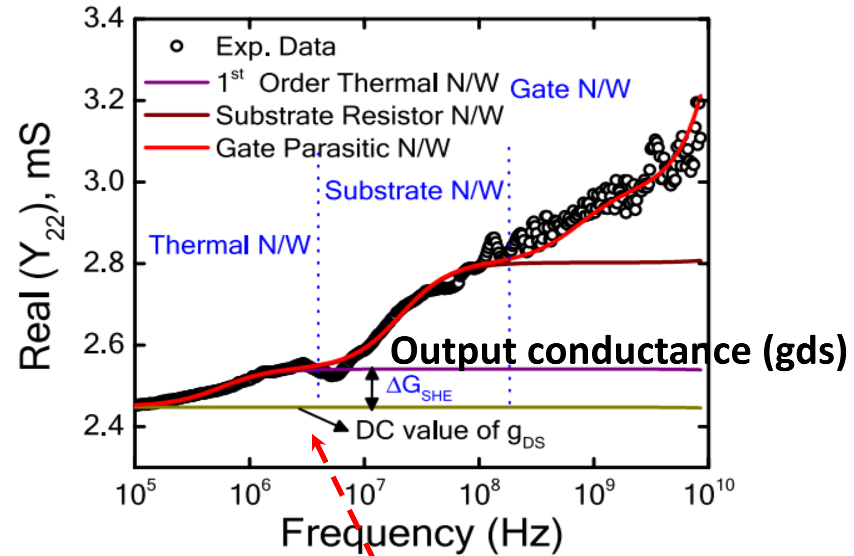


RF Modeling of FDSOI MOSFETs

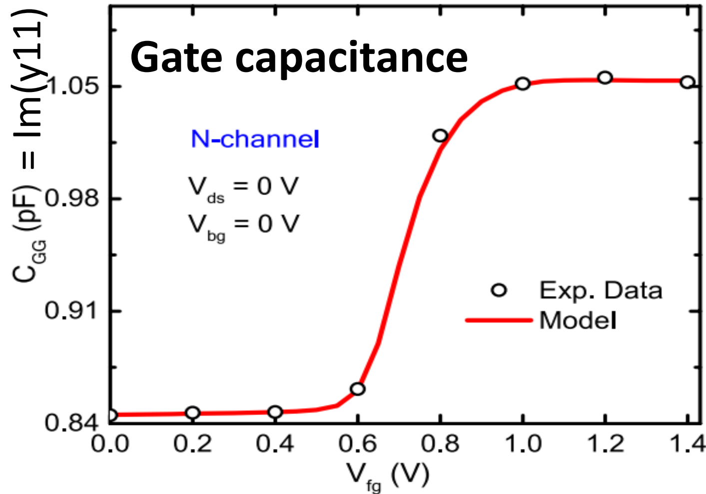
Parameter extraction for DC characteristics

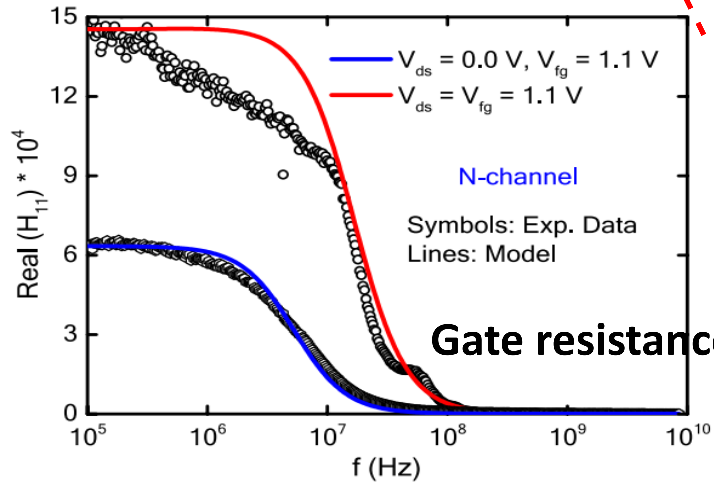
S-parameter measurement

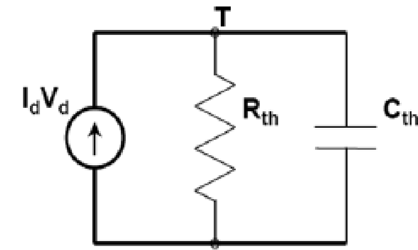




Iso-thermal frequency







Self heating model

P. Kushwaha et. al "RF Modeling of FDSOI Transistors Using Industry Standard BSIM-IMG Model," in *IEEE MTT*, June 2016.

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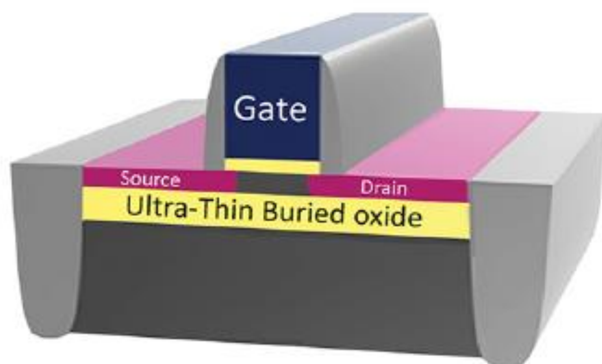

INDUSTRY STANDARD FDSOI COMPACT MODEL BSIM-IMG FOR IC DESIGN

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HARSHIT AGARWAL

ELSEVIER

Recently published BOOK on BSIM-IMG

- **Core Modeling**
- **I-V & C-V Modeling**
- **Leakage Current Modeling**
- **RF and Noise Models in BSIM-IMG**

Summary

- **Core I-V and C-V models for independent multi-gate FETs are developed and verified with TCAD without using fitting parameters**
- **BSIM-like short channel real device effects are implemented.**
- **Double hump gm behavior analysed and modelled**
- **RF and Noise models in BSIM-IMG are developed**

THANK YOU!