

Comparison of 32nm High-k Metal Gate Predictive Technology Model CMOS and MOSFET-Like CNFET compact Model Based Domino logic Circuits

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Outline

- Domino logic 32nm Predictive Technology Model (PTM) based AND, OR gate cells are compared with MOSFET-like Carbon Nano-FET (CNFET) model based AND, OR gate cells
- The analysis done at 25°C and 110°C in HSPICE.
- Static Power, Dynamic Power and Delay measurements are done

Predictive Technology Model (PTM) Low Power 32nm Metal Gate / High-K / Strained-Si



- NMOS Characteristics of BSIM 4.0 Level 54 Nominal Predictive Technology Model Generated using the online tool of Arizona State University

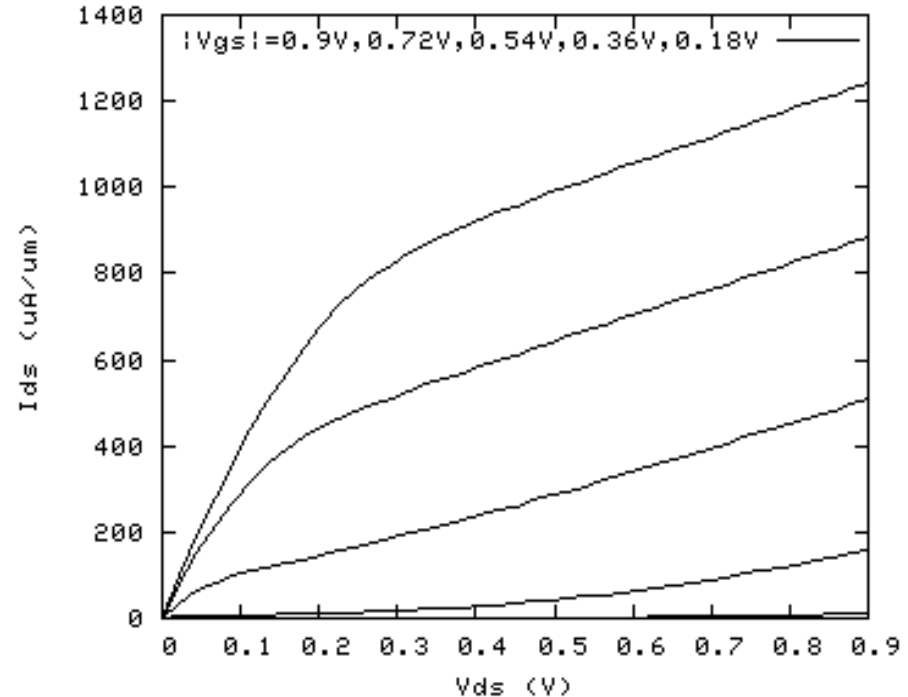
L_{eff} 12.6nm

V_{th} 0.16V

V_{dd} 0.9V

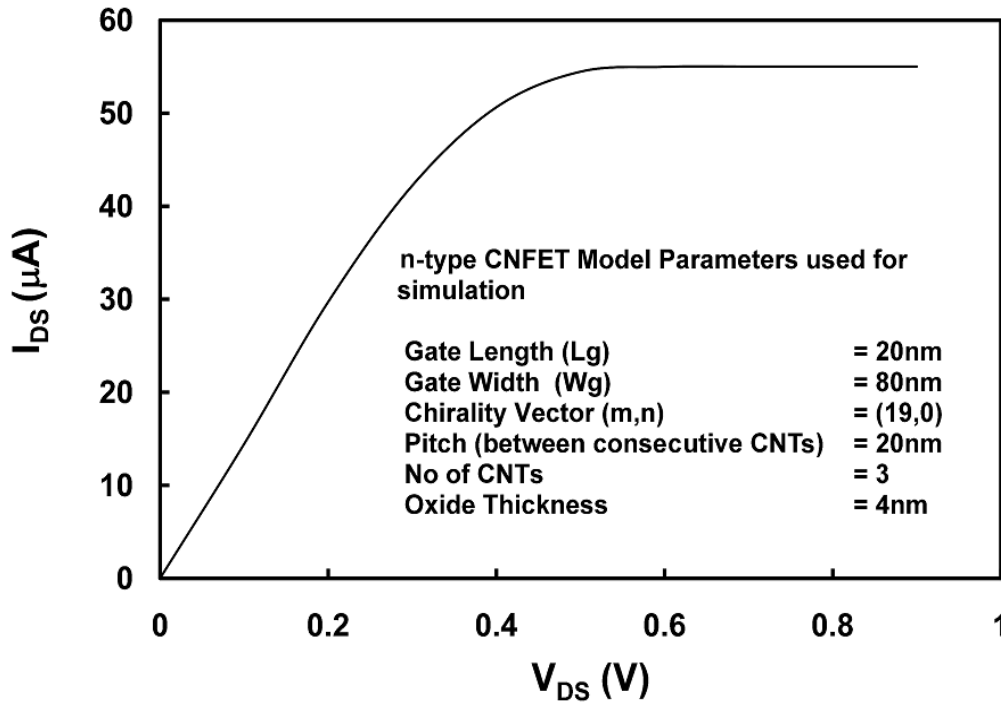
T_{ox} 1nm

R_{dsw} 150 Ohm

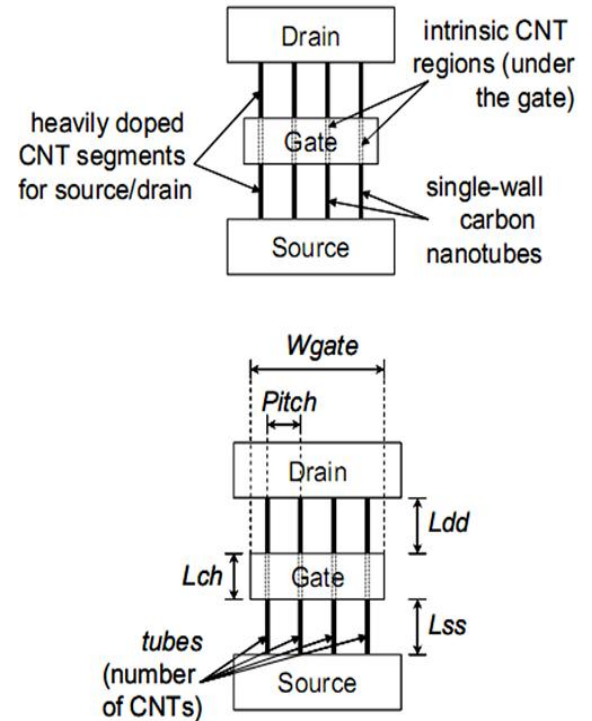


Stanford Single Walled-CNFET MOSFET-like HSPICE Compact Model Characteristics

CNFET drain current vs. drain-to-source voltage (V_{DS}) with 0.9V V_{GS} and substrate (back gate) grounded

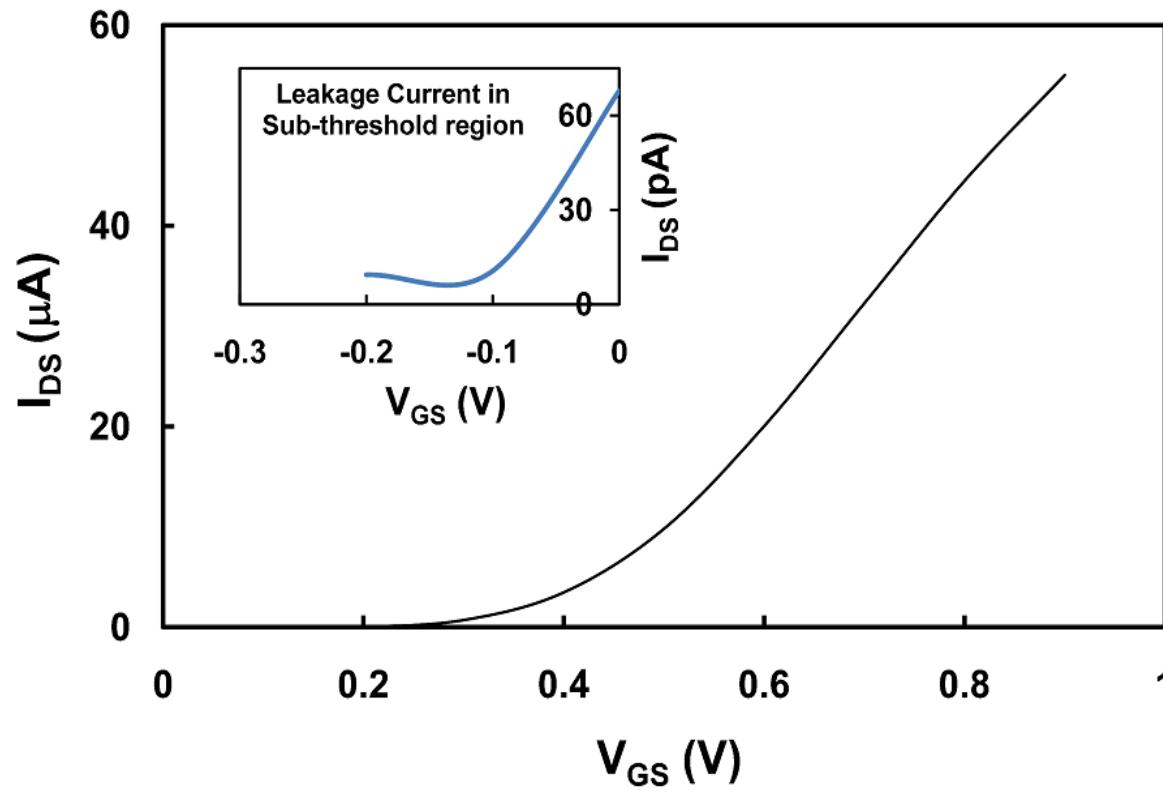


Schematic and model parameters of CNFET compact model



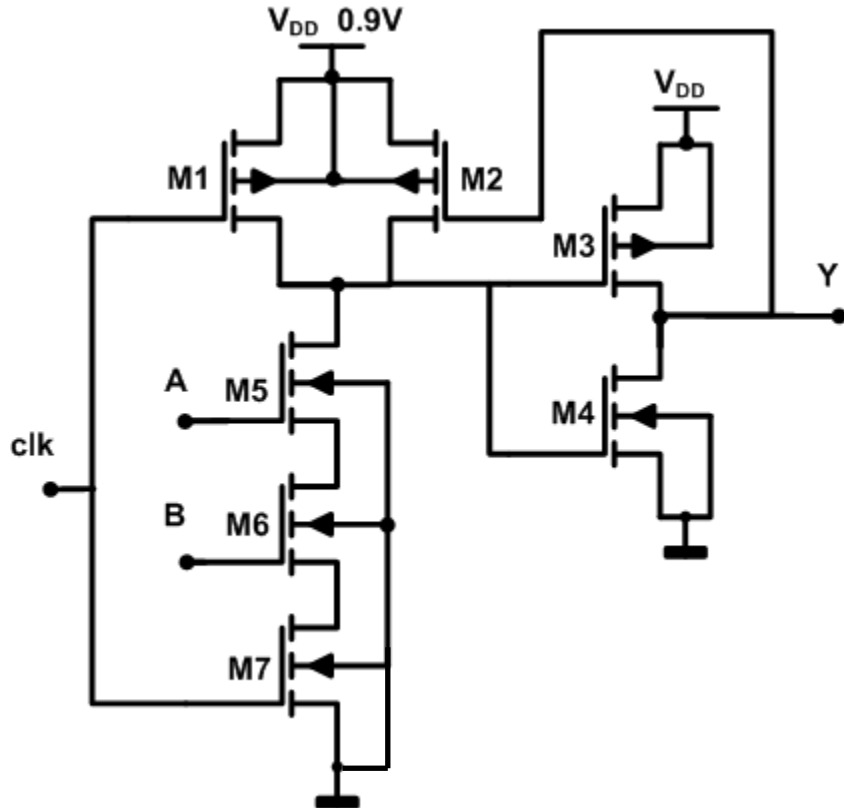
Stanford Single Walled-CNFET MOSFET-like HSPICE Compact Model Characteristics

CNFET drain current vs. drain-to-gate voltage (V_{GS}) with 0.9V V_{DS} and substrate (back gate) grounded

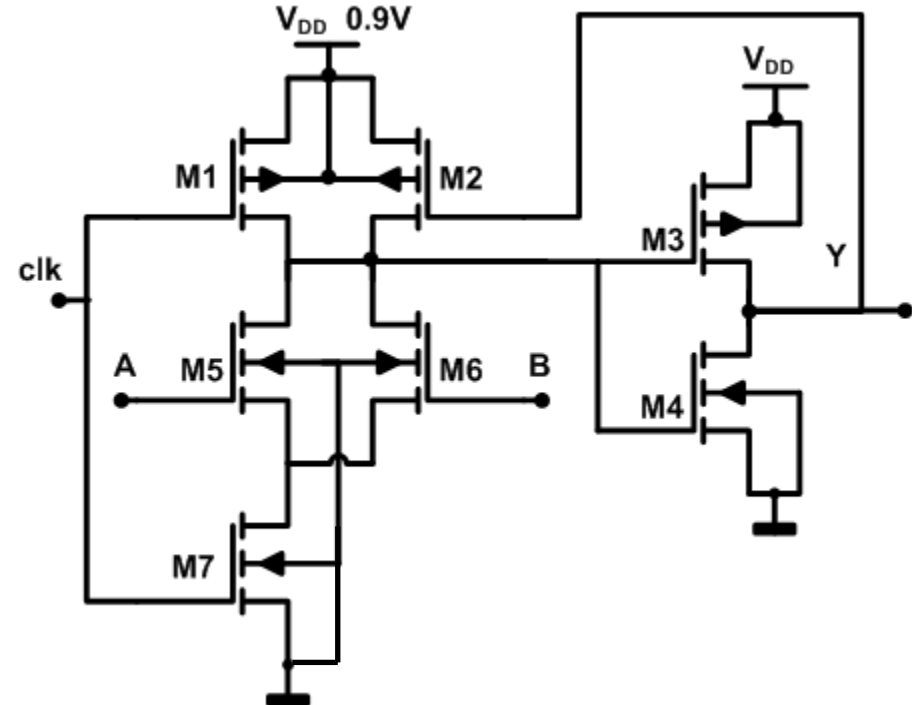


Domino Gates: AND, OR

Domino AND Gate



Domino OR Gate



$V_{DD} = 0.9V$ for both CNFET and 32nm CMOS
Load Capacitance = 0.0002pF

32nm CMOS and CNFET Transistor Dimensions



32nm CMOS PTM Dimensions for Domino AND, OR Gates

Transistor	Channel Width (w) x 10 ⁻⁹ m
M1	80
M2	32
M3	80
M4	40
M5	40
M6	40
M7	40

Channel Length = 32nm
V_{DD} = 0.9V

CNFET Dimensions for Domino AND, OR Gates

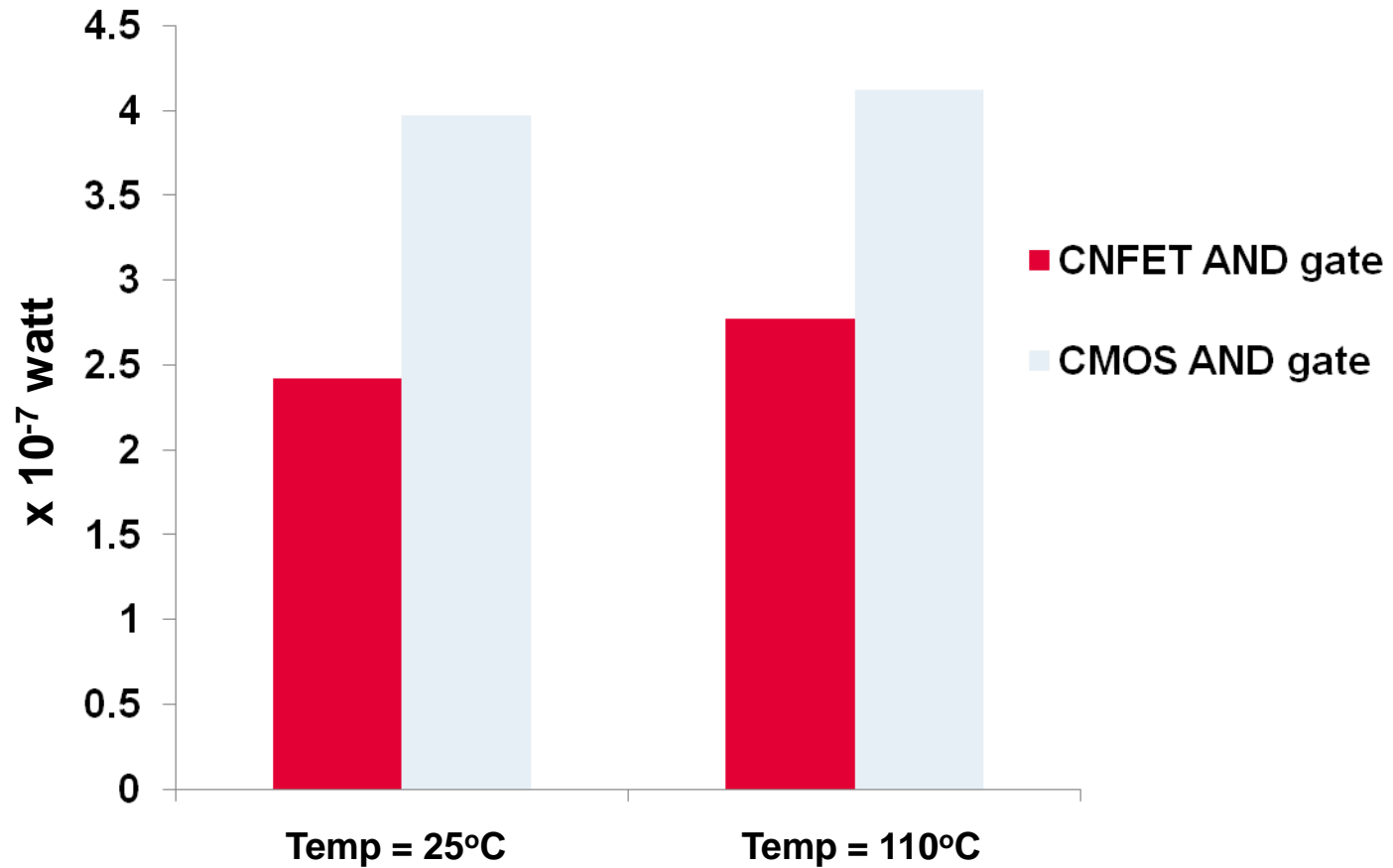
CNFET	Gate Width (Wg) x 10 ⁻⁹ m	Chirality Vector of CNT (m,n)	CNT Count
M1	40	(16,0)	1
M2	32	(16,0)	1
M3	40	(16,0)	1
M4	50	(19,0)	2
M5	50	(19,0)	2
M6	50	(19,0)	2
M7	50	(19,0)	2

Gate Length (Lg) = 20nm
V_{DD} = 0.9V

Static Power Measurement through DC Analysis

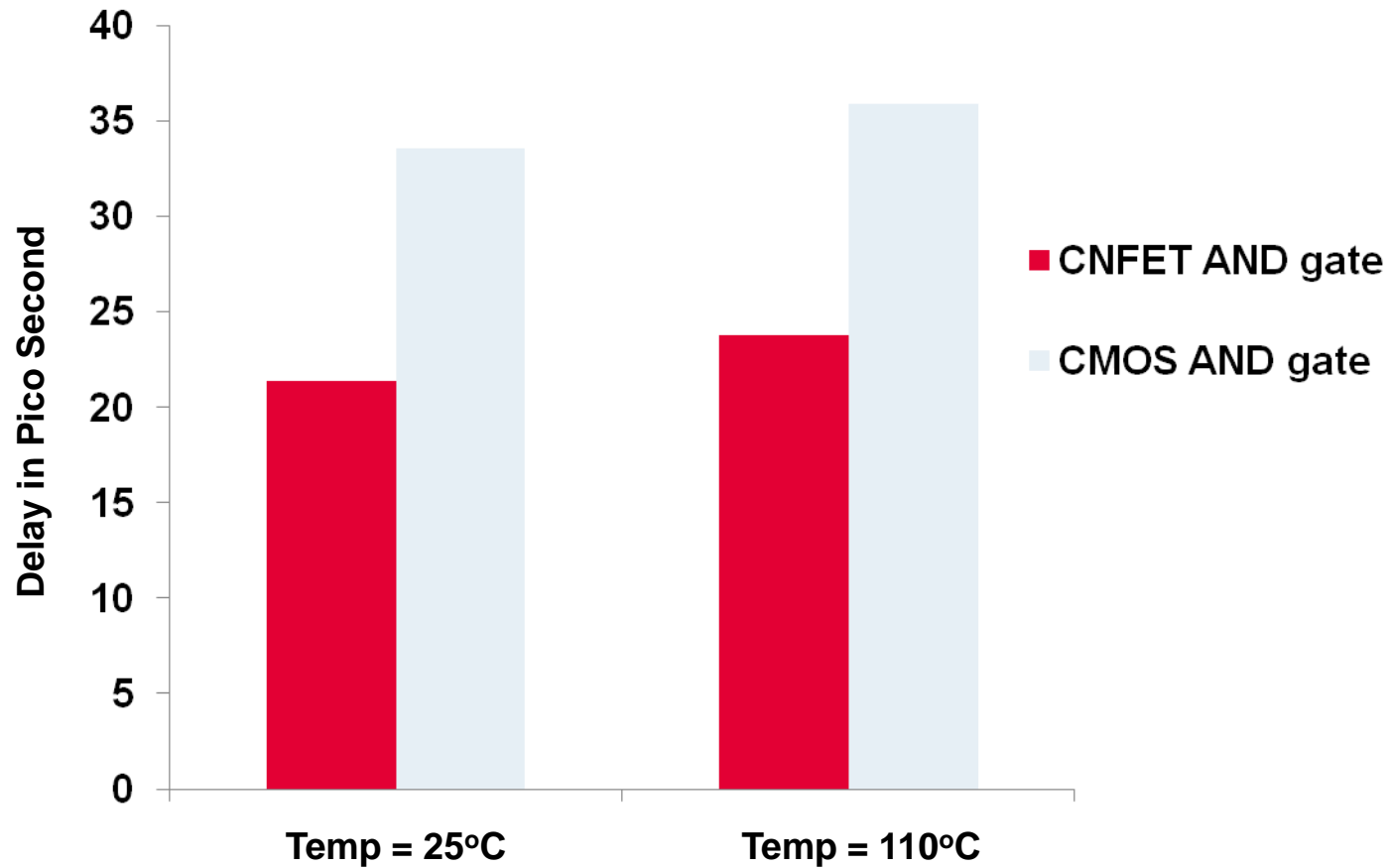
Domino Gate Type	Static Power at 25°C in Pico watt	Static power at 110°C in Pico watt
32nm PTM CMOS AND	9065	17962
CNFET AND	80.47	348
32nm PTM CMOS OR	9214	18516
CNFET OR	92.70	578.60

Dynamic Power of Domino AND Gate During Transient Analysis

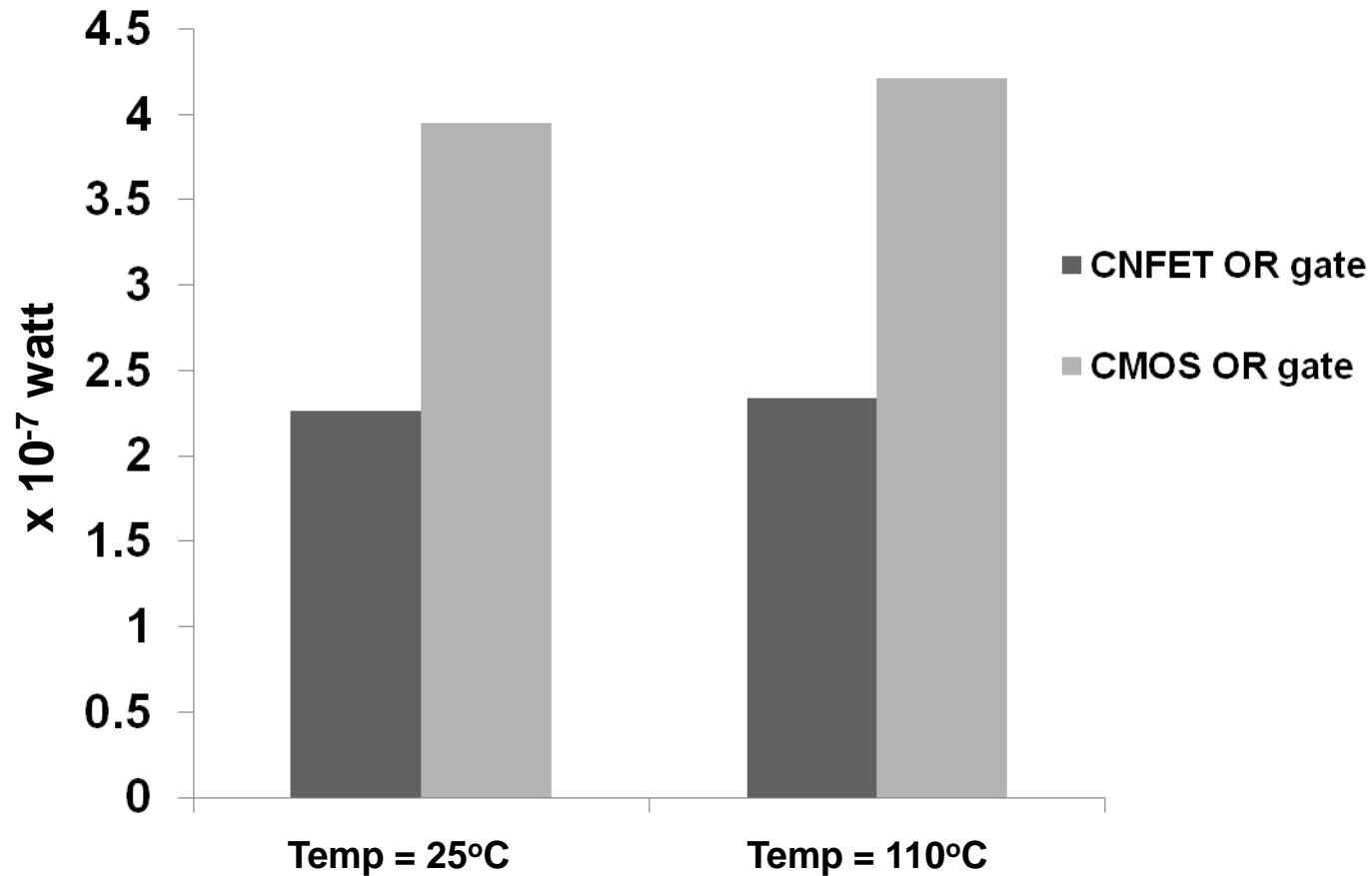


Simulation Results

Delay Measurement using Transient Analysis for Domino AND Gate

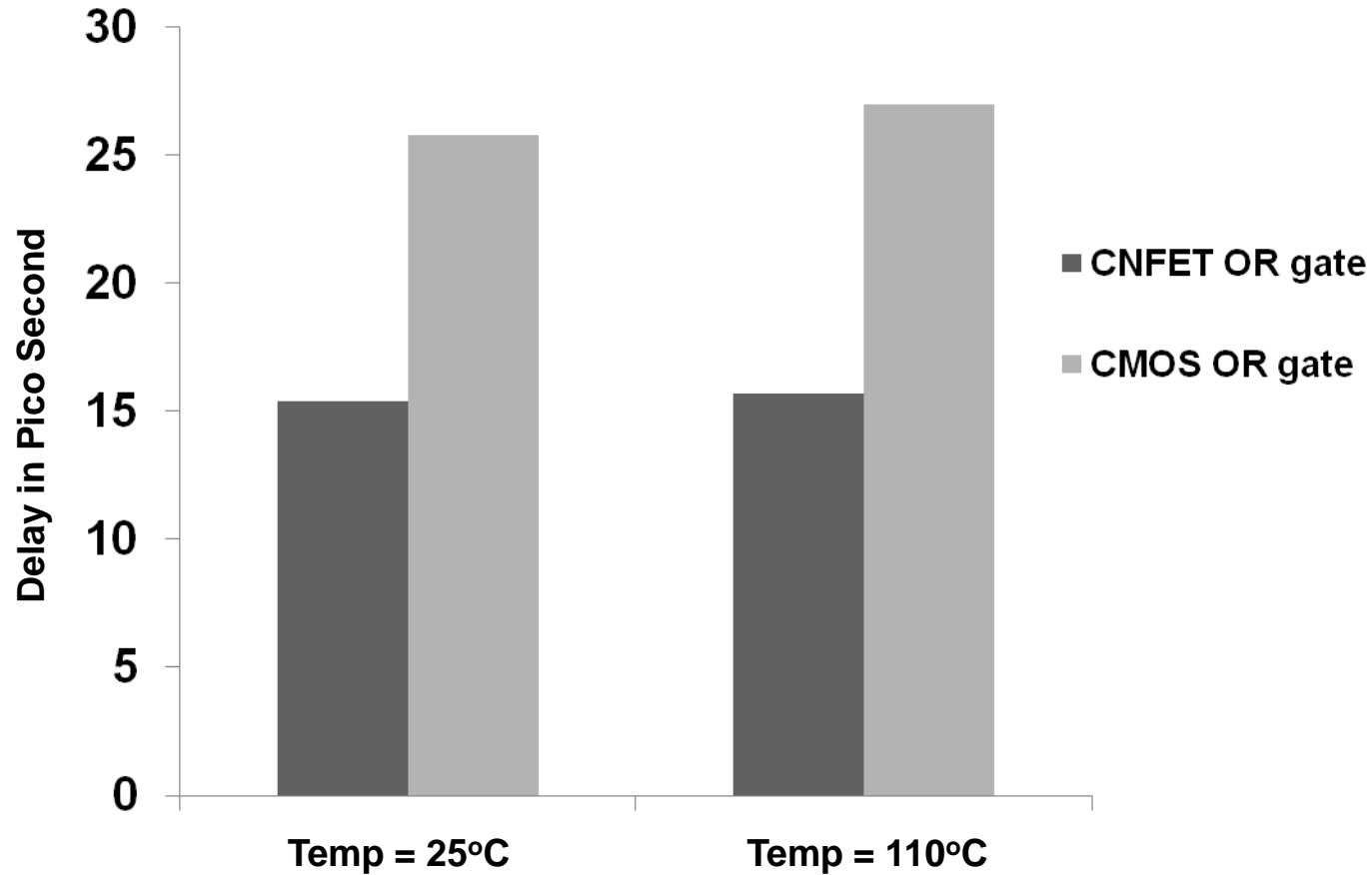


Dynamic Power of Domino OR Gate During Transient Analysis



Simulation Results

Delay Measurement using Transient Analysis for Domino OR Gate



Conclusion

- On comparison at 25°C and 110°C, the CNFET domino OR gate consumes nearly 100% less static power than CMOS Domino OR gate.
- Transient power of CNFET domino OR is nearly 43% lesser than its CMOS counterpart.
- Delay of CNFET Domino OR is 40% lesser than that of CMOS gate.
- In case of Domino AND, CNFET AND gate offers reduction in static power by 99% and transient power of CNFET Domino AND is nearly 40% lesser than that of 32nm CMOS Domino AND gate.
- In terms of delay, CNFET AND gate is 36% faster than CMOS gate. The overall static and dynamic power consumption of the gate is higher at 110°C.

References

- [1] Neil H.E Weste, David Harris, Ayan Banerjee, "CMOS VLSI DESIGN" Third edition, Pearson Education 2006.
- [2] M. Saravana, "Ultra Low Power Dual-Gate 6T and 8T Stack Forced CNFET SRAM Cells", MOS-AK workshop Rome, April 2010. <http://www.mos-ak.org/rome/posters.php>
- [3] Stanford University CNFET HSPICE Model website <http://nano.stanford.edu/model.php?id=23>.
- [4] PTM High Performance 16nm Metal Gate / High-K /Model, Nanoscale Integration and Modeling (NIMO) Group, Arizona State University, <http://www.eas.asu.edu/~ptm/>
- [5] Jie Deng "Device Modeling and Circuit Performance Evaluation For Nanoscale Devices: Silicon Technology Beyond 45 nm Node and Carbon Nanotube Field Effect Transistors", Stanford University, pp. 2-89, Jun. 2007.





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