Compact Model of Independent Gate Asymmetric DGFET

G. Dessai and G. Gildenblat

Arizona State University, USA

MOS-AK 2010, San Francisco, CA

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusion
- Related publications of the PSP group

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusion
- Related publications of the PSP group

Some Advantages of DGFET

- Improved scalability, near-ideal subthreshold slope
- Intrinsic body: high carrier mobility and lower random dopant fluctuation

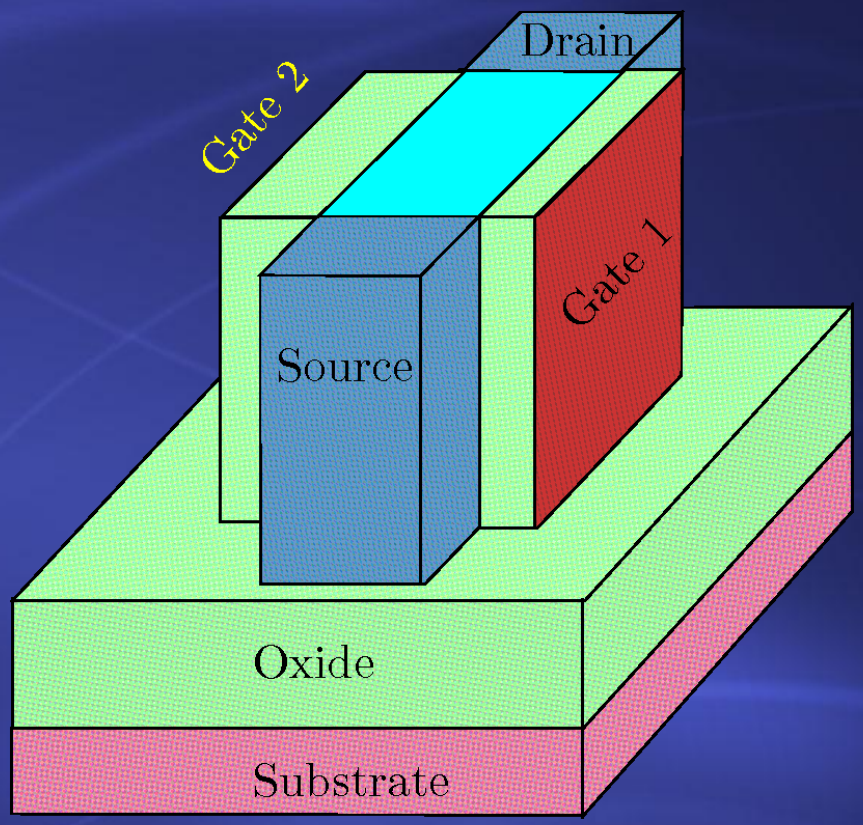
Advantages of Independent Gates

- Dynamic control of threshold voltage and transconductance
- Novel circuit applications
- Optimally designed asymmetric DGFET is found to be superior to its symmetric counterpart

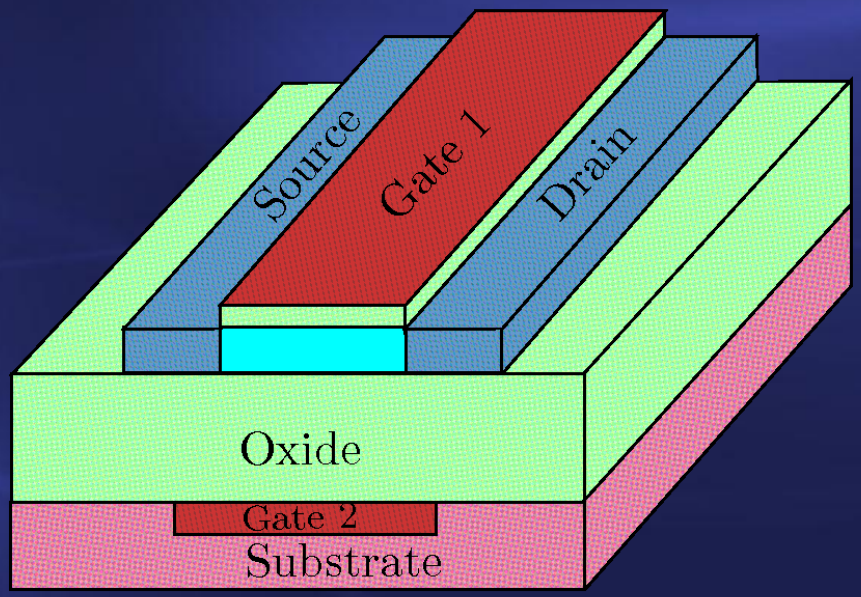
  [Kim and Fossum, TED, vol. 48, no. 2, p. 294, 2001]
- Statistical analysis of the symmetric DGFET may require asymmetric DGFET model. Initial steps: small t_{ox} variation in

  [Chang et al., TED, vol. 56, no. 10, p. 2297, 2009]

Asymmetric Independent Gate DGFET Structures



Independent gate FinFET



ETSOI with back gate

Problems

1. Before one can solve input voltage equations one needs to determine their form (trigonometric or hyperbolic). This itself requires numerical solution.
2. Two input voltage equations are coupled and poorly conditioned, difficult to solve numerically. Analytical approximations are available only for symmetric DGFET.
3. Various combinations of the conduction states of the two surfaces (weak, strong inversion etc.). It is undesirable to neglect the possibility of inversion of the second surface.
4. Exact current model is available, but the difficult part of any compact model is the charge model – not available in the exact closed form.
5. Volume inversion: charge-sheet model cannot be used.
6. New secondary effects (e.g. corner effects). This is not a major issue: if the core model is accurate and converges well, then this can be handled.
7. Many others (e.g. quantum confinement).

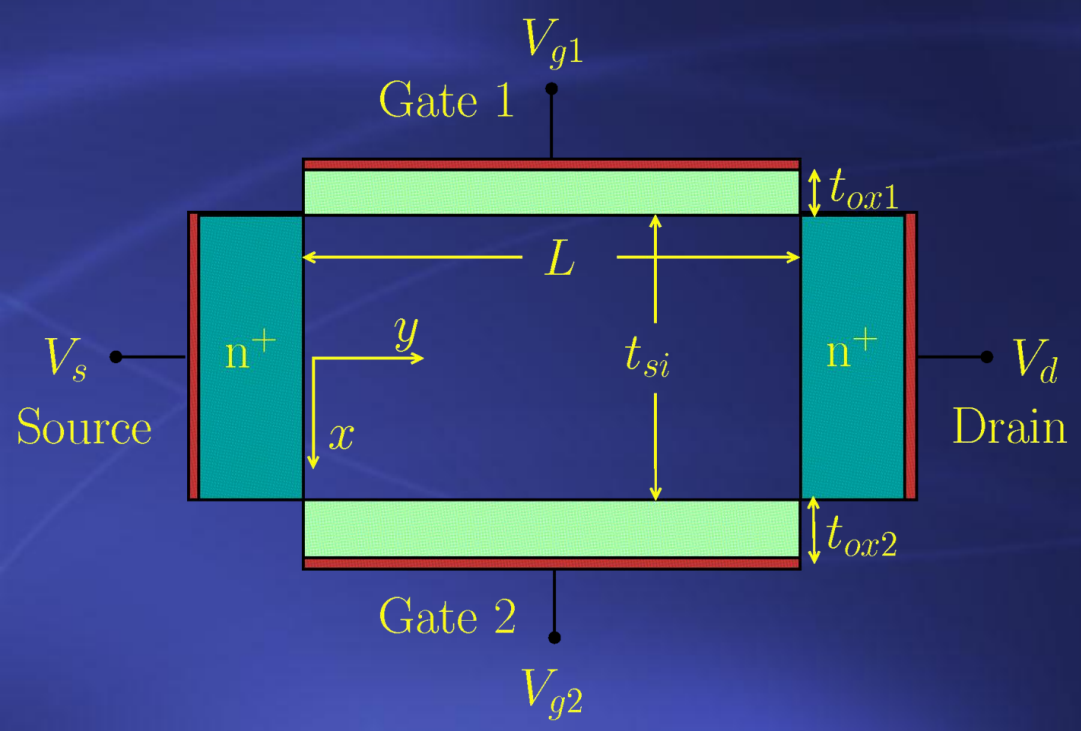
Recent Progress

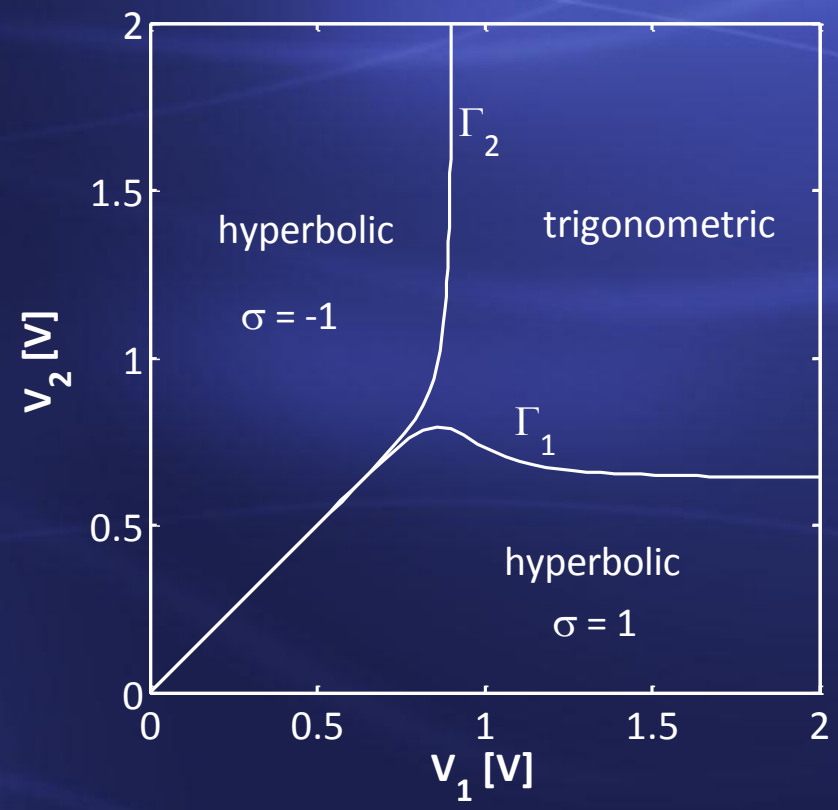
1. Analytical expression for the partition lines on the solution plane.
2. Reformulation of the input voltage equations (IVEs).
3. Reformulation of the charge model. Key idea: make equations isomorphic to the charge-sheet model without actually making this approximation. This is accomplished by introducing the effective charge density which, unlike the true charge density, is a non-linear function of the surface potentials. What is gained? Symmetric linearization of the effective charge leads to accurate equations in a simple and familiar form.
4. PSP framework becomes available. This idea has already been demonstrated to work on the PSP-based models of symmetric DGFET (including small-geometry effects)

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusions
- Related publications of the PSP group

Solution Space





$$V_j = V_{\mathrm{gj}} - \Delta\phi_j; \quad j = 1, 2$$

$$\sigma = \mathrm{sgn}(V_1 - V_2)$$

V_c=0.5 V, t_{si}=10nm, t_{ox1}=2 nm, t_{ox2}=20 nm

[Dessai and Gildenblat, SSE, vol. 54, no. 4, p. 382, 2010]

Solution of Poisson-Boltzmann Equation

Poisson-Boltzmann solution (neglecting hole contribution to charge density) may take trigonometric or hyperbolic form

Trigonometric:

$$\psi(x) = V_{\mathrm{c}} - 2\phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}}}{4L_{\mathrm{d}}\theta} \sin\left(\alpha + \frac{2\theta x}{t_{\mathrm{si}}}\right)\right]$$

Hyperbolic:

$$\psi(x) = V_{\mathrm{c}} - 2\phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}}}{4L_{\mathrm{d}}\theta_*} \sinh\left(\alpha_* + \sigma\frac{2\theta_* x}{t_{\mathrm{si}}}\right)\right]$$

where θ, α, θ_*, and α_* are the integration constants

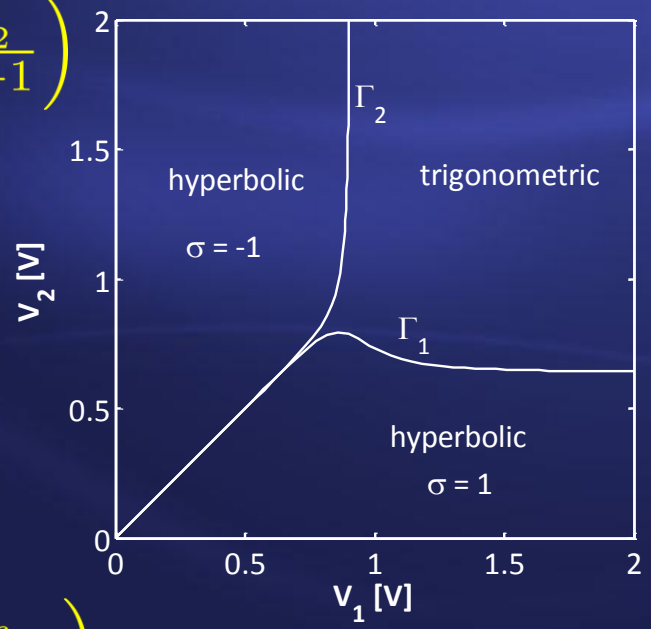
[Y. Taur, TED, vol. 48, no. 12, p. 2861, 2001; H. Lu and Y. Taur, TED,vol. 53, no. 5, p. 1161, 2006]

Analytical Expression for the Solution Space Partition Lines

Equation for Γ_1 ($V_1 > V_2$):

$$\Gamma_1 : V_2 = V_1 - 2\phi_t \ln\left(\frac{s+1}{s-1}\right) - 4\phi_t\left(\frac{r_1}{s-1} + \frac{r_2}{s+1}\right)$$

where, $$s = 1 + \frac{2r_1}{W\left[\frac{r_1 t_{si}}{2L_d}\exp\left(\frac{V_1 - V_c}{2\phi_t}\right)\right]}$$



W is the Lambert W function: $W(x)e^{W(x)}=x$

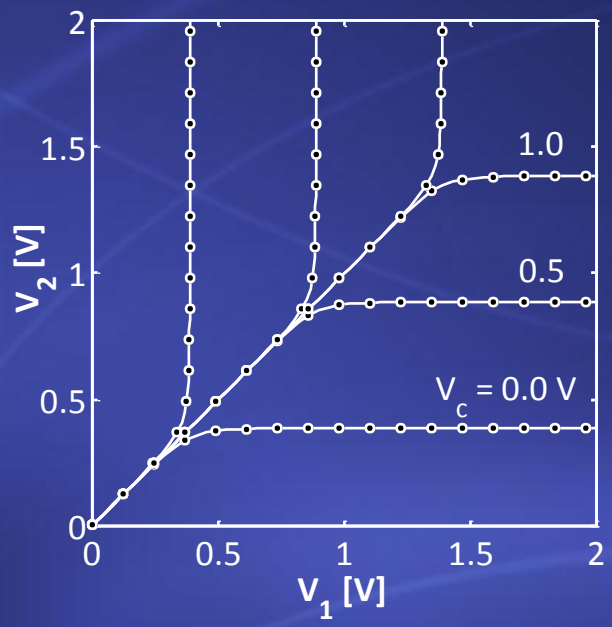
Equation for Γ_2 ($V_2 > V_1$):

$$\Gamma_2 : V_1 = V_2 - 2\phi_t \ln\left(\frac{s+1}{s-1}\right) - 4\phi_t\left(\frac{r_2}{s-1} + \frac{r_1}{s+1}\right)$$

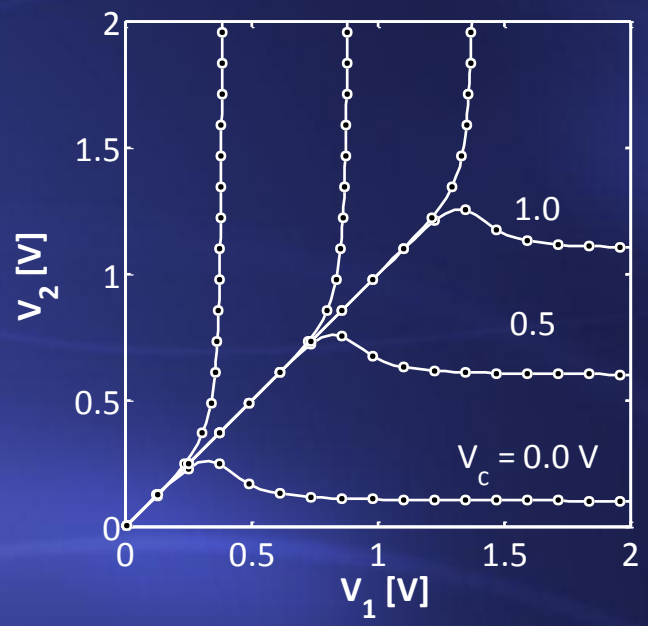
where, $$s = 1 + \frac{2r_2}{W\left[\frac{r_2 t_{si}}{2L_d}\exp\left(\frac{V_2 - V_c}{2\phi_t}\right)\right]}$$ $$r_j = C_{si}/C_{oxj}; \quad j = 1, 2$$

Solution Space Dependence on V_c, t_{ox} and t_{si}

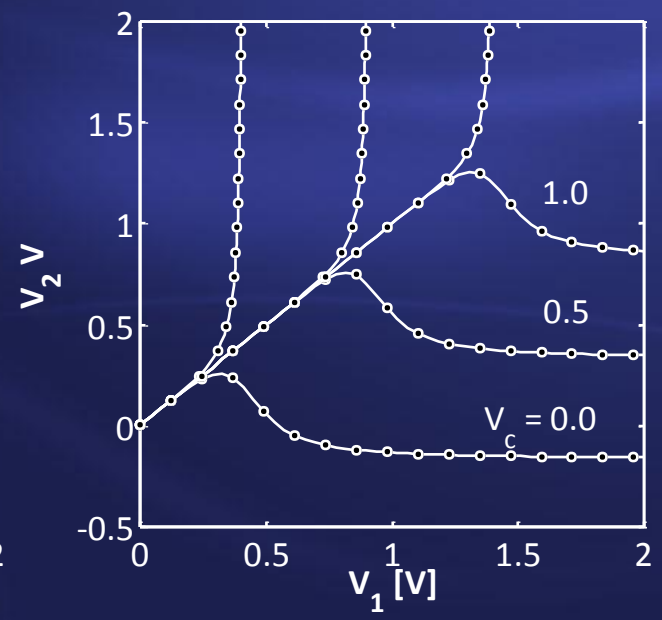
Circles: numerical solution
Lines: analytical solution



t_{si}=20nm, t_{ox1}=2 nm, t_{ox2}=2 nm.



t_{si}=20nm, t_{ox1}=2 nm, t_{ox2}=40 nm.



t_{si}=10nm, t_{ox1}=2 nm, t_{ox2}=40 nm.

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusions
- Related publications of the PSP group

Coupled Input Voltage Equations

- Two coupled IVEs for each solution type equation were derived by Prof. Taur's group

  [H. Lu and Y. Taur, TED,vol. 53, no. 5, p. 1161, 2006]

Trigonometric case:

$$\frac{V_1 - V_c}{2\phi_t} + \ln\left[\frac{t_{si}\sin(\alpha-\theta)}{4L_d\theta}\right] - 2r_1\theta\cot(\alpha-\theta) = 0$$

$$\frac{V_2 - V_c}{2\phi_t} + \ln\left[\frac{t_{si}\sin(\alpha+\theta)}{4L_d\theta}\right] + 2r_2\theta\cot(\alpha+\theta) = 0$$

Hyperbolic case:

$$\frac{V_1 - V_c}{2\phi_t} + \ln\left[\frac{t_{si}\sinh(\alpha_*-\sigma\theta_*)}{4L_d\theta_*}\right] - 2\sigma\theta_* r_1\coth(\alpha_*-\sigma\theta_*) = 0$$

$$\frac{V_2 - V_c}{2\phi_t} + \ln\left[\frac{t_{si}\sinh(\alpha_*+\sigma\theta_*)}{4L_d\theta_*}\right] + 2\sigma\theta_* r_2\coth(\alpha_*+\sigma\theta_*) = 0$$

- First one needs to determine the solution type from the terminal voltages
- Then IVEs are solved numerically for integration constants (θ, α) or (θ_*, α_*)
- Convergence is problematic (number of iterations increases drastically near the partition lines Γ_1, Γ_2)
- Convergence difficulty may manifest itself in the appearance of the fictitious imaginary roots

Single Input Voltage Equation

- Single IVE with one of the channel surface potential as unknown variable is proposed in [Sahoo and Mahapatra, TED, vol. 57, no. 3, p. 632 2010]. This is accomplished by an ingenious handling of the boundary conditions.
- For $V_1>V_2$ the IVE is formulated in terms of surface potential ψ_1 and for $V_2>V_1$ the IVE is formulated in terms of ψ_2.
- Step in the right direction. But: convergence is problematic, one needs optimization method to compensate for the poor initial condition guess. Computationally expensive and not quite suitable for compact modeling. Not tried in circuit simulations.
- Partition lines still need to be evaluated. The equations for the partition lines are equivalent to those in [Dessai and Gildenblat, SSE, vol. 54, no. 4, p. 382, 2010]
- In passing: an elegant system of three complex IVEs which have the same form regardless of the position in the solution space was recently derived in [Ortiz-Conde, SSE, 2010]. But three complex equations are like six real equations and Verilog-A/SPICE won't like this formulation. So, probably, compact modeling cannot be based on this approach. Also, the numerical difficulties are the same as before.

Modified Single Input Voltage Equation

[Dessai *et al.*, J. Comp. Electronics, 2010 (in press)]

By using the IVE from [Sahoo and Mahapatra, TED, vol. 57, no. 3, p. 632 2010] but changing the variable from surface potential to ξ we get better conditioned IVE (written here for $V_1 > V_2$)

$$\xi_1 = \beta^2 \left(C_{ox1}/C_f\right)^2 \left(V_1 - \psi_1\right)^2 \exp\left[\beta\left(V_c - \psi_1\right)\right] \quad (1)$$

Modified IVE for the hyperbolic case:

$$W\left(b_1\sqrt{\xi_1}\right)\left[1 + r\coth(\varphi_1)\sqrt{\frac{\xi_1 - 1}{\xi_1}}\right] + \ln\left[\frac{\sinh(\varphi_1)}{\sqrt{\xi_1 - 1}}\right] + \frac{\beta(V_2 - V_1)}{2} = 0$$

where $\varphi_1 = \sqrt{(\xi_1 - 1)/\xi_1} \cdot W\left(b_1\sqrt{\xi_1}\right)/r_1 + \sinh^{-1}\sqrt{\xi_1 - 1}$

and $b_1 = \left(C_f/2C_{ox1}\right)\exp\left[\beta\left(V_1 - V_c\right)/2\right]$

The idea: while all IVEs are mathematically equivalent, by using this form we can restrict the solution range since it becomes clear that $\xi_1 \geq 1$. This restriction helps to improve the robustness of the numerical algorithm. No such restriction was made available yet when one works with surface potentials directly. Of course, now one can obtain such restriction from (1) and apply this technique also to the original formulation in [Sahoo and Mahapatra, TED, vol. 57, no. 3, p. 632 2010].

Modified Single Input Voltage Equation

[Dessai *et al.*, J. Comp. Electronics, vol. 9, no. 3-4, pp. 103-107, 2010]

For trigonometric case we need further restrictions

$$W\left(b_1\sqrt{\xi_1}\right)\left[1+r\cot(\varphi_1)\sqrt{\frac{1-\xi_1}{\xi_1}}\right]+\ln\left[\frac{\sin(\varphi_1)}{\sqrt{1-\xi_1}}\right]+\frac{\beta(V_2-V_1)}{2}=0$$

$$\varphi_1=\sqrt{(1-\xi_1)/\xi_1}\cdot W\left(b_1\sqrt{\xi_1}\right)/r_1+\sin^{-1}\sqrt{1-\xi_1}$$

From the IVE it can be seen that $0 \le \xi_1 \le 1$

However, during numerical solution for some bias conditions ξ_1 can cause $\varphi_1 = \pi$ which creates a problem when evaluating $\cot(\varphi_1)$

To overcome this problem we select the initial range of ξ_1 to be between ξ_π and 1 where $\xi_\pi < 1$ is found from $\varphi_1(\xi_\pi) = \pi$

Relation of ξ_1 to ψ_1 , ψ_2 , α and θ

For $V_1 > V_2$ and hyperbolic case:

$$\psi_1 = V_1 - 2\phi_t W\left(b_1\sqrt{\xi_1}\right)$$

$$\psi_2 = \psi_1 - 2\phi_t \ln\left[\sinh(\varphi_1)/\sqrt{\xi_1 - 1}\right]$$

$$\theta_* = \sqrt{(\xi_1 - 1)/\xi_1} \cdot W\left(b_1\sqrt{\xi_1}\right)/2r_1$$

$$\alpha_* = \theta_* + \sinh^{-1}\sqrt{\xi_1 - 1}$$

For trigonometric case we replace ξ_1-1 by 1-ξ_1 and $\sinh^{-1}\sqrt{(\xi_1-1)}$ by $\sin^{-1}\sqrt{(1-\xi_1)}$

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusions
- Related publications of the PSP group

Effective Charge Density Concept

- Drift-diffusion current equation is written in a form reminiscent of the charge sheet approximation by defining effective charge density [Dessai *et al*., TED, vol. 57, no. 9, p. 2106, 2009]

$$I_d = \mu h_f \sum_{j=1}^{2} \left(\tilde{q}_{gj} \frac{d\psi_j}{dy} + \phi_t \frac{dq_{gj}}{dy} \right)$$

where q_{gj} and $\tilde{q}_{gj}$ are the gate charge density and effective gate charge density at gate *j* respectively

- No actual charge-sheet approximation is made
- The effective charge densities are (x_d can be selected as a matter of convenience and does not enter the equations of the model)

$$\tilde{q}_{g1} = \frac{q}{\frac{d\psi_1}{dy}} \int_{-t_{si}/2}^{x_d} n \frac{\partial \psi}{\partial y} dx + \epsilon_{si} E_x(x_d) \frac{dV_c}{d\psi_1} + \phi_t \epsilon_{si} \frac{dE_x(x_d)}{d\psi_1}$$

$$\tilde{q}_{g2} = \frac{q}{\frac{d\psi_2}{dy}} \int_{x_d}^{t_{si}/2} n \frac{\partial \psi}{\partial y} dx - \epsilon_{si} E_x(x_d) \frac{dV_c}{d\psi_2} - \phi_t \epsilon_{si} \frac{dE_x(x_d)}{d\psi_2}$$

- For a symmetric common gate DGFET this concept was introduced in [G. D. J. Smit *et al*. in Proc. NSTI-Nanotech, 2007] and developed in [Dessai *et al*., SSE, vol. 53, no. 4, p. 548, 2009] as a basis for an accurate charge model.

Effective Charge Density

For hyperbolic case:

$$q_{gj} = 4\phi_t C_{si} q_j$$

$$\tilde{q}_{gj} = q_{gj} + \phi_t C_{oxj}\left[1 - \frac{2\sigma_j(q_j^2 - n_j)(\alpha' - \sigma_j)}{q_j - \sigma_j n_j(\alpha' - \sigma_j)}\right]$$

where

$q_j = \sigma_j \theta \coth(\alpha - \sigma_j \theta)$ is the normalized gate charge density

$n_j = \theta^2 \mathrm{csch}^2(\alpha - \sigma_j \theta)$ is the normalized surface carrier concentration

$$\alpha' = \frac{r_1 n_1 - r_2 n_2 + r_1 q_1 - r_2 q_2 + (q_1 - q_2)/2}{(q_1 + q_2)/2 + r_1 n_1 + r_2 n_2}$$

$\sigma_j = \sigma$ for j=1 and $-\sigma$ for j=2 and σ = sgn (V_1-V_2)

For trigonometric case:

Replace hyperbolic functions by their trigonometric counterparts and set σ =1 irrespective of V_1 and V_2

Symmetric Charge Linearization

- Drain current: $I_d = \mu W \hat{q}_{g1} \frac{d\psi_1}{dy} = \mu W \hat{q}_{g2} \frac{d\psi_2}{dy}$

  where $\hat{q}_{gj} = (\tilde{q}_{gj} + \phi_t C_{oxj}) \frac{q_g}{q_{gj}}, \quad j = 1, 2$

- Linearizing w. r. t. ψ_j: $\hat{q}_{gj} = C_{oxj}(\nu_j - \alpha_j u_j)$

- ν_j is to be determined by requiring that I_d remains unchanged

$$\alpha_j = -\frac{\hat{q}_{gjd} - \hat{q}_{gjs}}{C_{oxj}\Delta\psi_j} \qquad u_j = \psi_j - \psi_{jm} \qquad \psi_{jm} = (\psi_{js} + \psi_{jd})/2$$

Then $I_d = \mu(W/L)C_{oxj}\nu_j\Delta\psi_j \qquad \Delta\psi_j = \psi_{jd} - \psi_{js}$

and $u_j(y)$ dependence becomes available: $\frac{dy}{du_j} = \frac{L(H_j - u_j)}{H_j \Delta\psi_j}; H_j = \frac{\nu_j}{\alpha_j}$

To determine ν_j set $I_d = I_d^{(exact)}$

Exact expression for I_d: [F. Liu *et al.*, TED, vol. 55, no. 3, p.816, 2008]

Charge Model

- Gate charge

$$Q_{Gj} = W \int_0^L q_{gj}\, dy = W \int_{u_{js}}^{u_{jd}} q_{gj} \frac{dy}{du_j}\, du_j$$

$$Q_{Gj} = WLC_{oxj}\left(V_{oxjm} + \frac{\Delta\psi_{sj}^2}{12H_j}\right)$$

- Drain charge

$$Q_D = -W \sum_{j=1}^{2} \int_0^L q_{gj} \frac{y}{L}\, dy$$

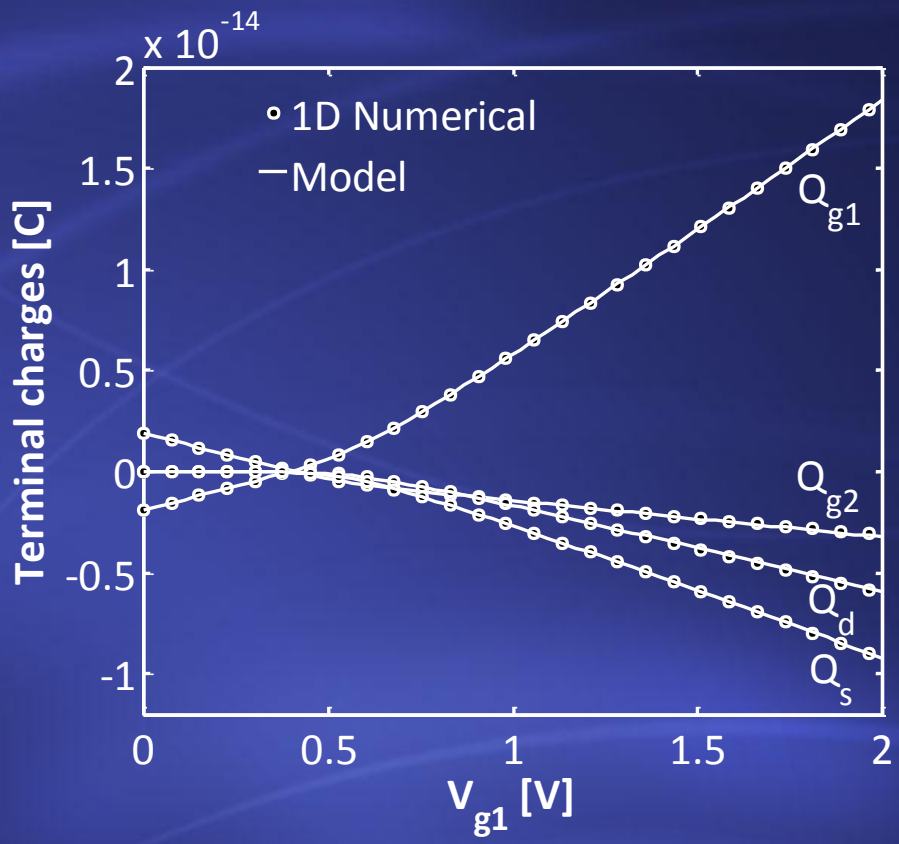
$$Q_D = -WL \sum_{j=1}^{2} C_{oxj}\left[\frac{V_{oxjm}}{2} - \frac{\Delta\psi_{sj}}{12}\left(1 - \frac{\Delta\psi_{sj}}{2H_j} - \frac{\Delta\psi_{sj}^2}{20H_j^2}\right)\right]$$

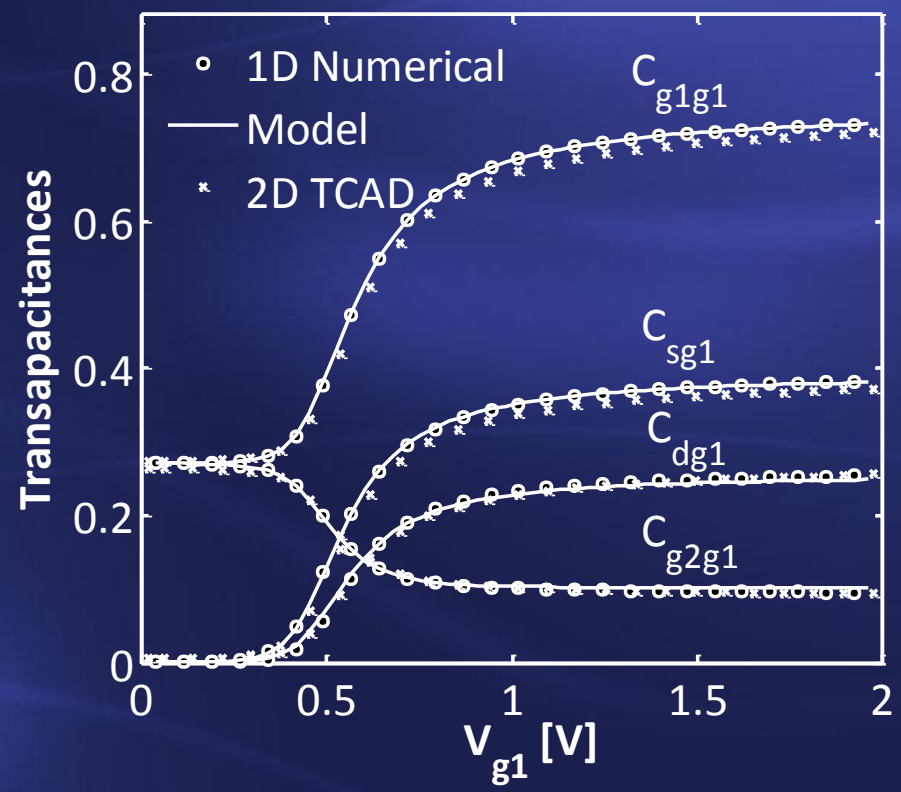
These equations include a symmetric common gate DGFET as a special case. They are, essentially the same as in SP or PSP models despite the fact that this time charge-sheet approximation is not used.

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusions
- Related publications of the PSP group

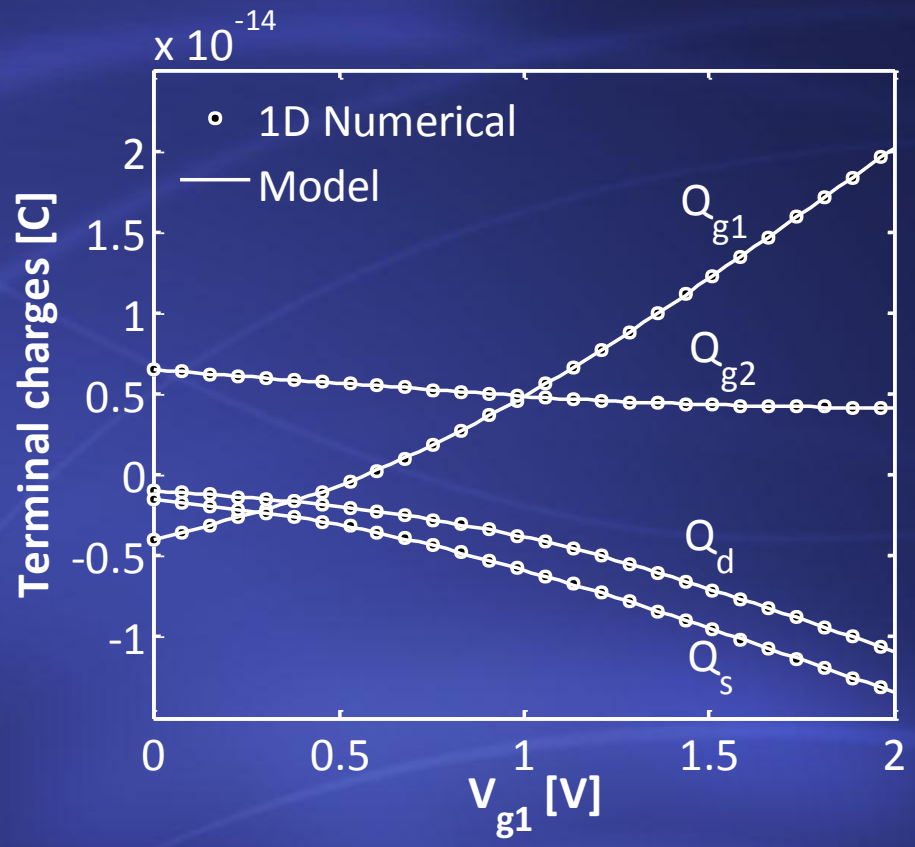
TCAD verification of the new Charge Model

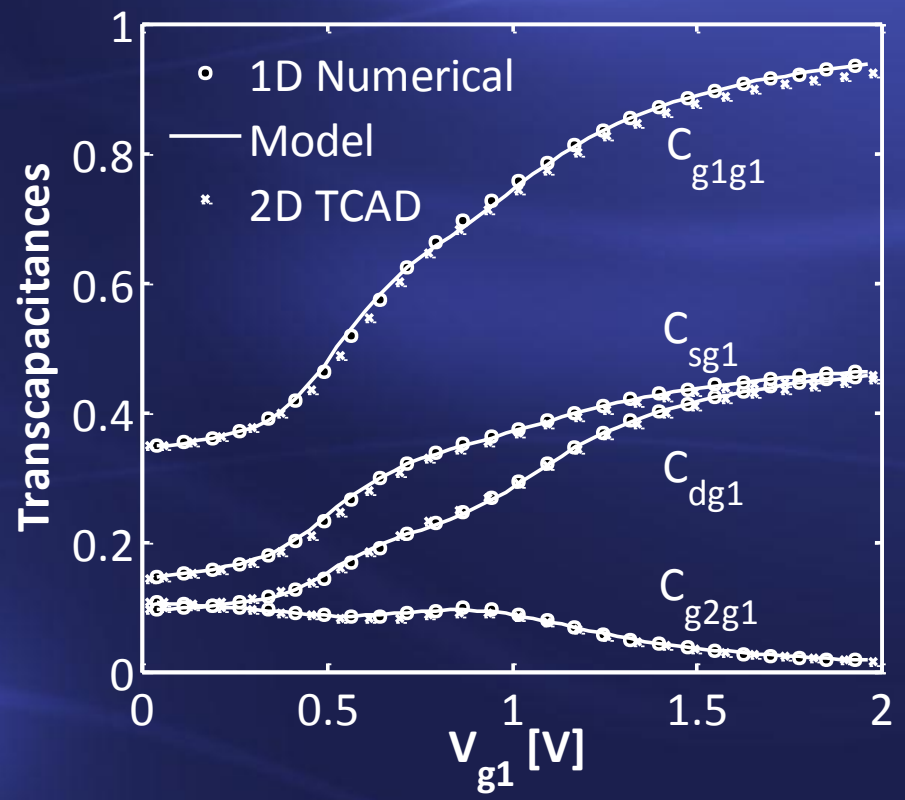




Channel 2 in weak inversion; t_{ox1} = 2nm, t_{ox2} = 2nm, t_{si} = 10 nm, V_{g2} = 0.4 V and V_d = 1.5 V

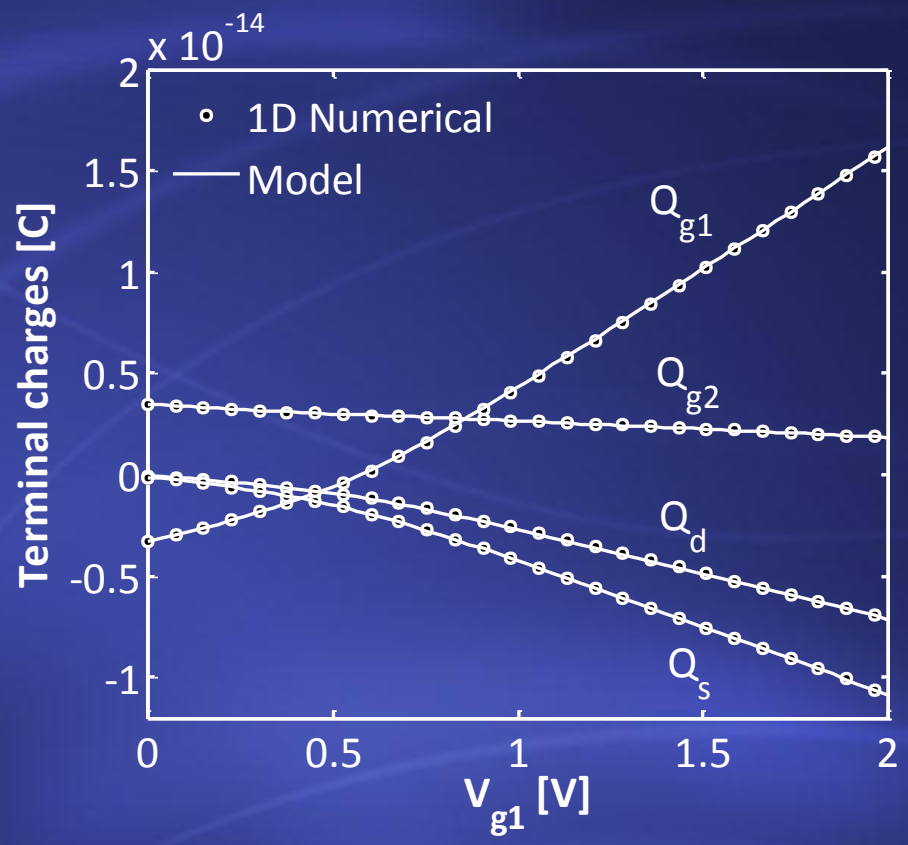
Charge Model Based on Symmetric Linearization Method

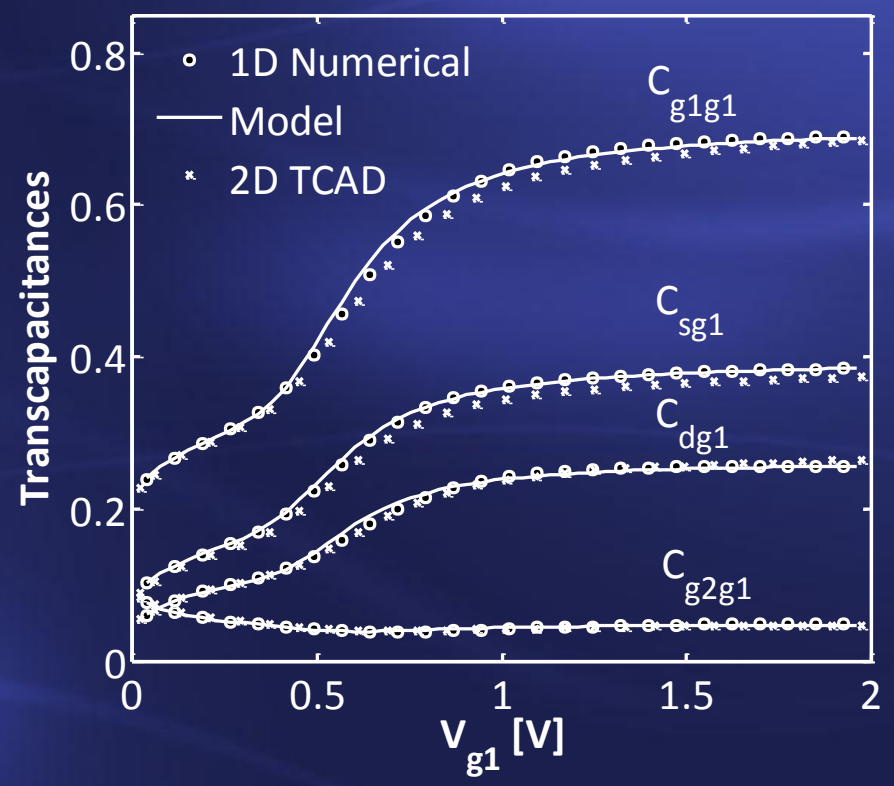




Channel 2 in strong inversion; t_{ox1} = 2nm, t_{ox2} = 2nm, t_{si} = 10 nm, V_{g2} = 1.0 V and V_d = 0.5 V

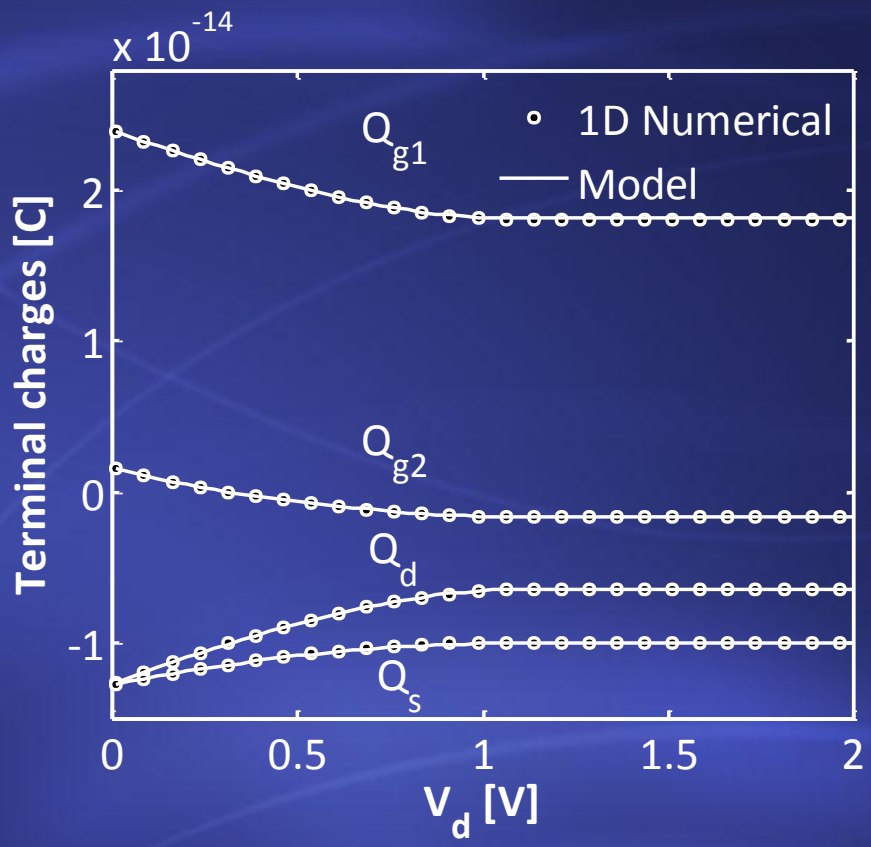
Charge Model Based on Symmetric Linearization Method

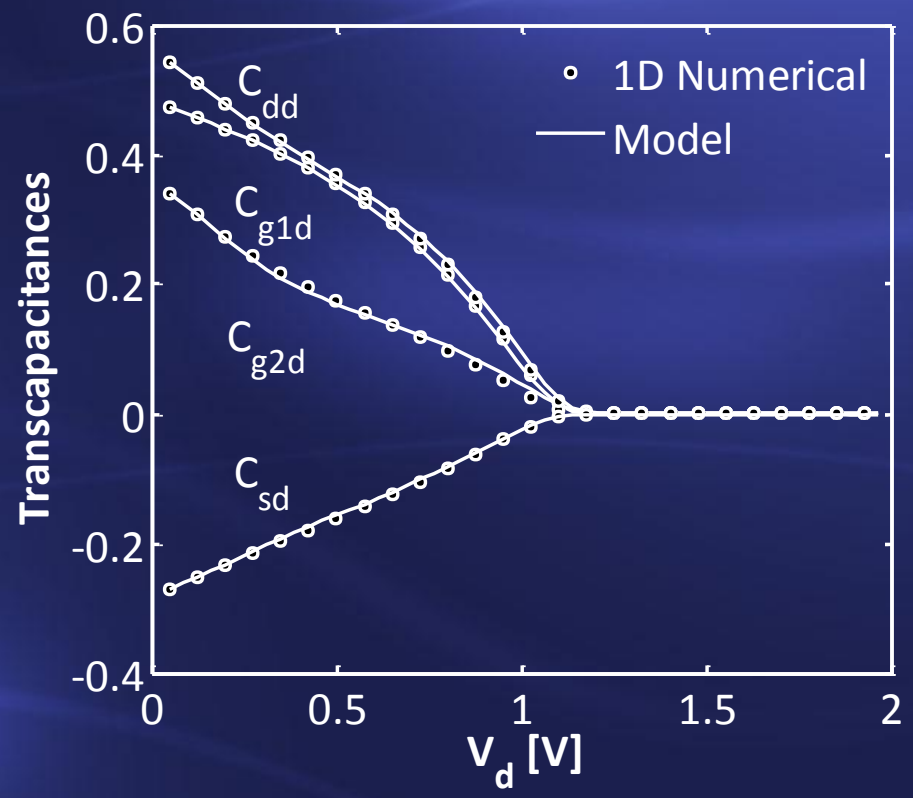




Asymmetric structure; t_{ox1} = 2nm, t_{ox2} = 10nm, t_{si} = 10 nm, V_{g2} = 1.5 V and V_d = 2.0 V

Charge Model Based on Symmetric Linearization Method





As a function of drain voltage; t_{ox1} = 2nm, t_{ox2} = 2nm, t_{si} = 10 nm, V_{g1} = 2.0 V and V_{g2} = 0.6 V

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusions
- Related publications of the PSP group

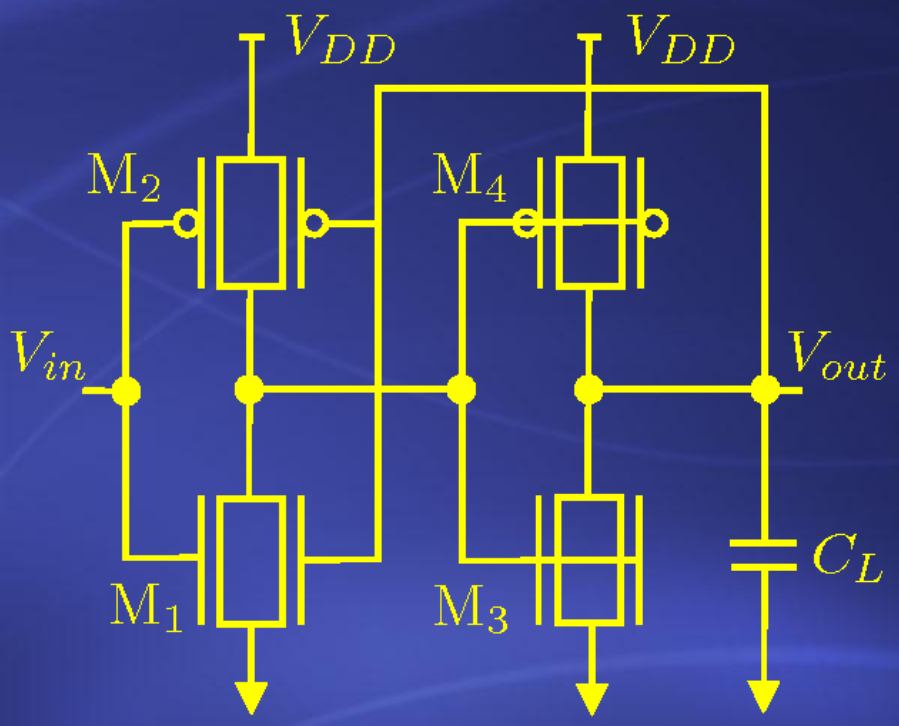
Model Implementation

- Use Verilog-A

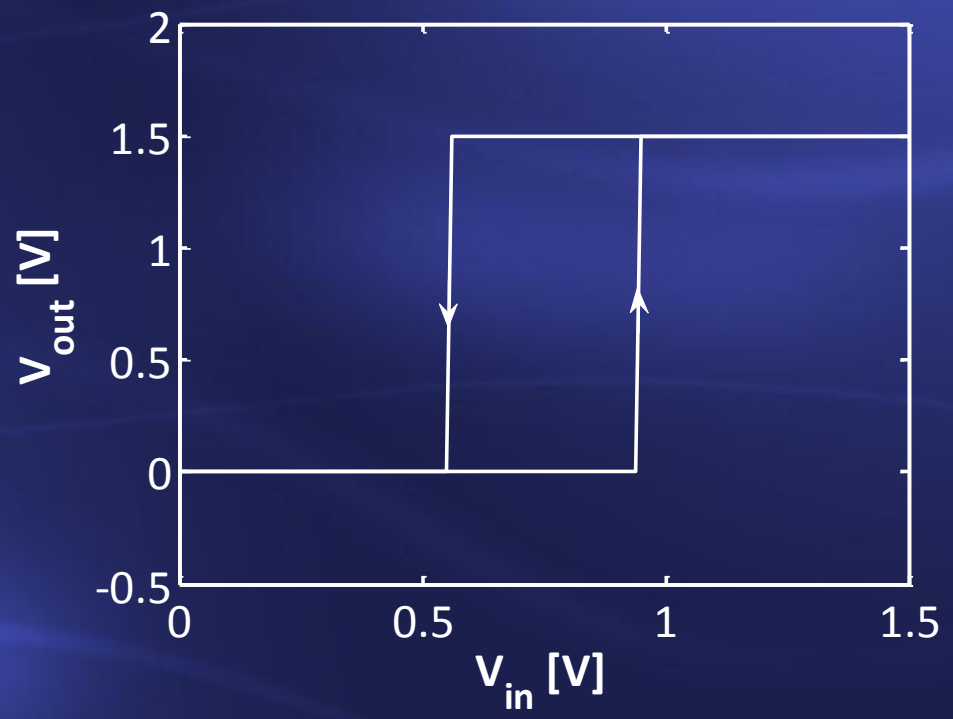
There is no good alternative to using high-level language: equations are complex, direct C-based implementation will almost certainly result in the erroneous handling of the derivatives. Verilog-A compilers are now available in common circuit simulators

- Convergence tests: RO's, Inverter trees (same as for PSP, PSP-SOI, PSP-HV)
- Simulations below include examples specific for DGFETs with independent gates: four transistor Schmitt trigger [Cakici *et al*. In Proc. IEEE Int. SOI Conf., 2003] and double balanced mixer [Zhang *et al*., TED, vol. 53, no. 10, p. 2198, 2005]. In these papers mixed mode TCAD (or conceptually similar) simulations were used. In what follows we use compact model in Verilog-A without any TCAD.

Simulation Example: Schmitt Trigger



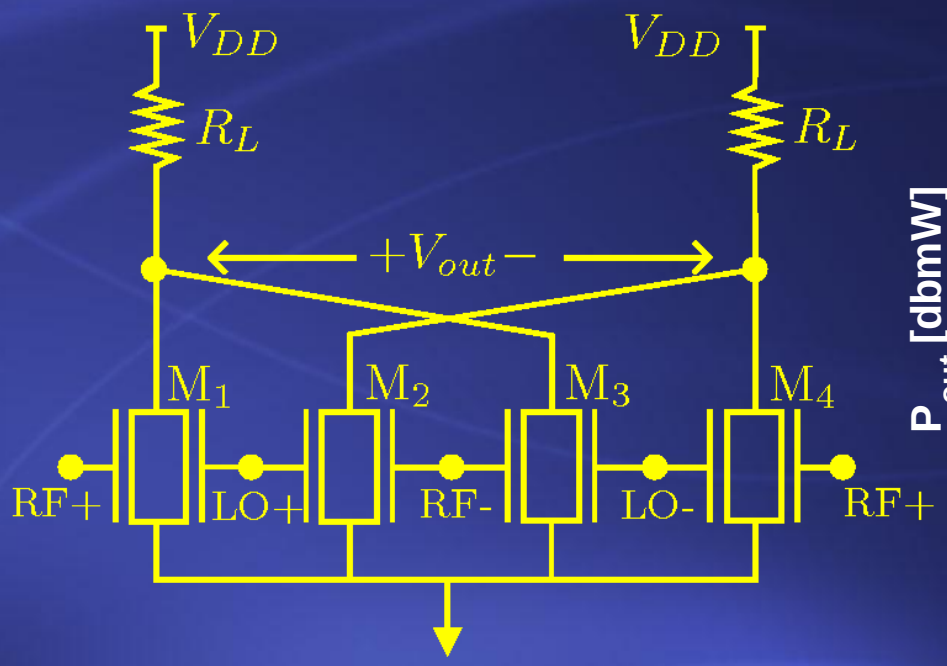
Four transistor Schmitt trigger



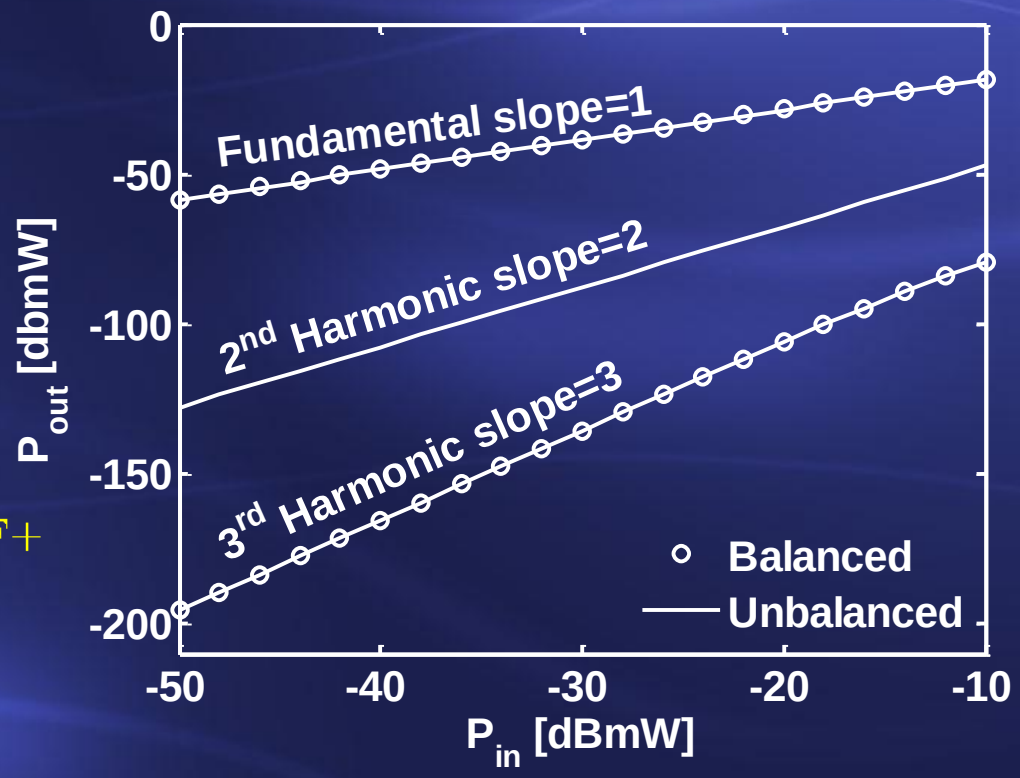
Transfer characteristics

Dynamic control of threshold voltage of M_1 and M_2 through feedback

Simulation Example: Double Balanced Mixer



Double balanced mixer



Harmonic balance simulation

Balanced: symmetric transistors
Unbalanced: asymmetric transistors

Outline

- Project Formulation
- Solution Space
- Input Voltage Equations
- Current and Charges
- TCAD Verification
- Model Implementation and Circuit Simulations
- Conclusions
- Related publications of the PSP group

Conclusions

- Recent progress in asymmetric DGFET theory enables a new compact model within the PSP context
- TCAD-based verification confirms the accuracy of the new approach
- Charge-sheet approximation is not used, there are no assumptions concerning the conduction state of any surface
- Handling the partition lines is the key aspect of any compact model of asymmetric DGFET: danger zone for the numerical solution of IVE(s)!
- New model is implemented in two standard circuit simulators. Circuit simulation examples illustrate the convergence of the model and the unique features of the asymmetric DGFET with independent gates

Acknowledgement

We are grateful to C.C. McAndrew of Freescale for his help with the model evaluation and implementation in circuit simulators.

PSP Group Publications on DGFET Modeling

1. G. D. J. Smit, A. J. Scholten, N. Serra, R. M. T. Pijper, R. van Langevelde, A. Mercha, G. Gildenblat, and D. B. M. Klaassen, "PSP based compact FinFET model describing dc and RF measurements," in *Tech. Dig. IEDM, 2006, pp. 175–178.*
2. G. D. J. Smit, A. J. Scholten, G. Curatola, R. van Langevelde, G. Gildenblat, and D. B. M. Klaassen, "PSP-based scalable compact FinFET model," in *NSTI-Nanotech, vol. 3, 2007, pp. 520–525.*
3. G. Dessai, A. Dey, G. Gildenblat, and G. D. J. Smit, "Symmetric linearization method for double-gate and surrounding-gate MOSFET models," *Solid-State Electron., vol. 53, no. 5, pp. 548–556, 2009.*
4. G. Dessai and G. Gildenblat, "Solution space for the independent-gate asymmetric DGFET," *Solid State Electron., vol. 54, no. 4, pp. 382–384,* Apr. 2010.
5. G. Dessai, W. Wu, and G. Gildenblat, "Compact charge model for independent-gate asymmetric DGFET," *IEEE Trans. Electron Devices,* vol. 57, no. 9, pp. 2106–2115, 2010.
6. G. Dessai, W. Wu, B. Bakkaloglu , C. C. McAndrew and G. Gildenblat, "Compact model and circuit simulations for asymmetric, independent gate FinFETs," *J. Computational Electronics*, vol. 9, no. 3-4, pp. 103-107, 2010.
7. A.J. Scholten, G.D.J. Smit, R.M.T. Pijper, L.F. Tiemeijer, A. Mercha and D.B.M. Klaassen. "FinFET compact modelling for analogue and RF applications", IEDM 2010.