

MOS-AK Meeting, ESSDERC-ESSCIRC 2013  
Bucharest, September 20, 2013

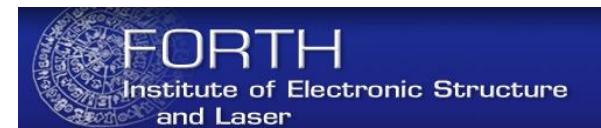
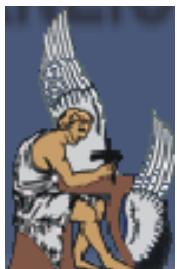
# TCAD assessment of gate-underlapped, Si and 4H-SiC, normally-on, vertical DG JFETs

Matthias Bucher, Rupendra Sharma

Technical University of Crete (TUC), 73100 Chania, Greece

Konstantinos Zekentes

Foundation for Research and Technology Hellas (FORTH), 70013 Heraklion, Greece



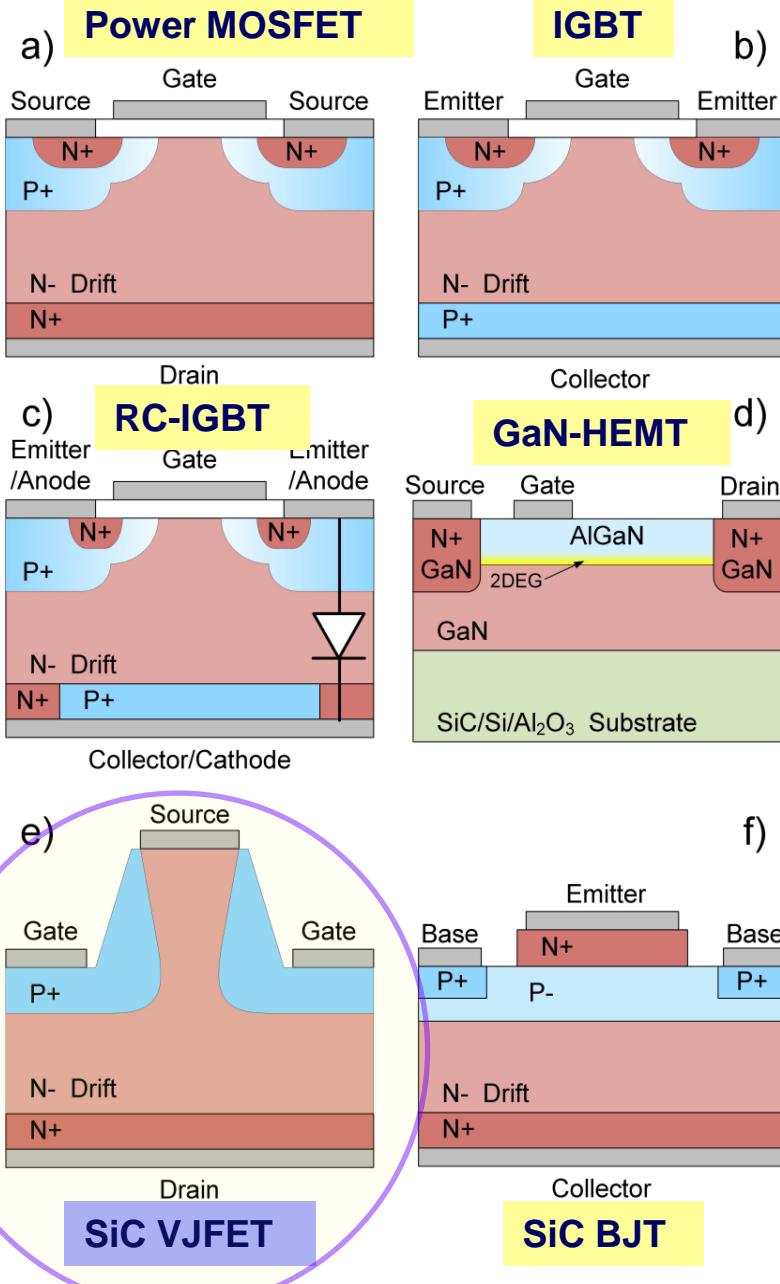
# Outline

- ❖ SiC based Power Devices
- ❖ Comparison of Silicon and Silicon Carbide Materials
- ❖ Physical structure of 4H-SiC VJFETs
- ❖ Optimization of the Structure
- ❖ Thermal Analysis
- ❖ Conclusions

# SiC based power devices

- ❖ SiC Power MOSFETs
- ❖ IGBTs
- ❖ GaN HEMTs
- ❖ SiC VJFETs
- ❖ SiC BJTs

- ❖ Goal of the project
  - ✓ Inverter for photovoltaic applications, using 4H-SiC JFETs
  - ✓ Development of compact model



# Silicon and 4H-Silicon Carbide

## ❖ 4H-SiC

- ✓ SiC bandgap is three times that of Si
  - Breakdown field (10 times greater than Si)
  - Thinner highly doped voltage-blocking layers
  - High-temperature applications possible >> 300°C
- ✓ 4H-SiC: mobility much higher than for 6H- or 3C-SiC
- ✓ Saturated electron velocity of 4H-SiC is twice that of Si

## ❖ Si

- Higher mobility than 4H-SiC
- Higher switching speed
- Low cost, ease of fabrication

Comparison of SiC with other Semiconductor Materials

| Property  | 6H SiC | 4H SiC | 3C SiC | GaAs | Si   |
|---|--------|--------|--------|------|------|
| Wide Energy Bandgap (eV)  | 2.9    | 3.26   | 2.2    | 1.43 | 1.12 |
| Electric Field Breakdown ( $\diamond 10^6$ V/cm @ 1000V operation)            | 2.5    | 2.2    | 2.0    | 0.30 | 0.25 |
| Thermal Conductivity (W/cm $\ddot{\epsilon}$ @ Room T)                        | 4.9    | 4.8    | 4.9    | 0.5  | 1.5  |
| Saturated Electron Drift ( $\diamond 10^7$ cm/s @ $E > 2 \diamond 10^5$ V/cm) | 2.0    | 2.0    | 2.5    | 1.0  | 1.0  |

# TCAD simulation – mobility parameters

## ❖ Caughey-Thomas mobility model

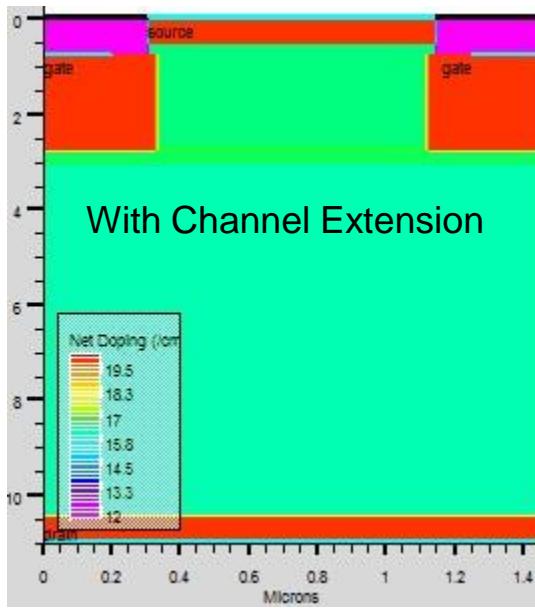
$$\mu_{n0} = \text{MU1N.CAUG} \cdot \left( \frac{T_L}{300K} \right)^{\text{ALPHAN.CAUG}}$$

$$+ \frac{\text{MU2N.CAUG} \cdot \left( \frac{T_L}{300K} \right)^{\text{BETAN.CAUG}} - \text{MU1N.CAUG} \cdot \left( \frac{T_L}{300K} \right)^{\text{ALPHAN.CAUG}}}{1 + \left( \frac{T_L}{300K} \right)^{\text{GAMMAN.CAUG}} \cdot \left( \frac{N}{\text{NCRITN.CAUG}} \right)^{\text{DELTAN.CAUG}}}$$

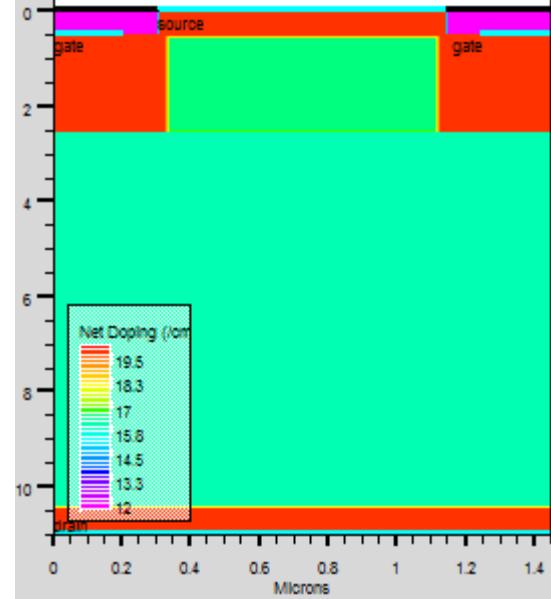
| Parameter | Unit                | Si                    | *4H-SiC            |
|-----------|---------------------|-----------------------|--------------------|
| MU1N      | cm <sup>2</sup> /Vs | 55.2                  | 40                 |
| MU2N      | cm <sup>2</sup> /Vs | 1429                  | 950                |
| NCRITN    | cm <sup>-3</sup>    | 9.68×10 <sup>16</sup> | 2×10 <sup>17</sup> |
| ALPHAN    | -                   | 0                     | -0.5               |
| BETAN     | -                   | -2.3                  | -2.4               |
| GAMMAN    | -                   | -3.8                  | 0.0                |
| DELTAN    | -                   | 0.73                  | 0.76               |

\* Roschke, Schwierz, IEEE TED 48(7), 2001

# VJFETs with and without channel extension



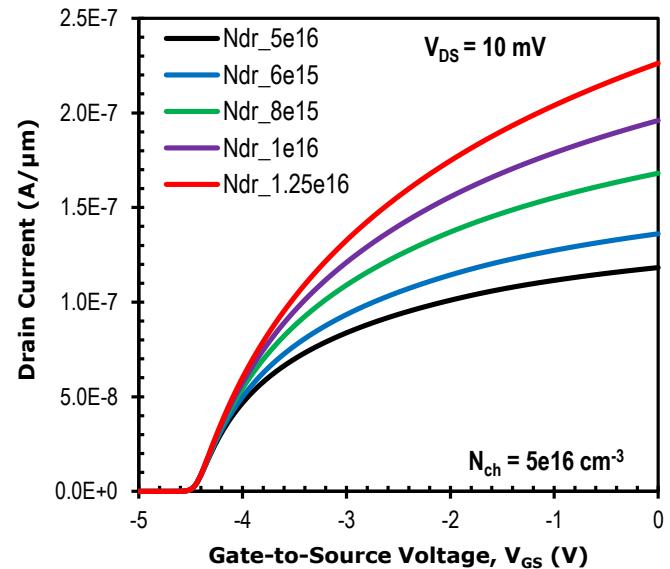
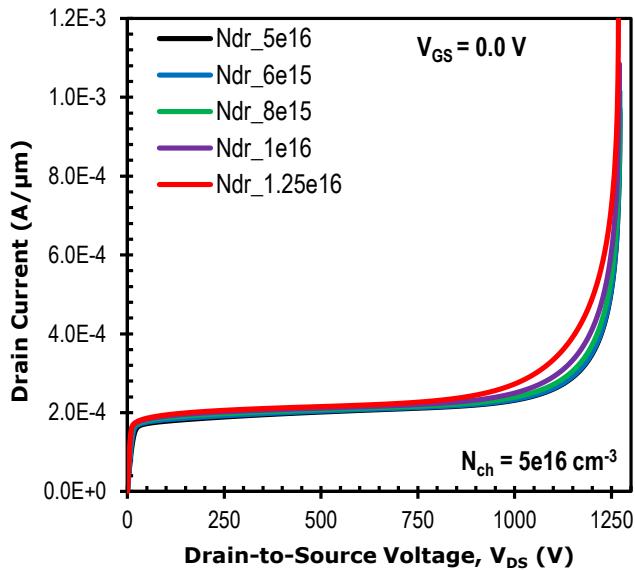
- ❖ Normally-on VJFET **with** channel extension
  - ✓  $V_T$  depends on doping of channel & dimensions
  - ✓  $V_T$  less sensitive to drift region doping
  - ✓ Better performance (Ron vs. Breakdown voltage)



- ❖ Normally-on VJFET **without** channel extension
  - ✓  $V_T$  depends on doping of channel, drift region & dimensions
  - ✓ Highly sensitive to drift region doping
- ❖ Channel extension VJFET is desirable

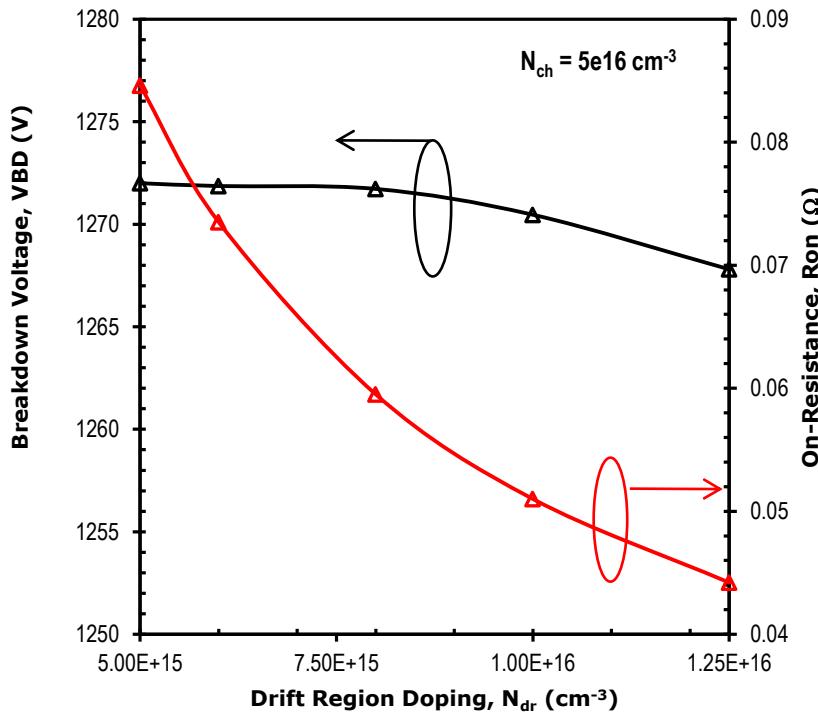
# Optimization of channel extension vertical DG JFET structure

- ❖ Normally-on VJFET with channel extension
  - ✓  $V_T$  not sensitive to drift region doping ( $N_{dr}$ )
  - ✓ Increase in drain current with increase of drift region doping



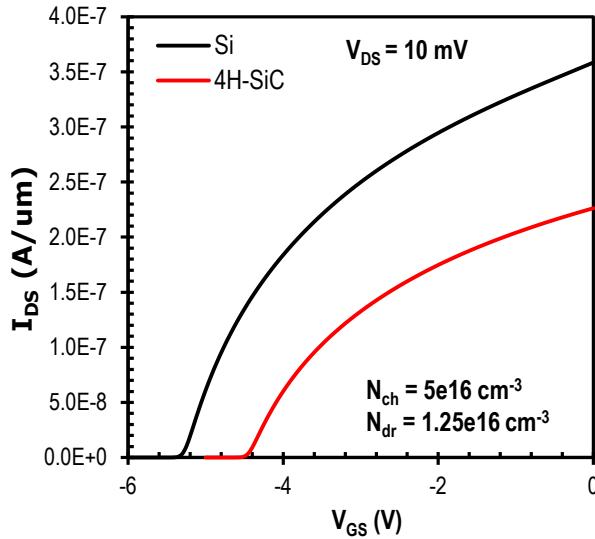
- ✓ Blocking voltage: slightly changes with  $N_{dr}$

# Optimization (breakdown vs. on-resistance)

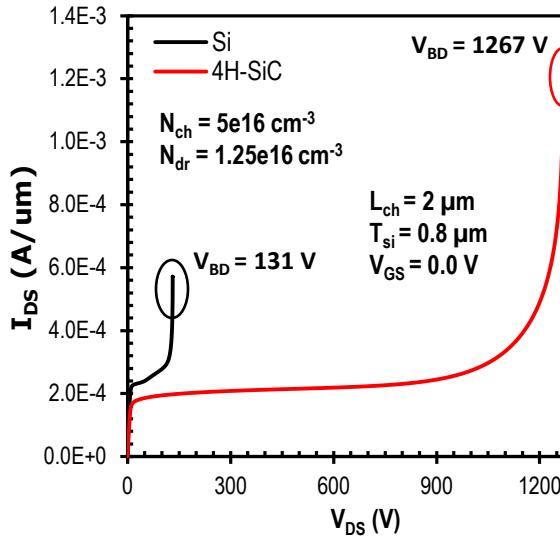


- ❖ Normally-on VJFET with channel extension
  - ✓ Improved on-resistance ( $R_{on}$ ) with higher  $N_{dr}$
  - ✓ Almost same breakdown voltage

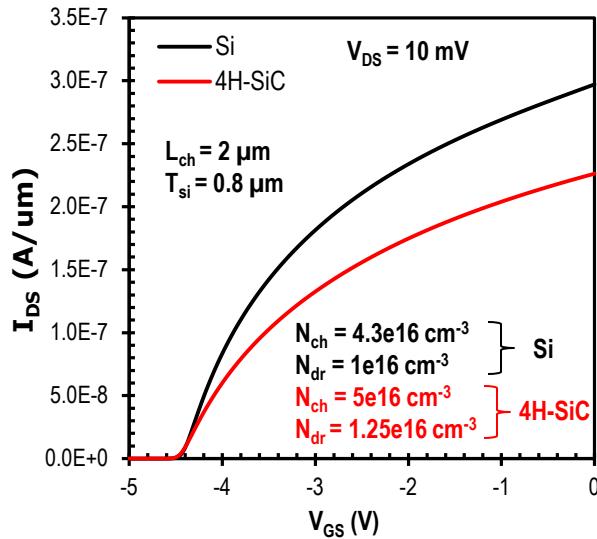
# Comparison: Si and 4H-SiC vertical JFET



- ❖ Si and 4H-SiC (same physical parameters)
  - ✓  $V_T$  difference  $\sim 1.0 \text{ V}$
  - ✓ Breakdown field for 4H-SiC ( $\sim 10$  times greater than Si)

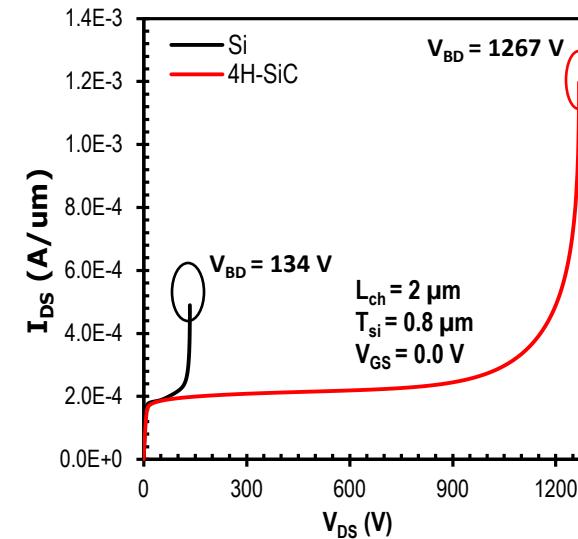


# Comparison: Si and 4H-SiC vertical JFET



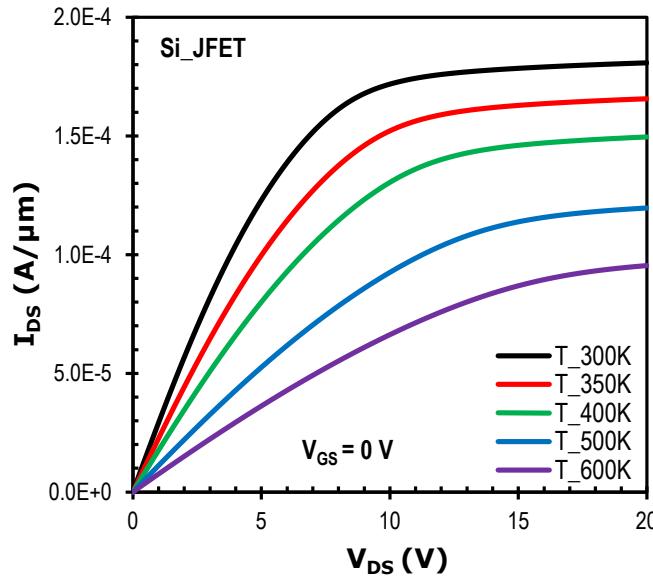
## ❖ Si and 4H-SiC

- ✓ Optimize channel doping of Si JFET for similar  $V_T$
- ✓ Maintaining the ratio of channel doping ( $N_{ch}$ ) to drift region doping ( $N_{dr}$ )



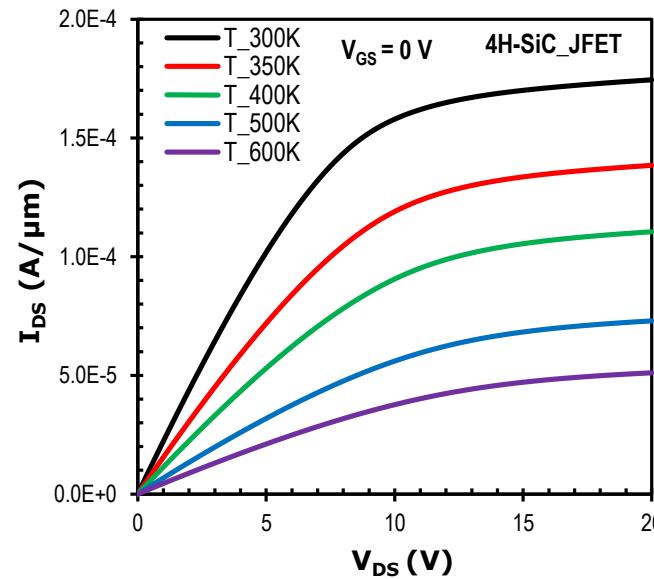
- ❖ 30 % higher drain current for Si JFET (higher mobility)

# Thermal analysis

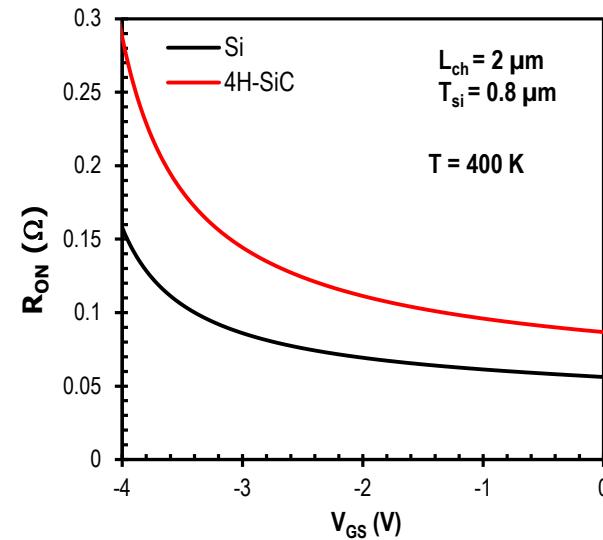
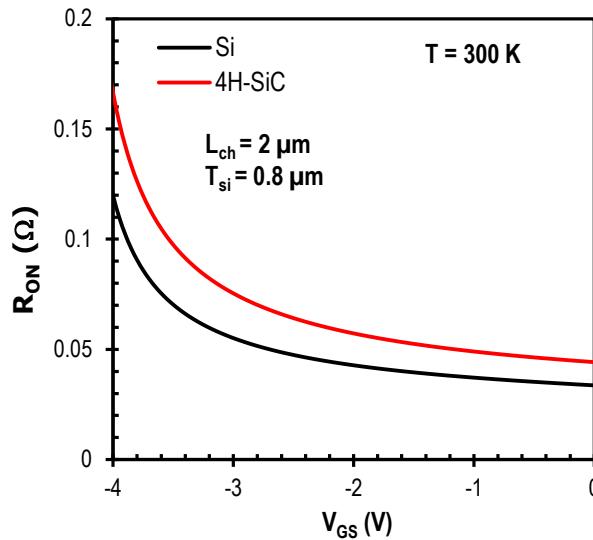


## ❖ Si and 4H-SiC vertical JFET

- ✓ Higher drain current for Si JFET
- ✓ Drain current decreases slightly more for 4H-SiC with temperature

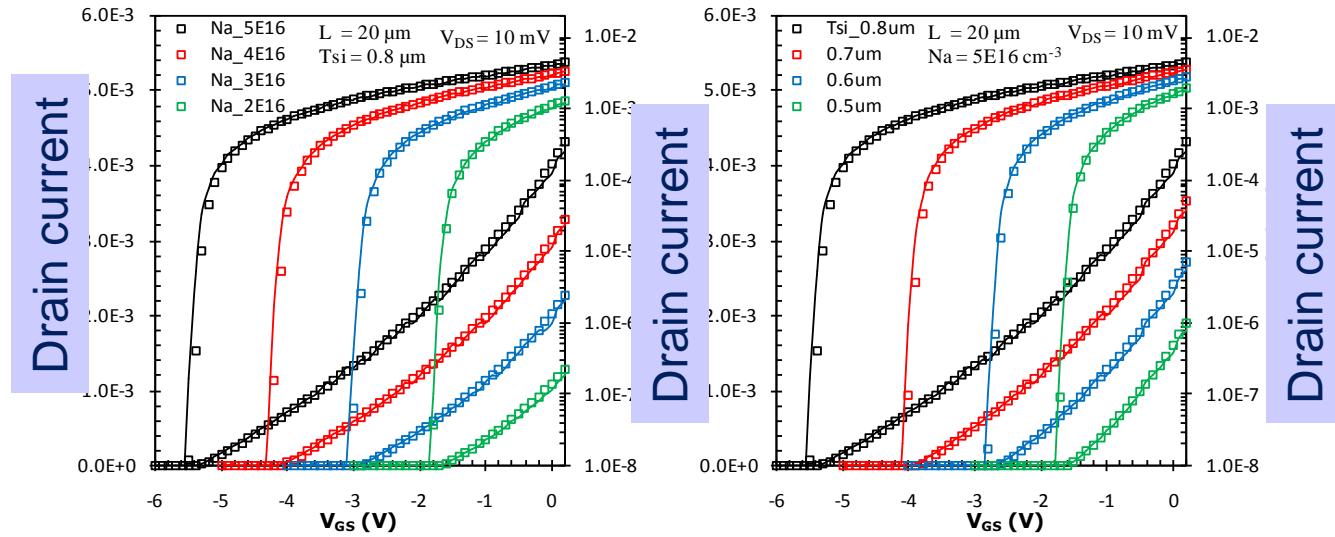


# Thermal analysis



- ❖ Si and 4H-SiC vertical JFET
  - ✓ Lower  $R_{on}$  for Si JFET
  - ✓  $R_{on}$  increases with increasing temperature
  - ✓ The increase in  $R_{on}$  with increasing temperature is less for Si JFET

# Outlook: compact model development



- ❖ First JFET charge-based model presented at MOS-AK 9/2012
- ❖ New model development underway
- ❖ Full charge-based intrinsic model for channel region
- ❖ Short-channel effects, scalability
- ❖ Drift extension modelling

# Conclusions

## ❖ Optimization

- ✓ Channel extension JFET is desirable for better on-resistance vs. breakdown voltage
- ✓ Channel extension JFET, less sensitive for drift region doping.
- ✓ Ratio of channel doping-to-drift region doping is very important.

## ❖ TCAD based analysis, Si vs. 4H-SiC JFET

- ✓ 4H-SiC JFET – good for very high voltage, high power applications
- ✓ Si JFET – performs better up to 150 V applications
- ✓ Si JFET - less sensitive to temperature

## ❖ Full scalable compact model for power JFETs underway.

# Acknowledgments



Ε. Π. Ανταγωνιστικότητα και Επιχειρηματικότητα (ΕΠΑΝ II), ΠΕΠ Μακεδονίας – Θράκης, ΠΕΠ Κρήτης και Νήσων Αιγαίου, ΠΕΠ Θεσσαλίας – Στερεάς Ελλάδας – Ηπείρου, ΠΕΠ Αττικής

- Cooperation project “ANTI-SiC” (09ΣΥΝ-32-1181)

This work was co-financed by Hellenic Funds and the European Regional Development Fund (ERDF), under the Hellenic National Strategic Reference Framework (NSRF) 2007-2013.

- Contact:

Prof. Matthias Bucher  
ECE Dept., Electronics Laboratory  
Technical University of Crete (TUC), 73100 Chania, Crete, Greece  
phone: +30 28210 37210  
bucher@electronics.tuc.gr, <http://www.electronics.tuc.gr>

