KU LEUVEN

BRUGES
9-12 SEPTEMBER
ESSERC 2024

micas
KU LEUVEN

Are open source digital design flows ready for mainstream?

ETH zürich

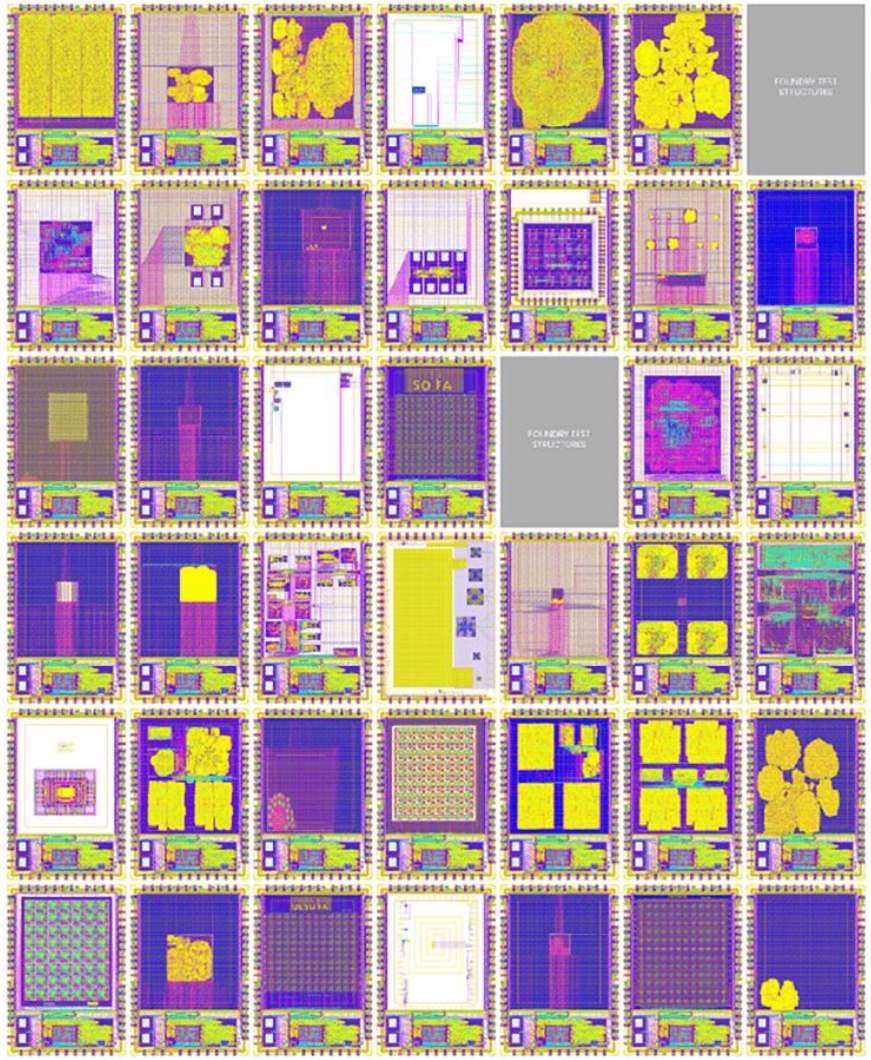
PULP
Parallel Ultra Low Power

Frank K. Gürkaynak
Microelectronics Design Center
ETH Zürich, SWITZERLAND
kgf@iis.ee.ethz.ch

IEEE SSCS Electron Devices Society CAS

Open Source HW is already a success

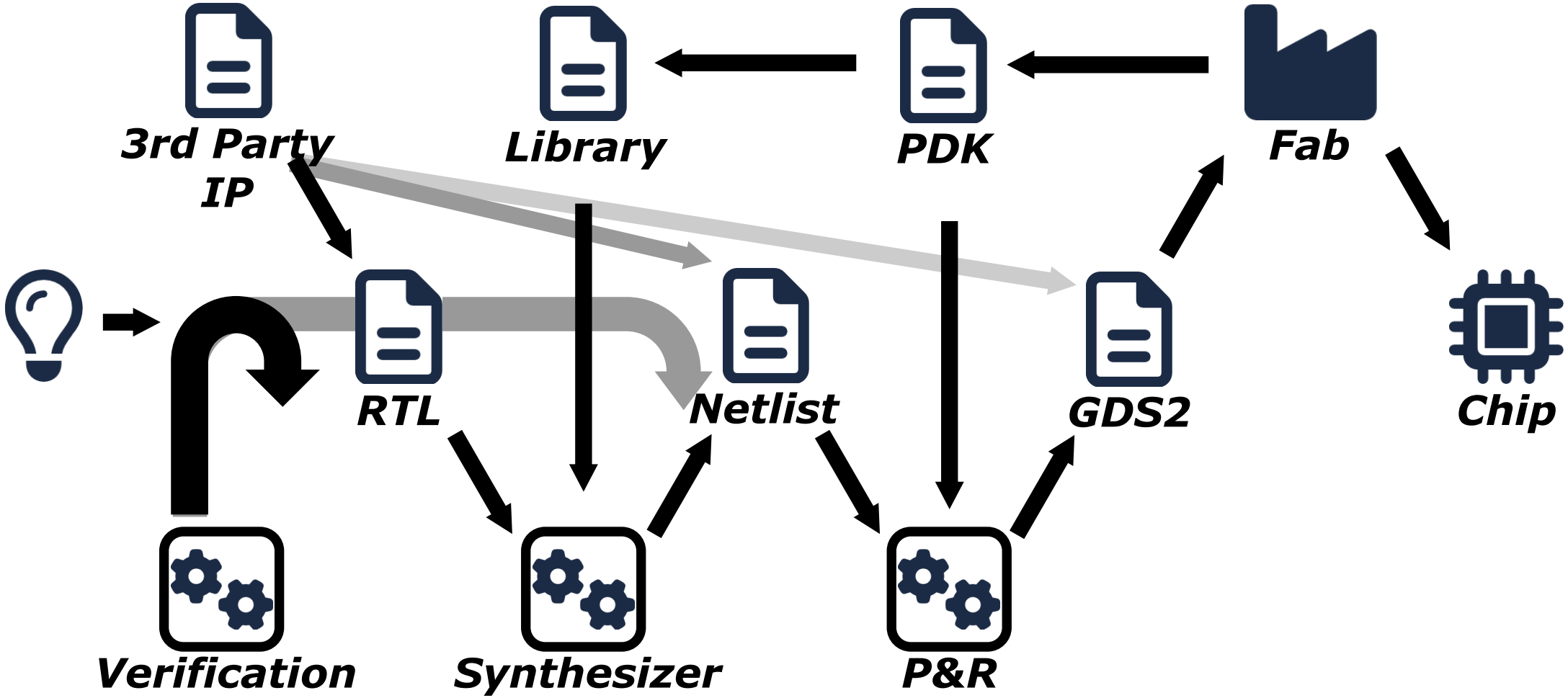
- Project supported by Google with Skywater
  - Resulted in hundreds of tape-outs
  - Reached to thousands of people
- Tiny TapeOuts add 100s of projects onto one tile of the Skywater modules
  - 238 chips on Tiny Tapeout 6
    - https://tinytapeout.com/runs/tt06/
- Complexity is limited
  - Excellent for teaching
  - But can it be used for more
  - How far can we push it?



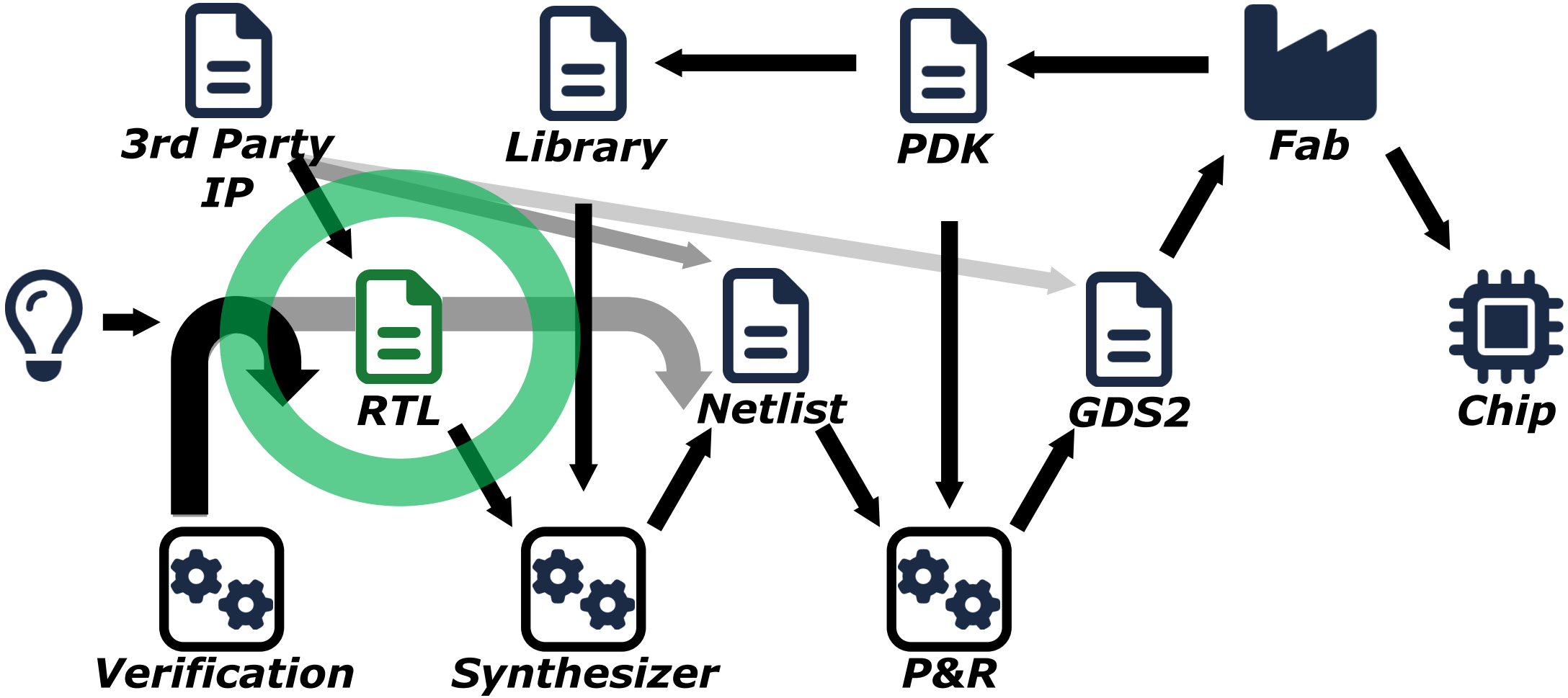
Say Hi to Basilisk!

- Completely open SoC design
  - **3.5x** timing &
    1.6x area improvement
    over existing open flows
  - Approaching QoR of commercial EDA
  - Complex design done in 6 months
- Key Metrics:
  - IHP's open 130nm node
  - 60 MHz TT backend (51 logic levels)
  - 1.08 MGE logic, 60% density
  - 24 SRAM macros (114 KiB)
  - 6.25 x 5.5mm (34mm²)

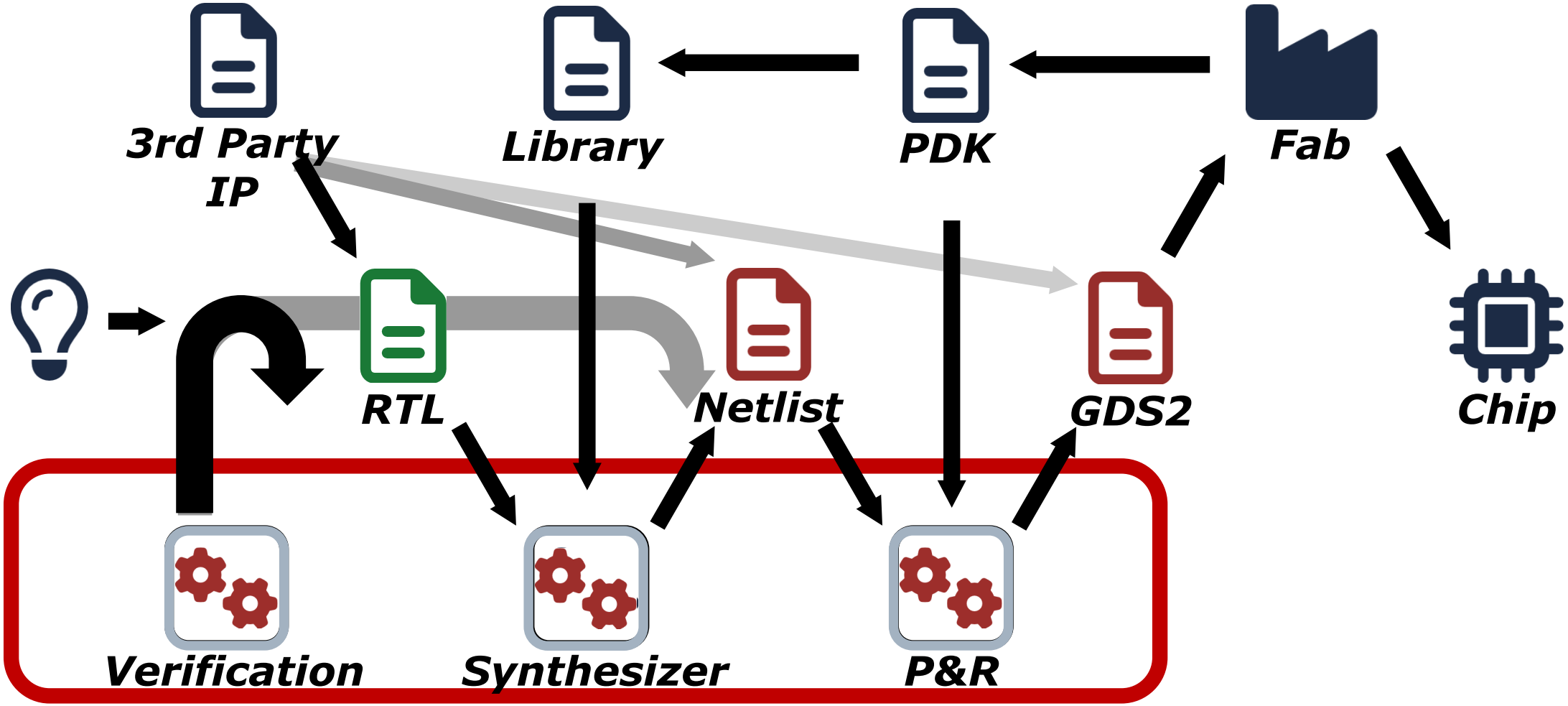
Simplified IC design flow



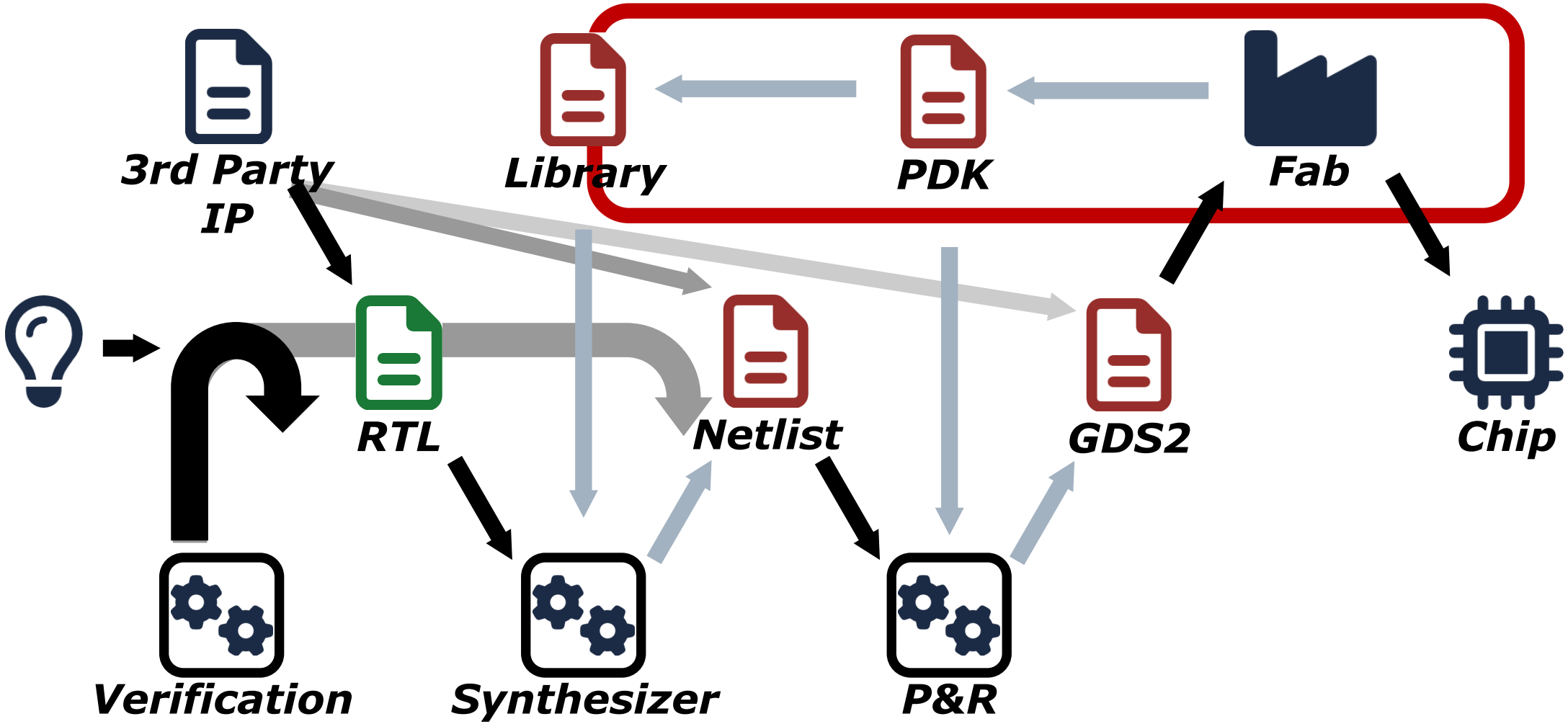
At the moment only RTL is open



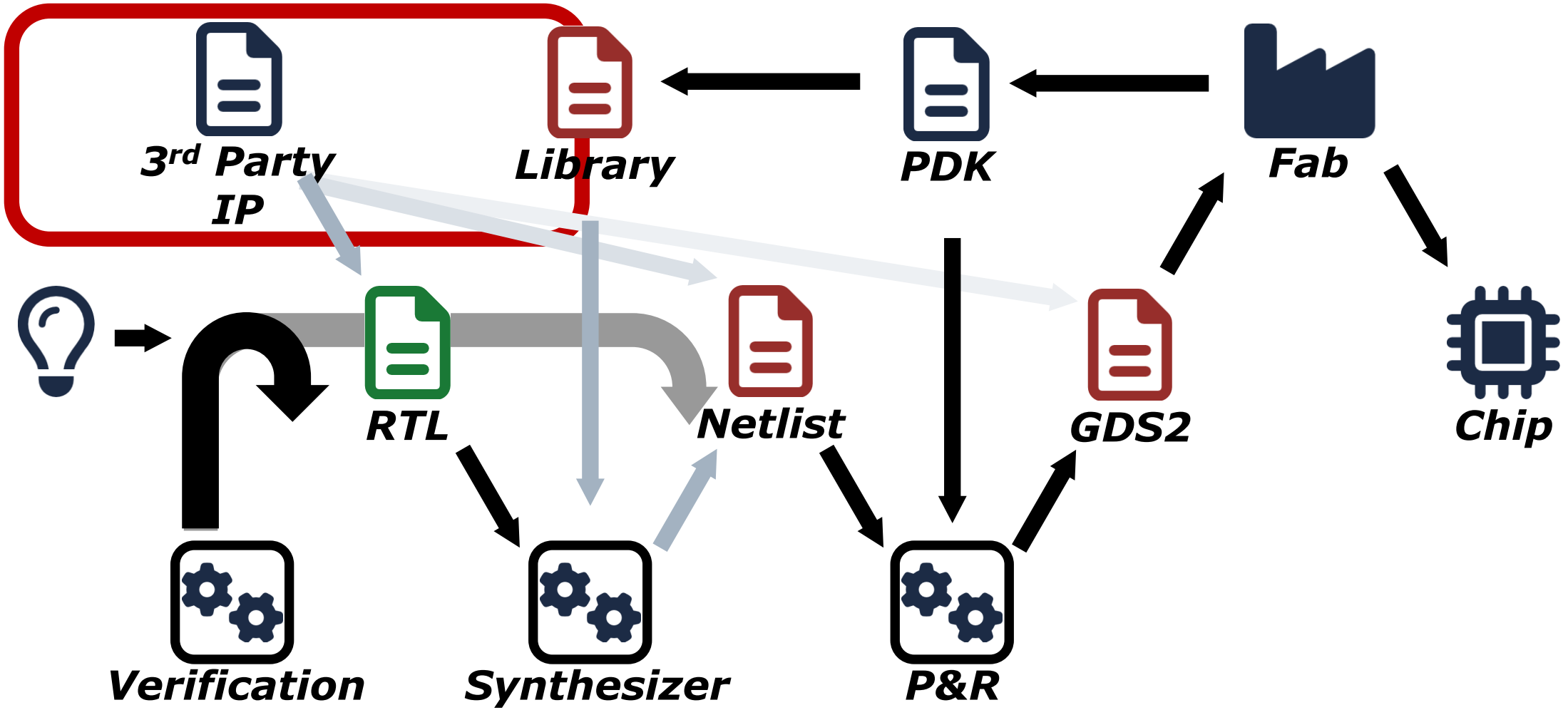
EDA vendors limit the output



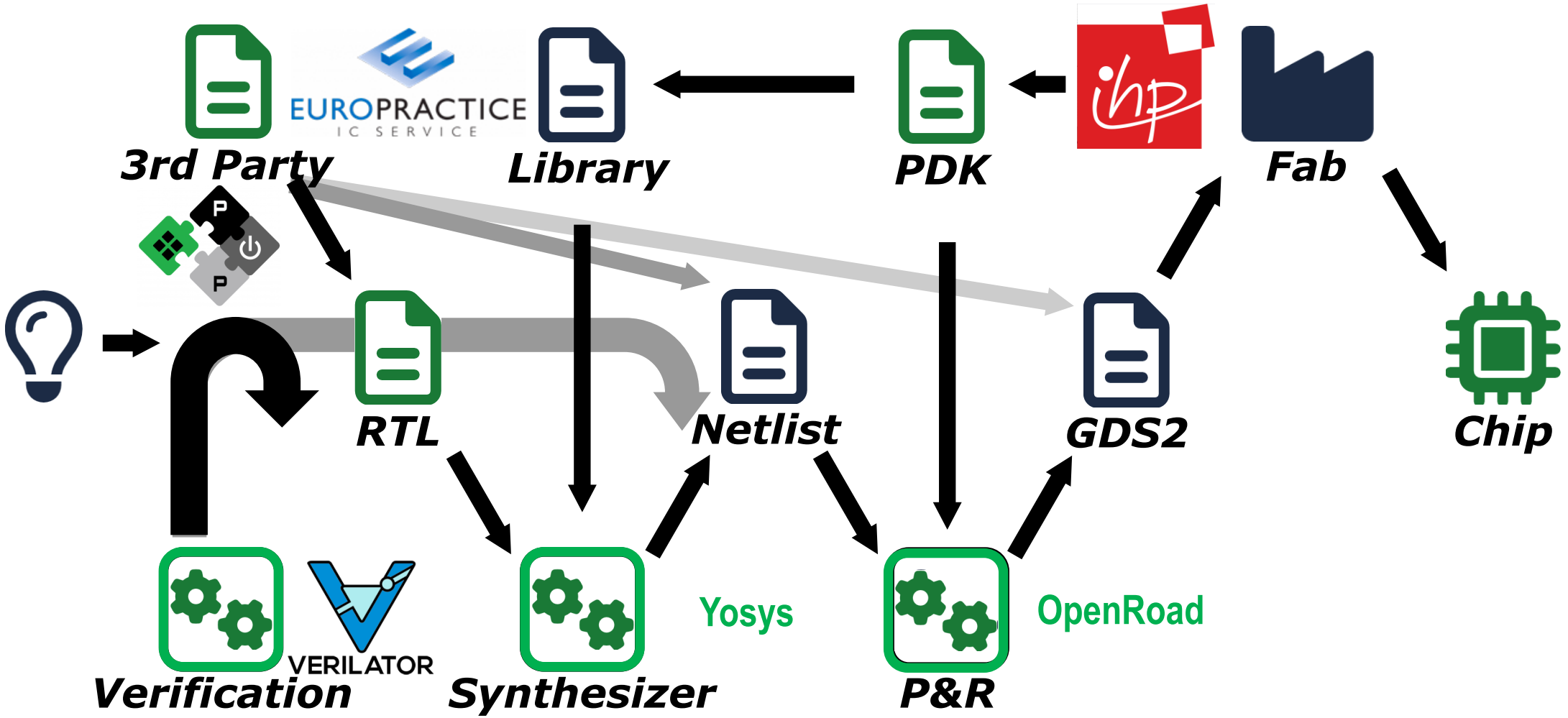
Fabs do not disclose PDK information



3rd party IP can limit open sourcing

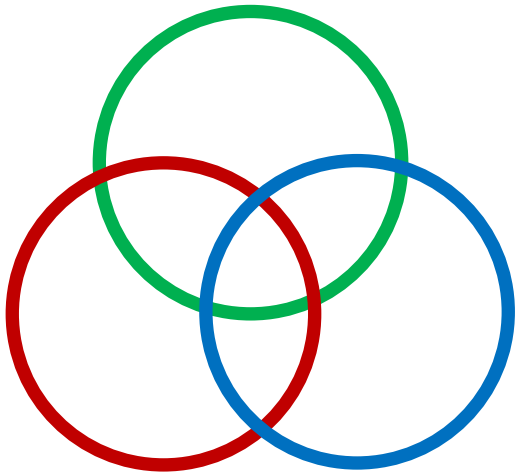


The road to opennes is here

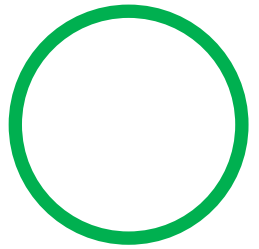


Three aspects of open source HW

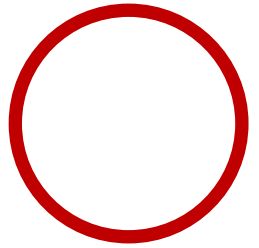
- **Design**
  - RTL / HDL descriptions (quite common)
  - Schematics / Physical Design (may have dependencies to technology information)
- **Tools** (EDA)
  - Front-end tools (Synthesis)
  - Back-end tools (Placement and Routing)
  - Verification tools (Simulation)
- **Manufacturing** (PDK)
  - Design rules for manufacturing (separation, minimum width of metals)
  - Layer stack informartion for parasitics (thickness, dielectric constants..)
  - Device models (SPICE parameters) for simulation



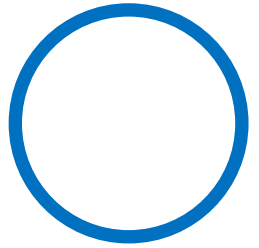
Three aspects are largely independent



- Open source contributions can use commercial EDA and closed PDKs
  - PULP Team has been working on open source HW design for 10+ years



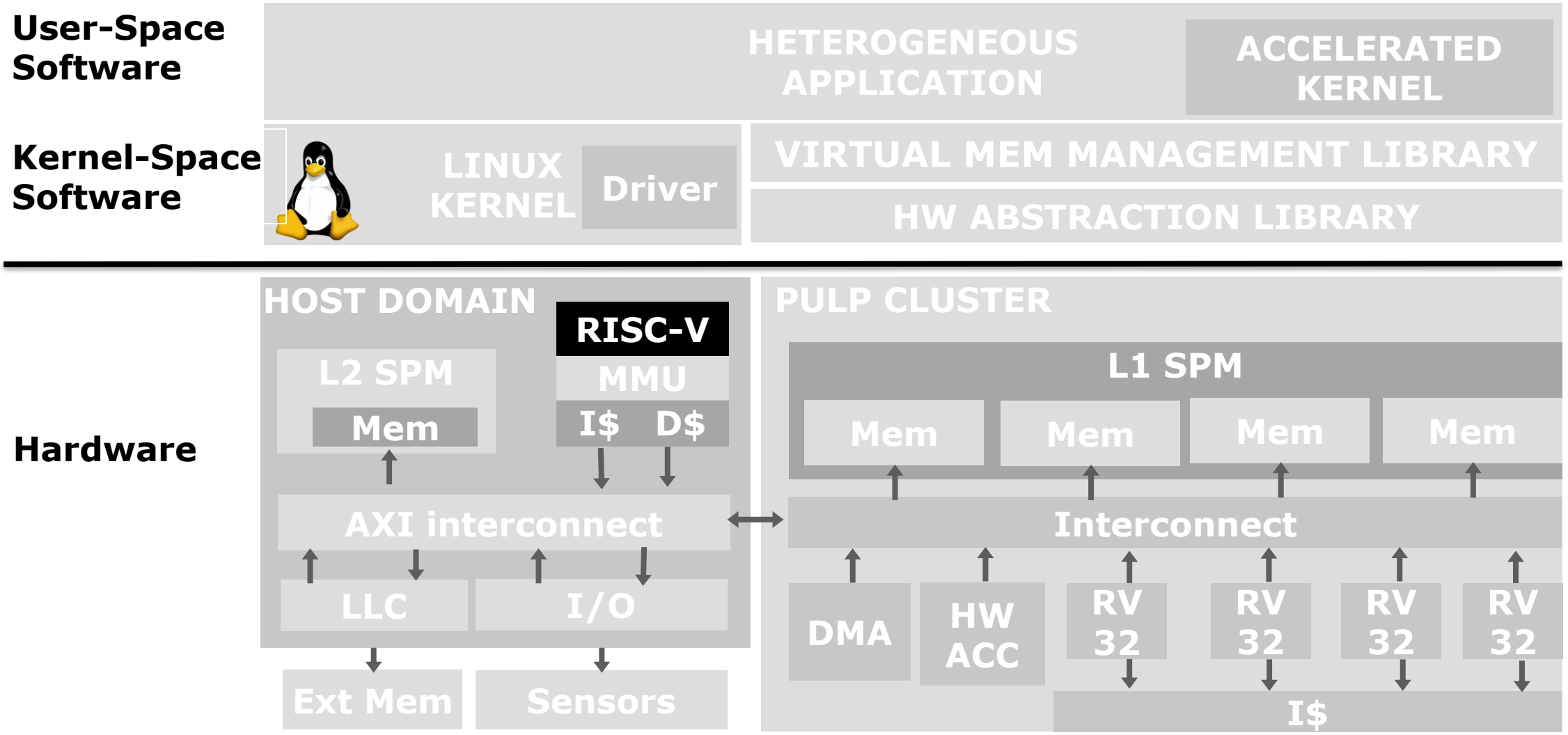
- Open source EDA tools work just as well on closed PDKs
  - The tools are actually agnostic to the process technology (or the design)
  - Access to the technology files makes adaptations to the flow is possible



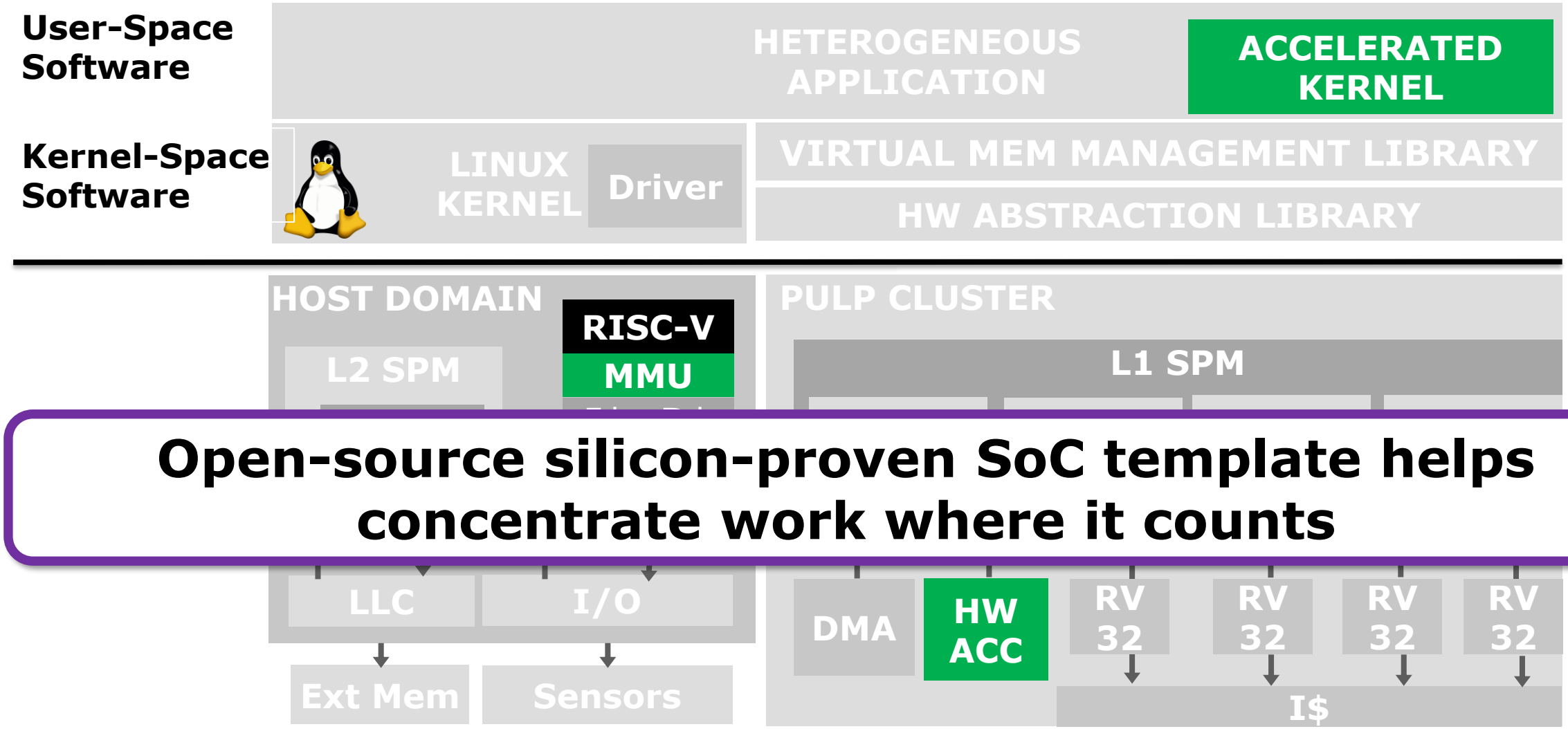
- Open source PDKs can be used with commercial tools
  - The manufacturer receives a GDS2, does not really care how it was designed.

We need all three aspects together for end-to-end open-source ICs

A modern SoC is quite complex



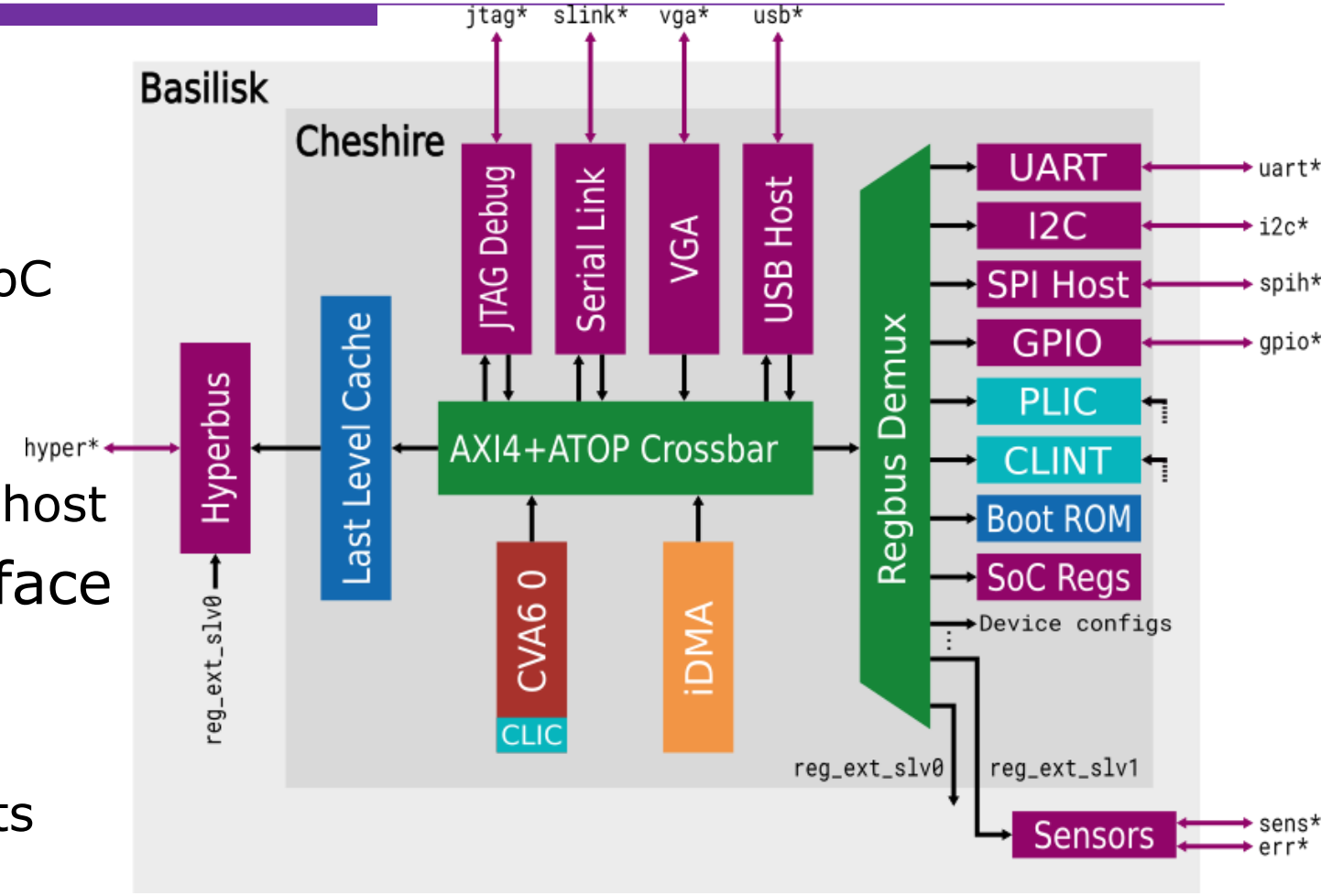
Innovation is only in part of the SoC



Open-source silicon-proven SoC template helps concentrate work where it counts

The Cheshire SoC Platform

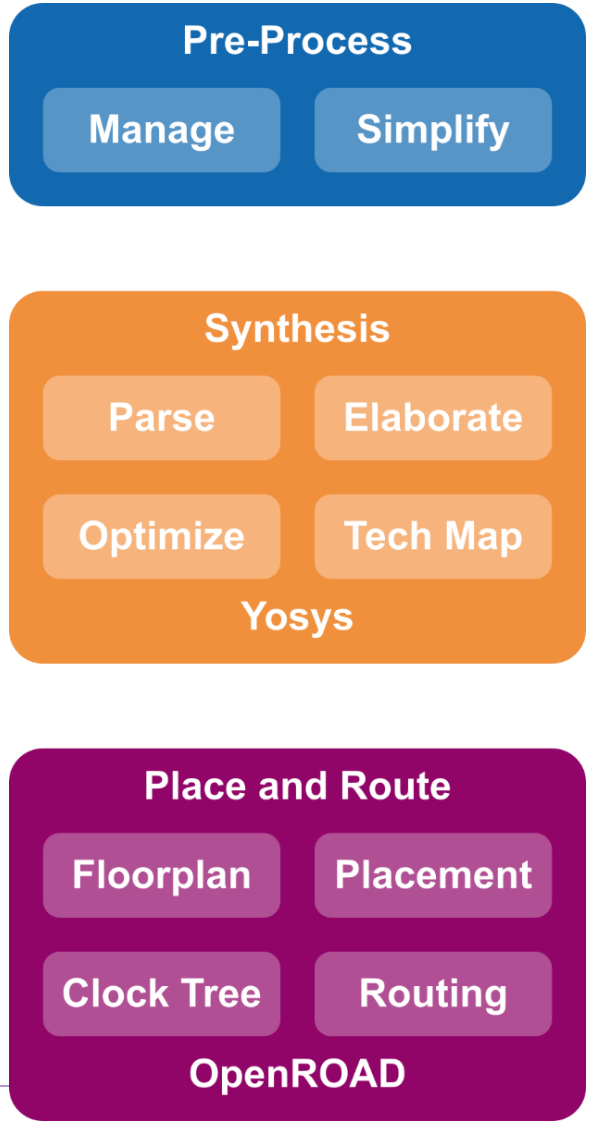
- Multi-million gate design
- 64-bit RISC-V Core
  - Complete Linux-capable SoC
  - Simple “Raspberry Pi”
- Rich Peripherals
  - Includes an open USB 1.1 host
- Open-source DRAM interface
  - Digital-only interface
- Silicon-proven
  - Multiple successful tapeouts with commercial EDA



https://github.com/pulp-platform/cheshire

Open-Source Tool-Flow of Basilisk

- Source management and pre-processing
  - Manage SystemVerilog codebase
  - Convert and simplify to Verilog
- Synthesis
  - Yosys from RTL to standard-cell netlist
  - Yosys uses ABC for high-effort logic optimization and technology mapping
- Backend
  - OpenROAD tool suite
  - Collection of leading-edge research tools



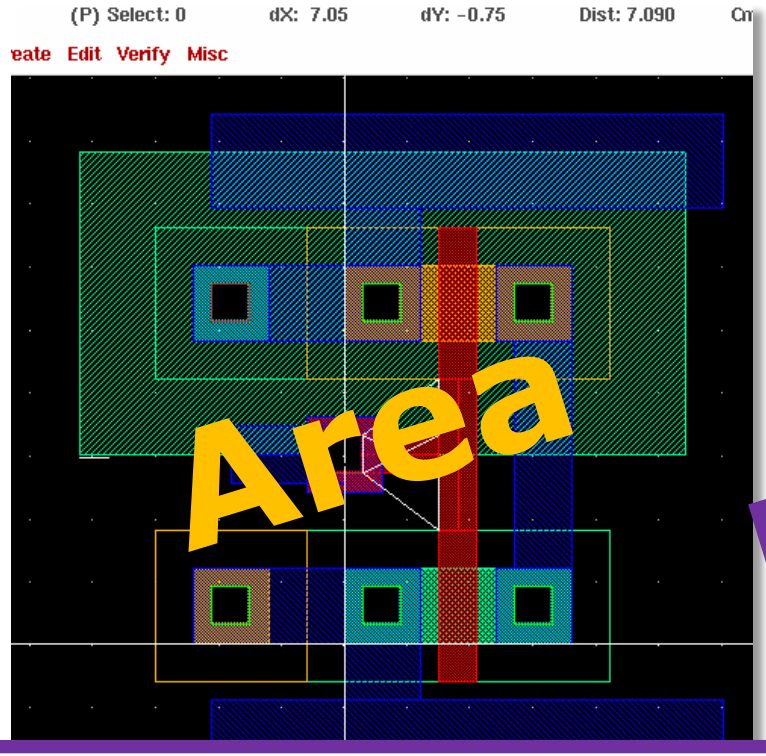
Is everything on the Basilisk flow open?

- Basilisk uses an 'almost completely open' flow
  - With a safety net: We also have commercial tools to fall back on
  - Some aspects, we ended up using commercial versions
    - DRC, LVS, backannotated gate-level simulation
    - I/O Cells in Basilisk are not the open-sourced versions
- There is a difference between available and works really well
  - The quality of results can use more improvement (at all levels)
  - Some tools would need to be re-designed to scale to larger designs
    - Runtime and resource usage could be improved

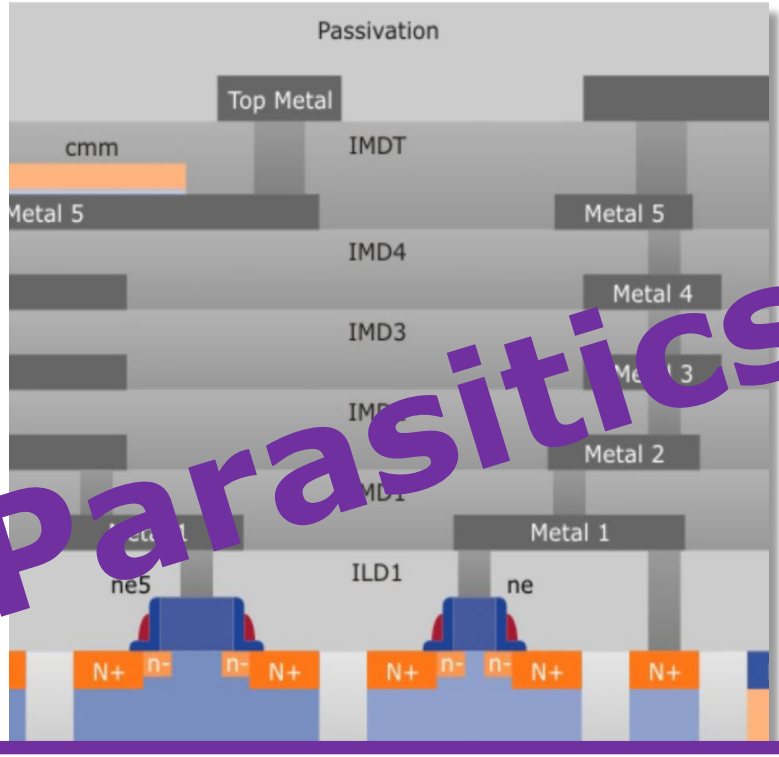
Still work to be done to cover all aspects of the flow!

What is in a process design kit?

Design Rules



Layer Stack



Transistor Models

```
** PTM-MG 20nm HSPICE Model Card for HP
** Nominal VDD=0.9V

.model nfet nmos level = 72
+ bulkmod = 1
+lmin     = 1e-008          lmax     = 2.4
*****************************************
*                          general
*****************************************
*========================= flags =======
+version  = 105.03          bulkmod  = 1
+gidlmod  = 0               iigsmod  = 0
+rgatemod = 0               igcmod   = 1
+coremod  = 0               igeomod  = 2
*========================= process =====
+eot      = 1.1e-010        eotbox   = 1.4
+nbody    = 3e+023          phig     = 4.1
+easub    = 4.05            ni0sub   = 1.1
+nsd      = 3e+026          ngate    = 0
+nseg     = 5               l        = 2.4
*========================= w/l =========
+xl       = 0               lint     = 1e-
+llc      = 0               dlc      = 0
```

Speed

You can not learn the secrets of how a fab manufactures chips through the information in the PDK!!

PDK information is not that “Secret”

- Guess what: the gate length of a transistor in a 65nm technology is: 65nm !!
  - Many of the design rules are trivial or expected from publicly available material
- Even Youtubers have the means to ‘delayer’ any given chip
  - For example “*14nm and 7nm are NOT what you think it is*” https://www.youtube.com/watch?v=1kQUXpZpLXI
  - The stack, materials, their dimensions can be obtained without much effort
- You can manufacture a chip with transistors and characterize it yourself
  - Getting transistor parameters of a given technology is not ‘difficult’

No manufacturing details disclosed by PDK!

Access to PDK is essential of OSHW

- The PDK holds the key to too many things
  - Physical layouts
  - Electrical characteristics
  - Parasitics
- This would prevent making hard IPs available openly
  - Standard cell libraries, memories, I/Os, data converters.
- Most PPA numbers would stay obfuscated
  - It is not like we can not publish any PPAs on commercial technologies
  - Can not discuss specific issues or highlight performance bottlenecks
- We also could not improve parts of the PDK
  - Only the manufacturer is normally able to make changes
  - Support for new tools, changes, updates, fixes

PDK is an enabler, not a provider!

- A successful design requires a number of things that are part of the PDK
  - But do not necessarily come as part of a PDK
  - More work is needed to provide them
- Design enablement IPs
  - Standard Cells, Memories/Memory generators, I/O cells
- Design flow issues
  - Efficient scripts, templates to realize designs in this flow.
  - Includes also simple things like fixing antenna violations to metal filling
- Analog IPs
  - Data converters, Serial I/Os, Memory controllers, PHYs for certain standards, Clocking

We need work to provide *companion* pieces to PDKs

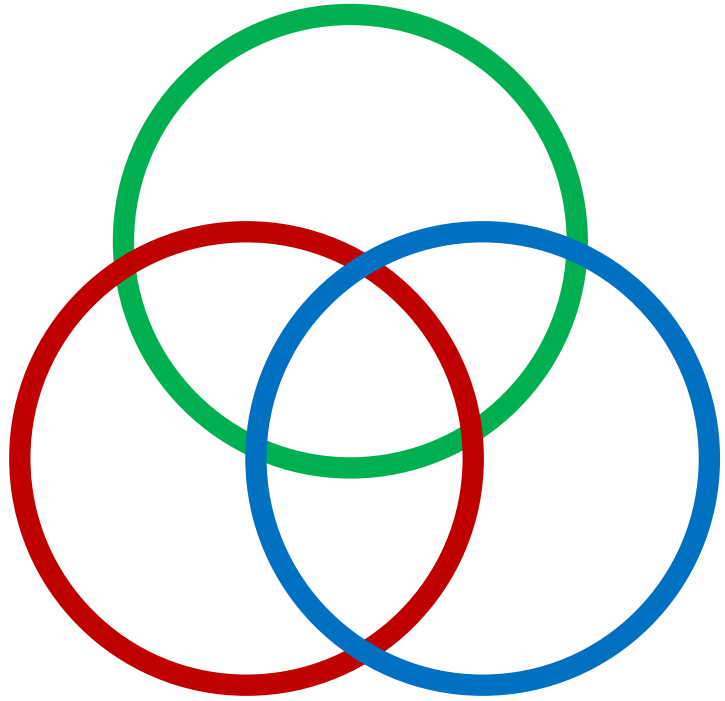
More Open PDKs are needed

- We have access to three open PDKs at the moment
  - Skywater 130nm
  - Globalfoundries 180 (500nm high-voltage flavor of their 180nm node)
  - IHP 130nm
- State of the Art from 2000-2004
  - Many exciting designs possible
- We need more
  - For more innovation: higher volume, faster turn-around, frequent MPWs
  - For more capabilities: Access to newer nodes

An Open PDK in the 65-28nm would be a game changer!

Open source HW is here to stay

- **Design**
  - Already quite established
  - Should also include hard-IP with open PDKs
- **Tools** (EDA)
  - Allows substantial designs to be completed
  - More work needed
- **Manufacturing** (PDK)
  - Need more volume, newer technologies



Exciting times ahead

PULP team will continue working !

- Open source fuels our research
  - Faster/easier collaboration
  - Verifiable results
  - Research opportunities at all levels
  - Great for education

- Follow us
  - https://pulp-platform.org
  - https://github.com/pulp-platform
  - https://x.com/pulp_platform